

# 1992 Data Book

**OVER  
40 NEW  
PRODUCTS**









## DATA BOOK

### *President's Message*

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Total customer satisfaction is Xicor's number one goal. Xicor provides the most extensive product offering to satisfy your needs in field-programmable nonvolatile microperipherals and support memory chips containing E<sup>2</sup>PROM, NOVRAM, E<sup>2</sup>POT and others. These CMOS products are available in a wide variety of speeds, voltages, package types, and a variety of interface configurations. The majority of the products are offered with extended temperature ranges, and many comply with all the requirements of MIL-STD-883 Revision C for Class B products.

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A handwritten signature in dark ink, appearing to read "R. Klein", with a stylized flourish at the end.

Raphael Klein  
President  
December, 1991

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Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829,482; 4,874,967; 4,883,976; 4,980,859; 5,012,132; 5,003,197; 5,023,694. Foreign patents and additional patents pending.

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In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

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- 2 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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## **Precautions for the Handling of MOS Devices**

---

Xicor products are designed with effective input protection to prevent damage to the devices under most conditions. However, any MOS circuit can be catastrophically damaged by excessive electrostatic discharge or transient voltages. The following procedures are recommended to avoid accidental circuit damage.

### **I. Testing MOS Circuits:**

1. All units should be handled directly from the conductive or antistatic plastic tube in which they were shipped if possible. This action minimizes touching of individual leads.
2. If units are to be tested without using the tube carrier, the following precautions should be taken:
  - a. Table surfaces which potentially will come in contact with the devices either directly or indirectly (such as through shipping tubes) must be metal or of another conductive material and should be electrically connected to the test equipment and to the test operator (a grounding bracelet is recommended).
  - b. The units should be transported in bundled antistatic tubes or metal trays, both of which will assume a common potential when placed on a conductive table top.
  - c. Do not band tubes together with adhesive tape or rubber bands without first wrapping them in a conductive layer.

### **II. Test Equipment (Including Environmental Equipment):**

1. All equipment must be properly returned to the same reference potential (ground) as the devices, the operator, and the container for the devices.
2. Devices to be tested should be protected from high voltage surges developed by:
  - a. Turning electrical equipment on or off.
  - b. Relay switching.
  - c. Transients from voltage sources (AC line or power supplies).

### **III. Assembling MOS Devices Onto PC Boards:**

1. The MOS circuits should be mounted on the PC board last.
2. Similar precautions should be taken as in Item 1 above, at the assembly work station.
3. Soldering irons or solder baths should be at the same reference (ground) potential as the devices.
4. Plastic materials which are not antistatic treated should be kept away from devices as they develop and maintain high levels of static charge.

### **IV. Device Handling:**

1. Handling of devices should be kept to a minimum. If handling is required, avoid touching the leads directly.

### **V. General:**

1. The handler should take every precaution that the device will see the same reference potential when moved.
2. Anyone handling individual devices should develop a habit of first touching the container in which the units are stored before touching the units.
3. Before placing the units into a PC board, the handler should touch the PC board first.
4. Personnel should not wear clothing which will build up static charge. They should wear smocks and clothing made of 100% cotton rather than wool or synthetic fibers.
5. Be careful of electrostatic build up through the movement of air over plastic material. This is especially true of acid sinks.
6. Personnel or operators should always wear grounded wrist straps when working with MOS devices.
7. A 1 meg ohm resistance ground strap is recommended and will protect people up to 5,000 volts AC RMS or DC by limiting current to 5 milliamperes.
8. Antistatic ionized air equipment is very effective and useful in preventing electrostatic damage.
9. Low humidity maximizes potential static problems. Maintaining humidity levels above 45% is one of the most effective ways to guard against static handling problems.



<b>NOVRAM* Data Sheets</b>	<b>1</b>
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NOVRAM is Xicor's nonvolatile static RAM device family.  
E<sup>2</sup>POT™ is a trademark of Xicor, Inc.



## X22C10

**64 x 4**

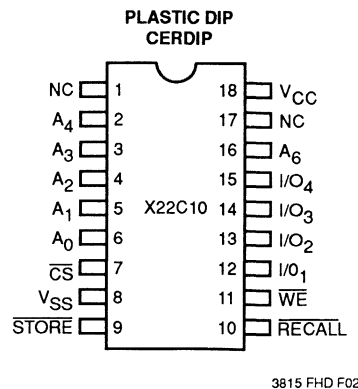
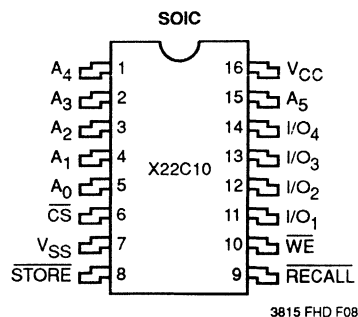
## Nonvolatile Static RAM

### DESCRIPTION

- The X22C10 is a 64 x 4 CMOS NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a non-volatile E<sup>2</sup>PROM. The NOVRAM design allows data to be easily transferred from RAM to E<sup>2</sup>PROM (STORE) and from E<sup>2</sup>PROM to RAM (RECALL). The STORE operation is completed within 5 ms or less and the RECALL is completed within 1 us.

Xicor NOVRAms are designed for unlimited write operations to the RAM, either RECALLs from E<sup>2</sup>PROM or writes from the host. The X22C10 will reliably endure 1,000,000 STORE cycles. Inherent data retention is greater than 100 years.

## PIN CONFIGURATION



## X22C10

### PIN DESCRIPTIONS AND DEVICE OPERATION

#### Addresses ( $A_0$ – $A_5$ )

The address inputs select a 4-bit memory location during a read or write operation.

#### Chip Select ( $\overline{CS}$ )

The Chip Select input must be LOW to enable read or write operations with the RAM array.  $\overline{CS}$  HIGH will place the I/O pins in the high impedance state.

#### Write Enable ( $\overline{WE}$ )

The Write Enable input controls the I/O buffers, determining whether a RAM read or write operation is enabled. When  $\overline{CS}$  is LOW and  $\overline{WE}$  is HIGH the I/O pins will output data from the selected RAM address locations. When both  $\overline{CS}$  and  $\overline{WE}$  are LOW, data presented at the I/O pins will be written to the selected address location.

#### Data In/Data Out ( $I/O_1$ – $I/O_4$ )

Data is written to or read from the X22C10 through the I/O pins. The I/O pins are placed in the high impedance state when either  $\overline{CS}$  is HIGH or during either a store or recall operation.

#### STORE

The STORE input, when LOW, will initiate the transfer of the entire contents of the RAM array to the E<sup>2</sup>PROM array. The  $\overline{WE}$  and  $\overline{RECALL}$  inputs are inhibited during the store cycle. The store operation is completed in 5 ms or less.

A store operation has priority over RAM read/write operations. If STORE is asserted during a read operation, the read will be discontinued. If STORE is asserted during a RAM write operation, the write will be immediately terminated and the store performed. The data at the RAM address that was being written will be unknown in both the RAM and E<sup>2</sup>PROM arrays.

#### RECALL

The  $\overline{RECALL}$  input, when LOW, will initiate the transfer of the entire contents of the E<sup>2</sup>PROM array to the RAM array. The transfer of data will be completed in 1  $\mu$ s or less.

An array recall has priority over RAM read/write operations and will terminate both operations when  $\overline{RECALL}$  is asserted.  $\overline{RECALL}$  LOW will also inhibit the STORE input.

#### Automatic Recall

Upon power-up the X22C10 will automatically recall data from the E<sup>2</sup>PROM array into the RAM array.

#### Write Protection

The X22C10 has three write protect features that are employed to protect the contents of the nonvolatile memory.

- V<sub>CC</sub> Sense—All functions are inhibited when V<sub>CC</sub> is <3.5V typical.
- Write Inhibit—Holding either  $\overline{STORE}$  HIGH or  $\overline{RECALL}$  LOW during power-up or power-down will prevent an inadvertent store operation and E<sup>2</sup>PROM data integrity will be maintained.
- Noise Protection—A STORE pulse of typically less than 20 ns will *not* initiate a store cycle.

#### PIN NAMES

Symbol	Description
$A_0$ – $A_5$	Address Inputs
$I/O_1$ – $I/O_4$	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{RECALL}$	Recall
$\overline{STORE}$	Store
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

3815 PGM T01

X22C10

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .....-65°C to +135°C  
Storage Temperature .....-65°C to +150°C  
Voltage on any Pin With  
    Respect to Ground .....-1.0V to +7.0V  
D.C. Output Current ..... 5 mA  
Lead Temperature  
    (Soldering, 10 Seconds) .....300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

3815 PGM T12

Supply Voltage	Limits
X22C10	5V ±10%

3815 PGM T13

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Supply Current, RAM Read/Write		40	mA	$\overline{CS} = V_{IL}$ , I/Os = Open, All Others = V <sub>IH</sub> , Addresses = 0.4V/2.4V Levels @ f = 8 MHz
I <sub>SB1</sub>	V <sub>CC</sub> Standby Current (TTL Inputs)		2	mA	Store or Recall Functions Not Active, I/Os = Open, All Other Inputs = V <sub>IH</sub>
I <sub>SB2</sub>	V <sub>CC</sub> Standby Current (CMOS Inputs)		100	µA	Store or Recall functions Not Active, I/Os = Open, All Other Inputs = V <sub>CC</sub> -0.3V
I <sub>LI</sub>	Input Leakage Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> (2)	Input Low Voltage	-1.0	0.8	V	
V <sub>IH</sub> (2)	Input High Voltage	2.0	V <sub>CC</sub> + 1.0	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 4.2 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -2.0 mA

3815 PGM T02

CAPACITANCE T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C <sub>I/O</sub> (1)	Input/Output Capacitance	8	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (1)	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

3815 PGM T03

Notes: (1) This parameter is periodically sampled and not 100% tested.  
(2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.



X22C10

MODE SELECTION

CE	WE	RECALL	STORE	I/O	Mode
H	X	H	H	Output High Z	Not Selected <sup>(3)</sup>
L	H	H	H	Output Data	Read RAM
L	L	H	H	Input Data High	Write "1" RAM
L	L	H	H	Input Data Low	Write "0" RAM
X	H	L	H	Output High Z	Array Recall
H	X	L	H	Output High Z	Array Recall
X	H	H	L	Output High Z	Nonvolatile Storing <sup>(4)</sup>
H	X	H	L	Output High Z	Nonvolatile Storing <sup>(4)</sup>

3815 PGM T05

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

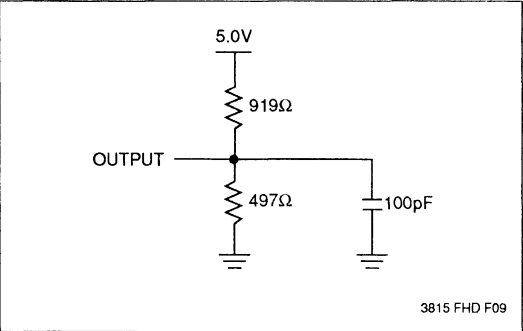
3815 PGM T07

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t <sub>PUR</sub> <sup>(5)</sup>	Power-up to Read Operation	100	μs
t <sub>PUW</sub> <sup>(5)</sup>	Power-up to Write or Store Operation	5	ms

3815 PGM T07

EQUIVALENT A.C. LOAD CIRCUIT



3815 FHD F09

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3815 PGM T04

- Notes:** (3) Chip is deselected but may be automatically completing a store cycle.  
(4)  $\overline{\text{STORE}} = \text{LOW}$  is required only to initiate the store cycle, after which the store cycle will be automatically completed (e.g.  $\overline{\text{STORE}} = \text{X}$ ).  
(5) t<sub>PUR</sub> and t<sub>PUW</sub> are the delays required from the time V<sub>CC</sub> is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

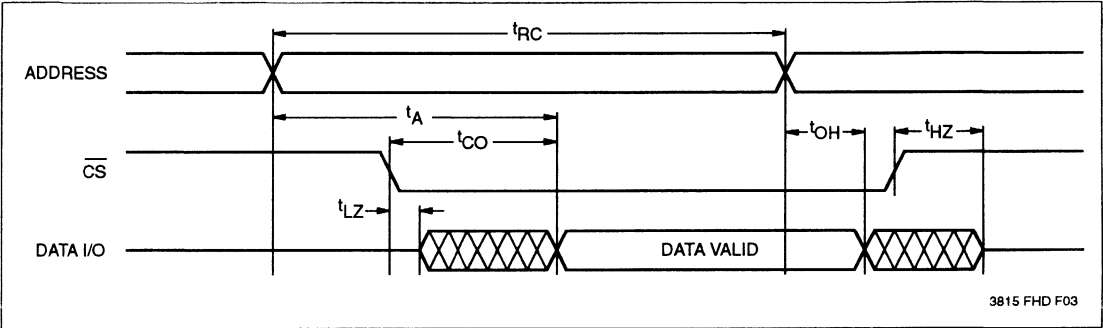
X22C10

A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)  
Read Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t <sub>RC</sub>	Read Cycle Time	120		ns
t <sub>AA</sub>	Access Time		120	ns
t <sub>CO</sub>	Chip Select to Output Valid		120	ns
t <sub>OH</sub>	Output Hold from Address Change	0		ns
t <sub>LZ</sub> <sup>(6)</sup>	Chip Select to Output in Low Z	0		ns
t <sub>HZ</sub> <sup>(6)</sup>	Chip Deselect to Output in High Z		50	ns

3815 PGM T08

Read Cycle



3815 FHD F03

Note: (6) t<sub>LZ</sub> min. and t<sub>HZ</sub> min. are periodically sampled and not 100% tested.

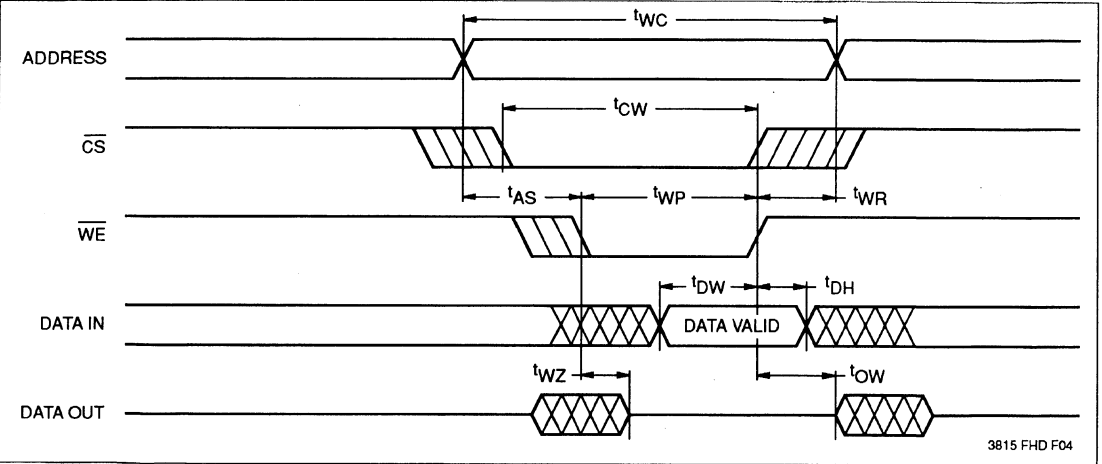
# X22C10

## Write Cycle Limits

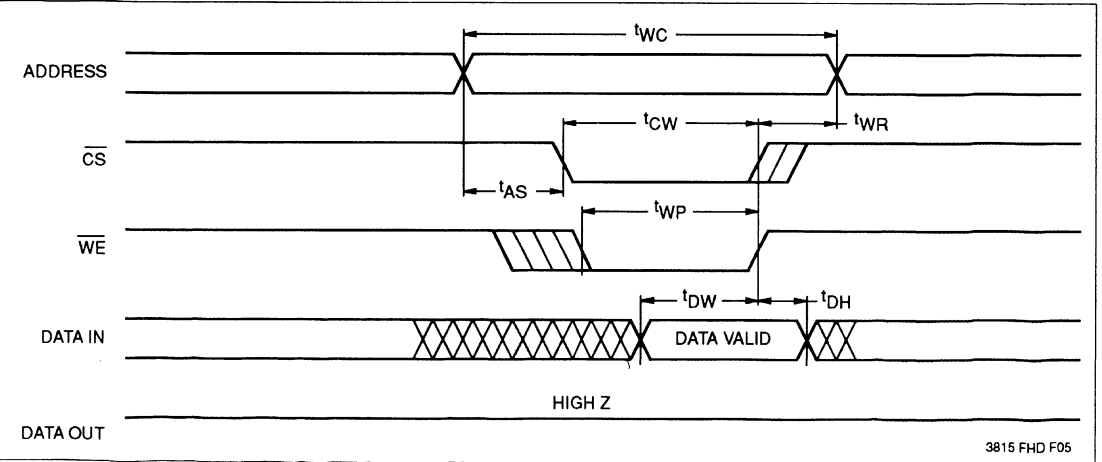
Symbol	Parameter	Min.	Max.	Units
$t_{WC}$	Write Cycle Time	120		ns
$t_{CW}$	Chip Select to End of Write	90		ns
$t_{AS}$	Address Setup Time	0		ns
$t_{WP}$	Write Pulse Width	90		ns
$t_{WR}$	Write Recovery Time	0		ns
$t_{DW}$	Data Valid to End of Write	40		ns
$t_{DH}$	Data Hold Time	0		ns
$t_{WZ}$	Write Enable to Output in High Z		50	ns
$t_{OW}$	Output Active from End of Write	0		ns

3815 PGM T09

## Write Cycle



## Early Write Cycle



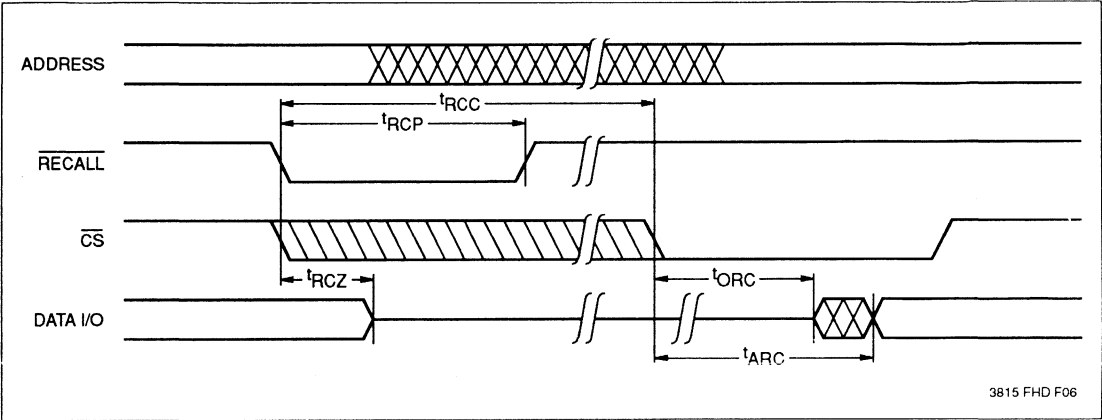
X22C10

Recall Cycle Limits

Symbol	Parameter	Min.	Max.	Units
$t_{RCC}$	Array Recall Time		1200	$\mu$ s
$t_{RCP}$	Recall Pulse Width <sup>(6)</sup>	90		ns
$t_{RCZ}$	Recall to Output in High Z		50	ns
$t_{ORC}$	Output Active from End of Recall	0		ns
$t_{ARC}$	Recalled Data Access Time from End of Recall		150	ns

3815 PGM T10

Recall Cycle



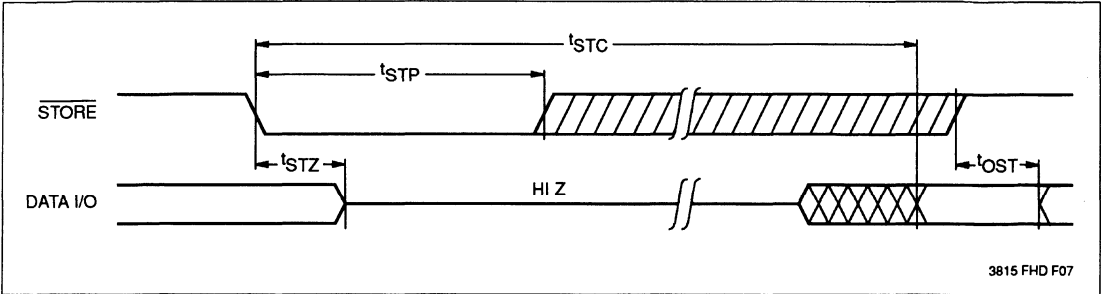
X22C10

Store Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t <sub>STC</sub>	Internal Store Time		5	ms
t <sub>STP</sub>	Store Pulse Width	90		ns
t <sub>STZ</sub>	Store to Output in High Z		50	ns
t <sub>OST</sub>	Output Active from End of Store	0		ns

3815 PGM T11

Store Cycle Limits



3815 FHD F07

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

1K Bit

X22C12

256 x 4

## Nonvolatile Static RAM

### FEATURES

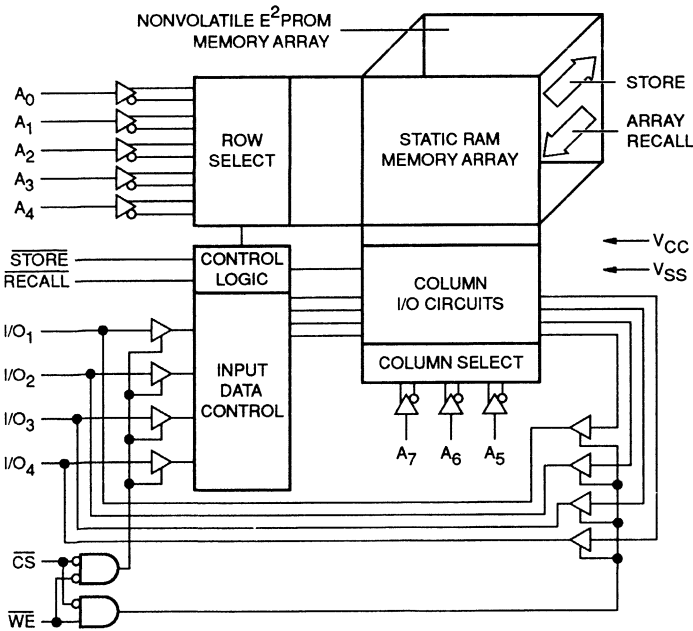
- High Performance CMOS
  - 120 ns RAM Access Time
- High Reliability
  - Store Cycles: 1,000,000
  - Data Retention: 100 Years
- Low Power Consumption
  - Active: 40 mA Max.
  - Standby: 100  $\mu$ A Max.
- Infinite Array Recall, RAM Read and Write Cycles
- Nonvolatile Store Inhibit:  $V_{CC} = 3.5V$  Typical
- Fully TTL and CMOS Compatible
- JEDEC Standard 18-Pin 300-mil DIP
- 100% Compatible with X2212
  - With Timing Enhancements

### DESCRIPTION

The X22C12 is a 256 x 4 CMOS NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a non-volatile E<sup>2</sup>PROM. The NOVRAM design allows data to be easily transferred from RAM to E<sup>2</sup>PROM (STORE) and from E<sup>2</sup>PROM to RAM (RECALL). The STORE operation is completed within 5 ms or less and the RECALL is completed within 1  $\mu$ s.

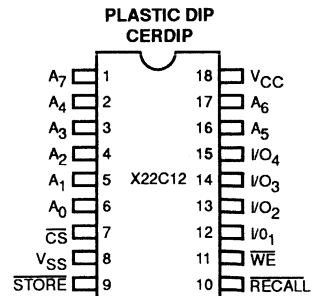
Xicor NOVRAMs are designed for unlimited write operations to the RAM, either RECALLs from E<sup>2</sup>PROM or writes from the host. The X22C12 will reliably endure 1,000,000 STORE cycles. Inherent data retention is greater than 100 years.

### FUNCTIONAL DIAGRAM

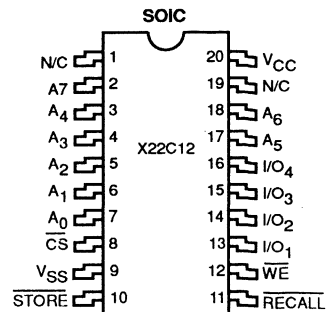


3817 FHD F01

### PIN CONFIGURATION



3817 FHD F02



3817 FHD F10

# X22C12

## PIN DESCRIPTIONS AND DEVICE OPERATION

### Addresses (A<sub>0</sub>–A<sub>7</sub>)

The address inputs select a 4-bit memory location during a read or write operation.

### Chip Select ( $\overline{\text{CS}}$ )

The Chip Select input must be LOW to enable read or write operations with the RAM array.  $\overline{\text{CS}}$  HIGH will place the I/O pins in the high impedance state.

### Write Enable ( $\overline{\text{WE}}$ )

The Write Enable input controls the I/O buffers, determining whether a RAM read or write operation is enabled. When  $\overline{\text{CS}}$  is LOW and  $\overline{\text{WE}}$  is HIGH the I/O pins will output data from the selected RAM address locations. When both  $\overline{\text{CS}}$  and  $\overline{\text{WE}}$  are LOW, data presented at the I/O pins will be written to the selected address location.

### Data In/Data Out (I/O<sub>1</sub>–I/O<sub>4</sub>)

Data is written to or read from the X22C12 through the I/O pins. The I/O pins are placed in the high impedance state when either  $\overline{\text{CS}}$  is HIGH or during either a store or recall operation.

### $\overline{\text{STORE}}$

The  $\overline{\text{STORE}}$  input, when LOW, will initiate the transfer of the entire contents of the RAM array to the E<sup>2</sup>PROM array. The  $\overline{\text{WE}}$  and  $\overline{\text{RECALL}}$  inputs are inhibited during the store cycle. The store operation is completed in 5 ms or less.

A store operation has priority over RAM read/write operations. If  $\overline{\text{STORE}}$  is asserted during a read operation, the read will be discontinued. If  $\overline{\text{STORE}}$  is asserted during a RAM write operation, the write will be immediately terminated and the store performed. The data at the RAM address that was being written will be unknown in both the RAM and E<sup>2</sup>PROM arrays.

### $\overline{\text{RECALL}}$

The  $\overline{\text{RECALL}}$  input, when LOW, will initiate the transfer of the entire contents of the E<sup>2</sup>PROM array to the RAM array. The transfer of data will be completed in 1  $\mu$ s or less.

An array recall has priority over RAM read/write operations and will terminate both operations when  $\overline{\text{RECALL}}$  is asserted.  $\overline{\text{RECALL}}$  LOW will also inhibit the  $\overline{\text{STORE}}$  input.

### Automatic Recall

Upon power-up the X22C12 will automatically recall data from the E<sup>2</sup>PROM array into the RAM array.

### Write Protection

The X22C12 has three write protect features that are employed to protect the contents of the nonvolatile memory.

- V<sub>CC</sub> Sense—All functions are inhibited when V<sub>CC</sub> is <3.5V typical.
- Write Inhibit—Holding either  $\overline{\text{STORE}}$  HIGH or  $\overline{\text{RECALL}}$  LOW during power-up or power-down will prevent an inadvertent store operation and E<sup>2</sup>PROM data integrity will be maintained.
- Noise Protection—A  $\overline{\text{STORE}}$  pulse of typically less than 20 ns will *not* initiate a store cycle.

## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>7</sub>	Address Inputs
I/O <sub>1</sub> –I/O <sub>4</sub>	Data Inputs/Outputs
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CS}}$	Chip Select
$\overline{\text{RECALL}}$	Recall
$\overline{\text{STORE}}$	Store
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

3817 PGM T01

# X22C12

## ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .....	–65°C to +135°C
Storage Temperature .....	–65°C to +150°C
Voltage on any Pin With Respect to Ground .....	–1.0V to +7.0V
D.C. Output Current .....	5 mA
Lead Temperature (Soldering, 10 Seconds) .....	300°C

## COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3817 PGM T12

Supply Voltage	Limits
X22C12	5V ±10%

3817 PGM T13

## D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Supply Current, RAM Read/Write		40	mA	$\overline{CS} = V_{IL}$ , I/Os = Open, All Others = V <sub>IH</sub> , Addresses = 0.4V/2.4V Levels @ f = 8 MHz
I <sub>SB1</sub>	V <sub>CC</sub> Standby Current (TTL Inputs)		2	mA	Store or Recall Functions Not Active, I/Os = Open, All Other Inputs = V <sub>IH</sub>
I <sub>SB2</sub>	V <sub>CC</sub> Standby Current (CMOS Inputs)		100	μA	Store or Recall functions Not Active, I/Os = Open, All Other Inputs = V <sub>CC</sub> – 0.3V
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> (2)	Input Low Voltage	–1.0	0.8	V	
V <sub>IH</sub> (2)	Input High Voltage	2.0	V <sub>CC</sub> + 1.0	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 4.2 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = –2.0 mA

3817 PGM T02

## CAPACITANCE T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C <sub>I/O</sub> (1)	Input/Output Capacitance	8	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (1)	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

3815 PGM T03

Notes: (1) This parameter is periodically sampled and not 100% tested.  
(2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.



X22C12

MODE SELECTION

CE	WE	RECALL	STORE	I/O	Mode
H	X	H	H	Output High Z	Not Selected <sup>(3)</sup>
L	H	H	H	Output Data	Read RAM
L	L	H	H	Input Data High	Write "1" RAM
L	L	H	H	Input Data Low	Write "0" RAM
X	H	L	H	Output High Z	Array Recall
H	X	L	H	Output High Z	Array Recall
X	H	H	L	Output High Z	Nonvolatile Storing <sup>(4)</sup>
H	X	H	L	Output High Z	Nonvolatile Storing <sup>(4)</sup>

3817 PGM T05

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

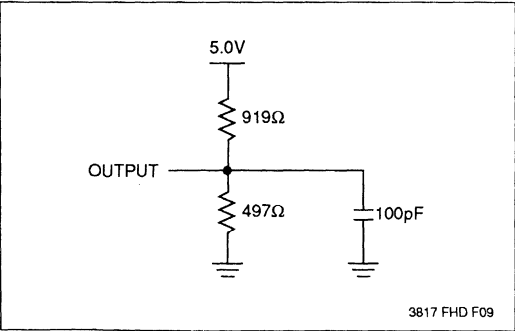
3817 PGM T06

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t <sub>PUR</sub> <sup>(5)</sup>	Power-up to Read Operation	100	μs
t <sub>PW</sub> <sup>(5)</sup>	Power-up to Write or Store Operation	5	ms

3817 PGM T07

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3817 PGM T04

- Notes:** (3) Chip is deselected but may be automatically completing a store cycle.  
(4) STORE = LOW is required only to initiate the store cycle, after which the store cycle will be automatically completed (e.g. STORE = X).  
(5) t<sub>PUR</sub> and t<sub>PW</sub> are the delays required from the time V<sub>CC</sub> is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

# X22C12

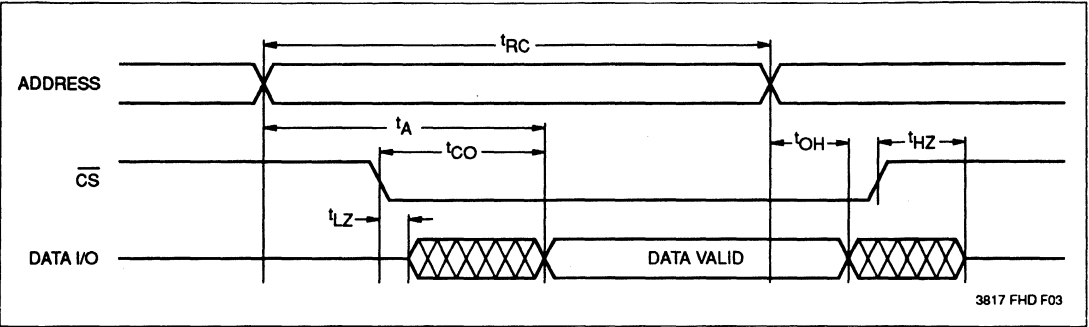
## A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

### Read Cycle Limits

Symbol	Parameter	Min.	Max.	Units
$t_{RC}$	Read Cycle Time	150		ns
$t_{AA}$	Access Time		150	ns
$t_{CO}$	Chip Select to Output Valid		150	ns
$t_{OH}$	Output Hold from Address Change	0		ns
$t_{LZ}^{(6)}$	Chip Select to Output in Low Z	0		ns
$t_{HZ}^{(6)}$	Chip Deselect to Output in High Z		50	ns

3817 PGM T08

### Read Cycle



3817 FHD F03

**Note:** (6)  $t_{LZ}$  min. and  $t_{HZ}$  min. are periodically sampled and not 100% tested.

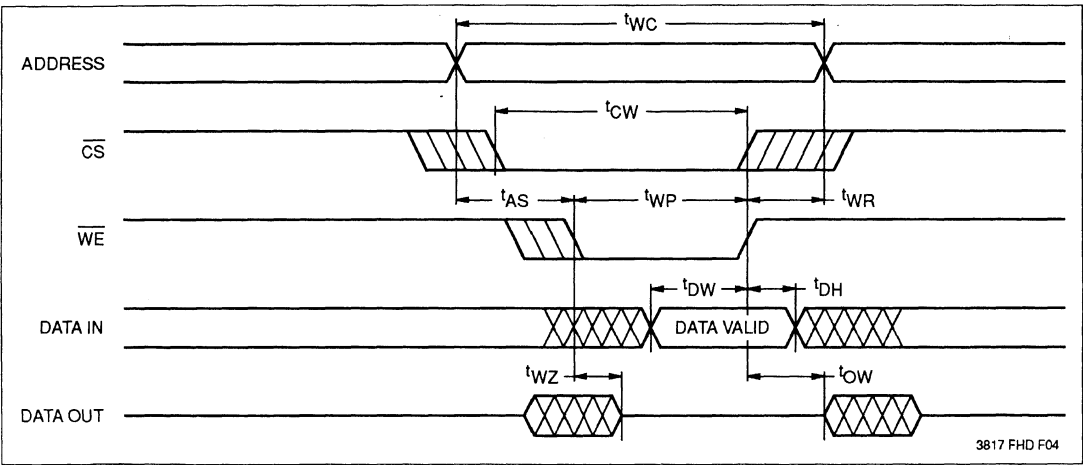
X22C12

Write Cycle Limits

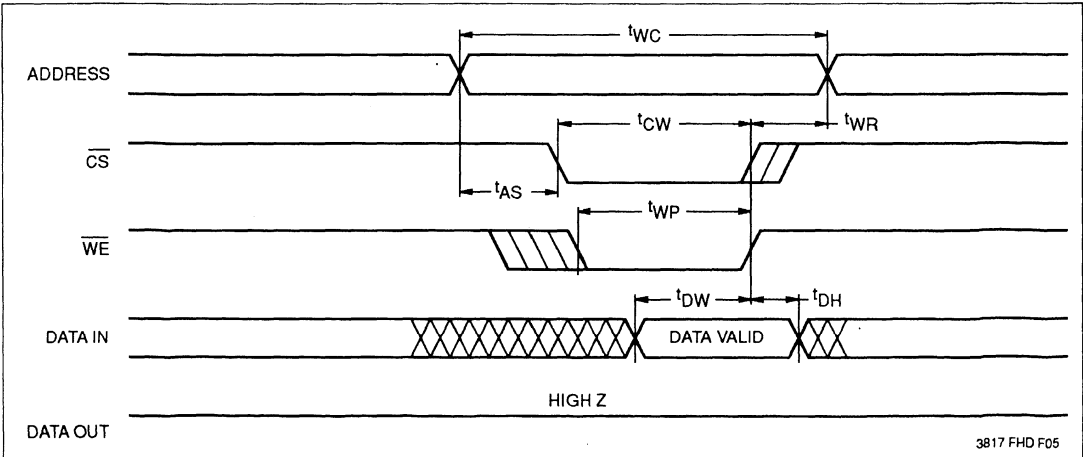
Symbol	Parameter	Min.	Max.	Units
$t_{WC}$	Write Cycle Time	150		ns
$t_{CW}$	Chip Select to End of Write	90		ns
$t_{AS}$	Address Setup Time	0		ns
$t_{WP}$	Write Pulse Width	90		ns
$t_{WR}$	Write Recovery Time	0		ns
$t_{DW}$	Data Valid to End of Write	40		ns
$t_{DH}$	Data Hold Time	0		ns
$t_{WZ}$	Write Enable to Output in High Z		50	ns
$t_{OW}$	Output Active from End of Write	0		ns

3817 PGM T09

Write Cycle



Early Write Cycle



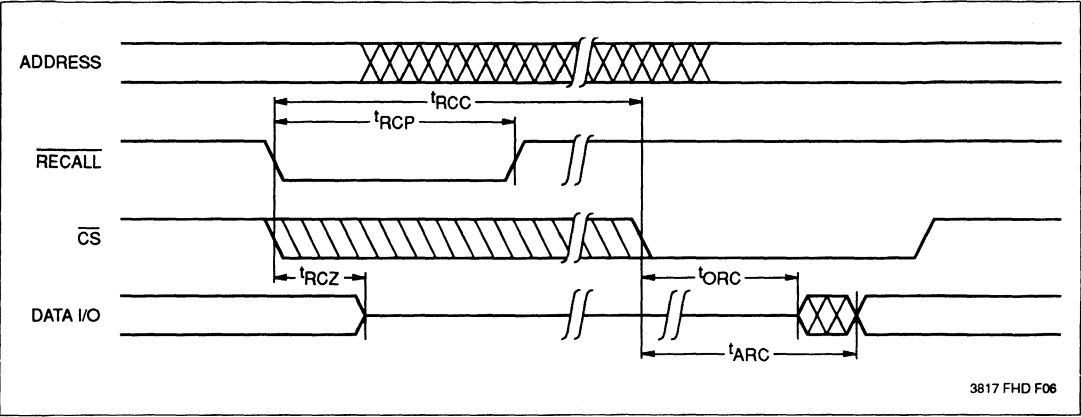
X22C12

Recall Cycle Limits

Symbol	Parameter	Min.	Max.	Units
$t_{RCC}$	Array Recall Time		1	$\mu$ s
$t_{RCP}^{(7)}$	Recall Pulse Width	90		ns
$t_{RCZ}$	Recall to Output in High Z		50	ns
$t_{ORC}$	Output Active from End of Recall	0		ns
$t_{ARC}$	Recalled Data Access Time from End of Recall		150	ns

3817 PGM T10

Recall Cycle



1

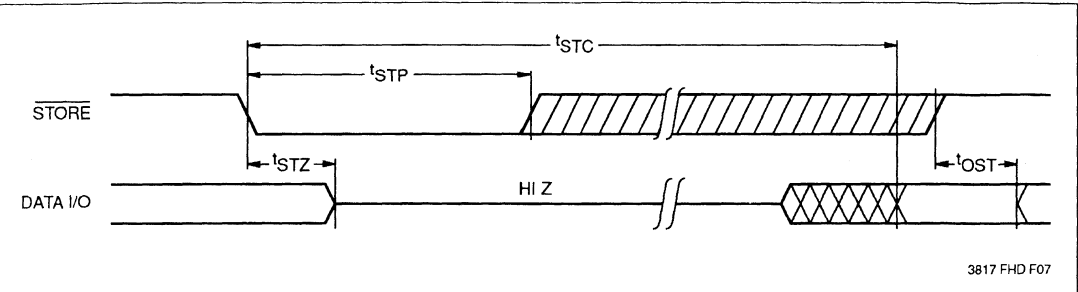
X22C12

Store Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t <sub>STC</sub>	Internal Store Time		5	ms
t <sub>STP</sub>	Store Pulse Width	90		ns
t <sub>STZ</sub>	Store to Output in High Z		50	ns
t <sub>OST</sub>	Output Active from End of Store	0		ns

3817 PGM T11

Store Cycle Limits



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance



4K

X20C04

512 x 8 Bit

Nonvolatile Static RAM

FEATURES

- High Reliability
  - Endurance: 1,000,000 Store Operations
  - Retention: 100 Years Minimum
- Power-on Recall
  - E<sup>2</sup>PROM Data Automatically Recalled Into SRAM Upon Power-up
- Lock Out Inadvertent Store Operations
- Low Power CMOS
  - Standby: 250μA
- Infinite E<sup>2</sup>PROM Array Recall, and RAM Read and Write Cycles
- Compatible with X2004

DESCRIPTION

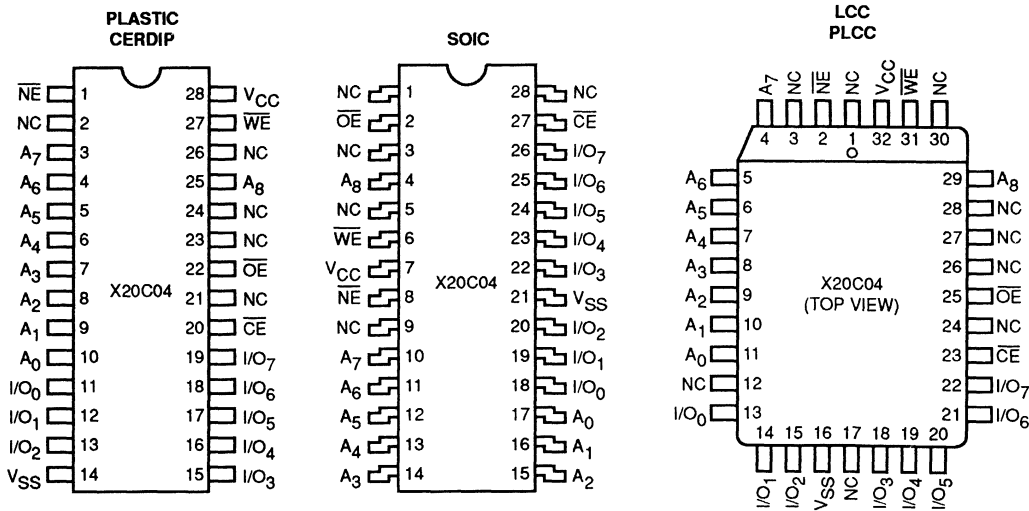
The Xicor X20C04 is a 512 x 8 NOVRAM featuring a static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E<sup>2</sup>PROM). The X20C04 is fabricated with advanced CMOS floating gate technology to achieve low power and wide power-supply margin. The X20C04 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, EPROMs and E<sup>2</sup>PROMs.

The NOVRAM design allows data to be easily transferred from RAM to E<sup>2</sup>PROM (store) and E<sup>2</sup>PROM to RAM (recall). The store operation is completed in 5 ms or less and the recall operation is completed in 5 μs or less.

Xicor NOVRAMS are designed for unlimited write operations to RAM, either from the host or recalls from E<sup>2</sup>PROM, and a minimum 1,000,000 store operations to the E<sup>2</sup>PROM. Data retention is specified to be greater than 100 years.

1

PIN CONFIGURATION



3825 FHD F02

3825 FHD F16

3825 FHD F03

# X20C04

## PIN DESCRIPTIONS

### Addresses (A<sub>0</sub>–A<sub>8</sub>)

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{CE}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH, power consumption is reduced.

### Output Enable ( $\overline{OE}$ )

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of  $\overline{CE}$ ,  $\overline{WE}$  or  $\overline{NE}$ .

### Data In/Data Out (I/O<sub>0</sub>–I/O<sub>7</sub>)

Data is written to or read from the X20C04 through the I/O pins. The I/O pins are placed in the high impedance state when either  $\overline{CE}$  or  $\overline{OE}$  is HIGH or when  $\overline{NE}$  is LOW.

### Write Enable ( $\overline{WE}$ )

The Write Enable input controls the writing of data to both the static RAM and stores to the E<sup>2</sup>PROM.

### Nonvolatile Enable ( $\overline{NE}$ )

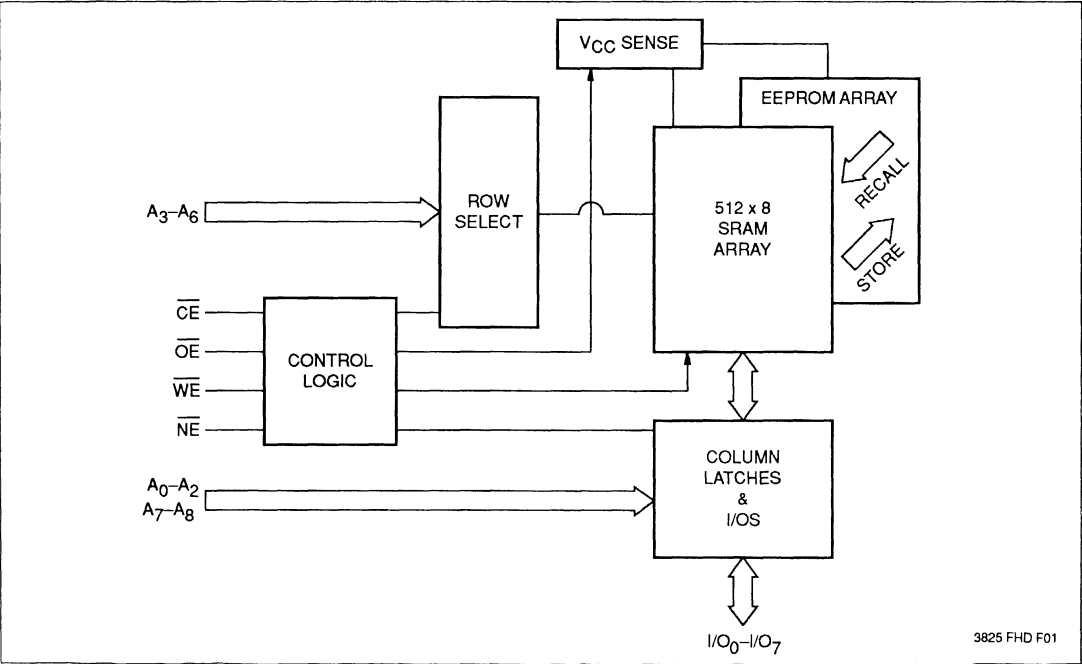
The Nonvolatile Enable input controls all accesses to the E<sup>2</sup>PROM array (store and recall functions).

## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>8</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{NE}$	Nonvolatile Enable
VCC	+5V
VSS	Ground
NC	No Connect

3825 PGM T01

## FUNCTIONAL DIAGRAM



3825 FHD F01

# X20C04

## DEVICE OPERATION

The  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{WE}$  and  $\overline{NE}$  inputs control the X20C04 operation. The X20C04 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH, or when  $\overline{NE}$  is LOW.

### RAM Operations

RAM read and write operations are performed as they would be with any static RAM. A read operation requires  $\overline{CE}$  and  $\overline{OE}$  to be LOW with  $\overline{WE}$  and  $\overline{NE}$  HIGH. A write operation requires  $\overline{CE}$  and  $\overline{WE}$  to be LOW with  $\overline{NE}$  HIGH. There is no limit to the number of read or write operations performed to the RAM portion of the X20C04.

### Nonvolatile Operations

With  $\overline{NE}$  LOW, recall operation is performed in the same manner as RAM read operation. A recall operation causes the entire contents of the E<sup>2</sup>PROM to be written into the RAM array. The time required for the operation to complete is 5 $\mu$ s or less. A store operation causes the entire contents of the RAM array to be stored in the nonvolatile E<sup>2</sup>PROM. The time for the operation to complete is 5 ms or less.

### Power-Up Recall






Upon power-up ( $V_{CC}$ ), the X20C04 performs an automatic array recall. When  $V_{CC}$  minimum is reached, the recall is initiated, regardless of the state of  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{WE}$  and  $\overline{NE}$ .

### Write Protection

The X20C04 has five write protect features that are employed to protect the contents of both the nonvolatile memory and the RAM.

- $V_{CC}$  Sense—All functions are inhibited when  $V_{CC}$  is  $\leq 3.5V$ .
- A RAM write is required before a Store Cycle is initiated.
- Write Inhibit—Holding either  $\overline{OE}$ ,  $\overline{WE}$  high,  $\overline{CE}$  high or  $\overline{NE}$  high during power up and power down will prevent an inadvertent store operation.
- Noise Protection—A combined  $\overline{WE}$ ,  $\overline{NE}$ ,  $\overline{OE}$  and  $\overline{CE}$  pulse of less than 20ns will not initiate a Store Cycle.
- Noise Protection—A combined  $\overline{WE}$ ,  $\overline{NE}$ ,  $\overline{OE}$  and  $\overline{CE}$  pulse of less than 20ns will not initiate a recall cycle.

### SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance



X20C04

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....-65°C to +135°C  
Storage Temperature .....-65°C to +150°C  
Voltage on any Pin with  
    Respect to Ground .....-1.0V to +7V  
D.C. Output Current .....10mA

\*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

3825 PGM T02

Supply Voltage	Limits
X20C04	5V ±10%

3825 PGM T03

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I <sub>CC1</sub>	V <sub>CC</sub> Current (Active)		100	mA	NE = WE = V <sub>IH</sub> , CE = OE = V <sub>IL</sub> Address Inputs = 0.4V/2.4V levels @ f = 5MHz. All I/Os = Open
I <sub>CC2</sub>	V <sub>CC</sub> Current During Store		10	mA	All Inputs = V <sub>IH</sub> All I/Os = Open
I <sub>SB1</sub>	V <sub>CC</sub> Standby Current (TTL Input)		10	mA	CE = V <sub>IH</sub> All Other Inputs = V <sub>IH</sub> , All I/Os = Open
I <sub>SB2</sub>	V <sub>CC</sub> Standby Current (CMOS Input)		250	µA	All Inputs = V <sub>CC</sub> - 0.3 All I/Os = Open
I <sub>LI</sub>	Input Leakage Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , CE = V <sub>IH</sub>
V <sub>IL</sub> (1)	Input Low Voltage	-1.0	0.8	V	
V <sub>IH</sub> (1)	Input High Voltage	2.0	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2.1mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -400µA

3825 PGM T04

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t <sub>PUR</sub> (2)	Power-Up to RAM Operation	100	µs
t <sub>PUW</sub> (2)	Power-Up to Nonvolatile Operation	5	ms

3825 PGM T05

CAPACITANCE T<sub>A</sub> = 25°C, F = 1.0MHZ, V<sub>CC</sub> = 5V.

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (2)	Input/Output Capacitance	10	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (2)	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

3825 PGM T06

Notes: (1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.

X20C04

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Changes/Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

3825 PGM T07

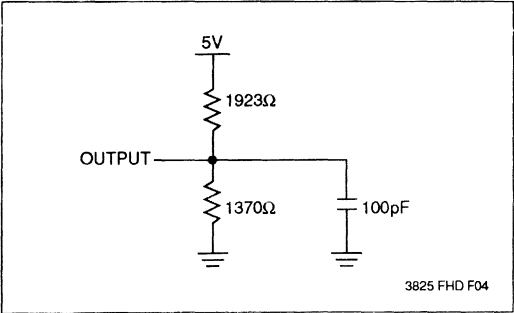
1

MODE SELECTION

CE	WE	NE	OE	Mode	I/O	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	H	L	Read RAM	Output Data	Active
L	L	H	X	Write "1" RAM	Input Data High	Active
L	L	H	X	Write "0" RAM	Input Data Low	Active
L	H	L	L	Array Recall	Output High Z	Active
L	L	L	H	Nonvolatile Storing	Output High Z	Active
L	H	H	H	Output Disabled	Output High Z	Active
L	L	L	L	Not Allowed	Output High Z	Active
L	H	L	H	No Operation	Output High Z	Active

3825 PGM T09

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V

3825 PGM T08

# X20C04

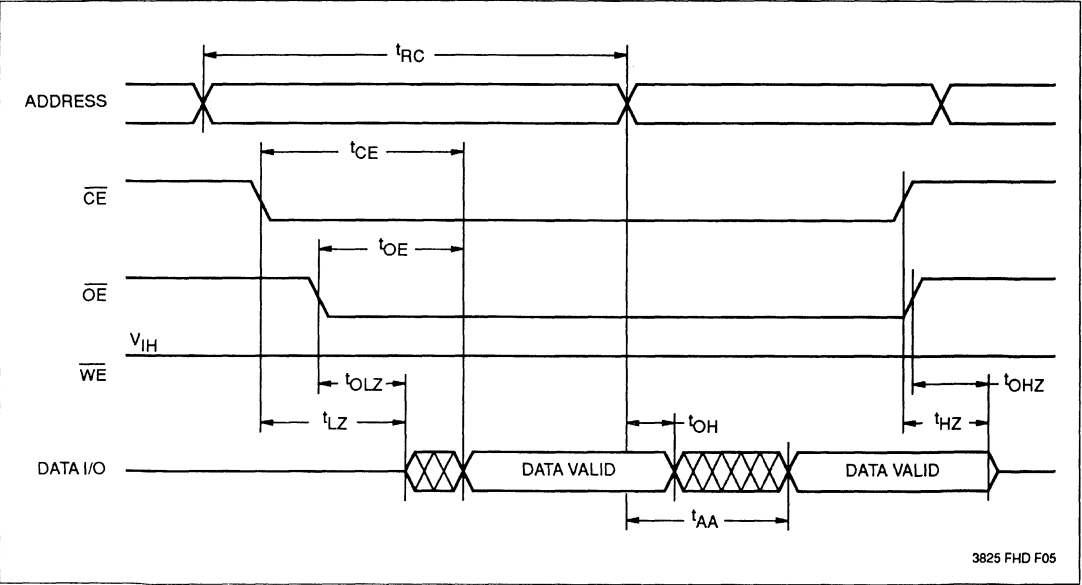
## A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

### Read Cycle Limits

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	150		200		250		300		ns
t <sub>CE</sub>	Chip Enable Access Time		150		200		250		300	ns
t <sub>AA</sub>	Address Access Time		150		200		250		300	ns
t <sub>OE</sub>	Output Enable Access Time		50		70		100		150	ns
t <sub>LZ</sub> <sup>(3)</sup>	Chip Enable to Output in Low Z	0		0		0		0		ns
t <sub>OLZ</sub> <sup>(3)</sup>	Output Enable to Output in Low Z	0		0		0		0		ns
t <sub>HZ</sub> <sup>(3)</sup>	Chip Disable to Output in High Z		80		100		100		100	ns
t <sub>OHZ</sub> <sup>(3)</sup>	Output Disable to Output in High Z		80		100		100		100	ns
t <sub>OH</sub>	Output Hold From Address Change	0		0		0		0		ns

3825 PGM T10

### Read Cycle



3825 FHD F05

**Note:** (3) t<sub>LZ</sub> min., t<sub>HZ</sub>, t<sub>OLZ</sub> min., and t<sub>OHZ</sub> are periodically sampled and not 100% tested. t<sub>HZ</sub> max. and t<sub>OHZ</sub> max. are measured, with C<sub>L</sub> = 5pF from the point when CE or OE return high (whichever occurs first) to the time when the outputs are no longer driven.

# X20C04

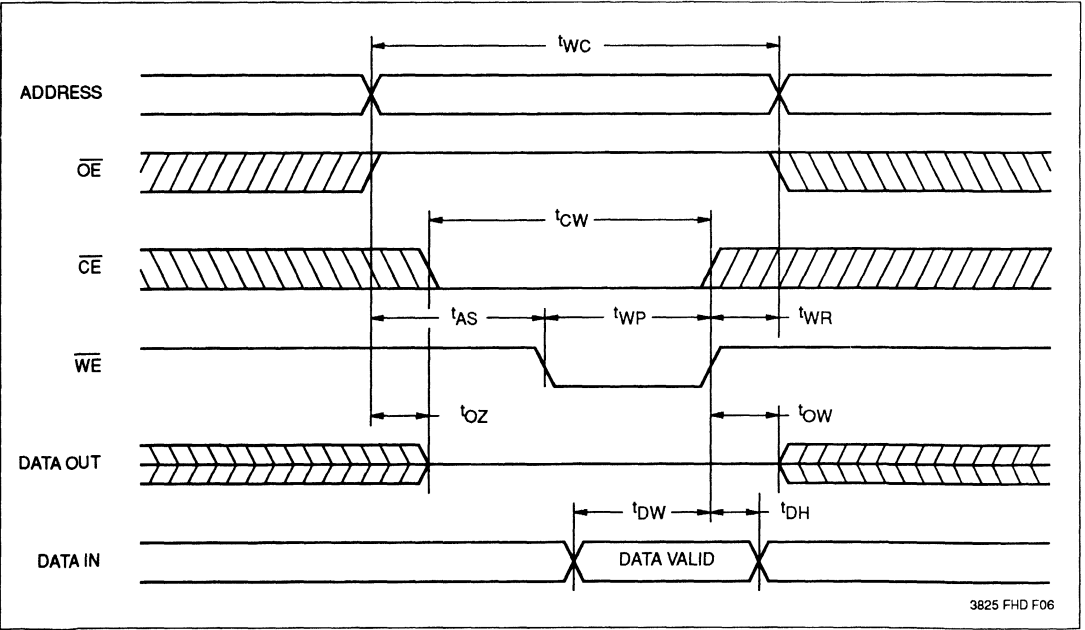
## Write Cycle Limits

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{WC}$	Write Cycle Time	150		200		250		300		ns
$t_{CW}$	Chip Enable to End of Write Input	150		200		250		300		ns
$t_{AS}$	Address Setup Time	0		0		0		0		ns
$t_{WP}$	Write Pulse Width	100		120		150		200		ns
$t_{WR}$	Write Recovery Time	0		0		0		0		ns
$t_{DW}$	Data Setup to End of Write	100		120		150		200		ns
$t_{DH}$	Data Hold Time	0		0		0		0		ns
$t_{WZ}^{(4)}$	Write Enable to Output in High Z		80		100		100		100	ns
$t_{OW}^{(4)}$	Output Active from End of Write	5		5		5		5		ns
$t_{OZ}^{(4)}$	Output Enable to Output in High Z		80		100		100		100	ns

3825 PGM T11

1

## WE Controlled Write Cycle

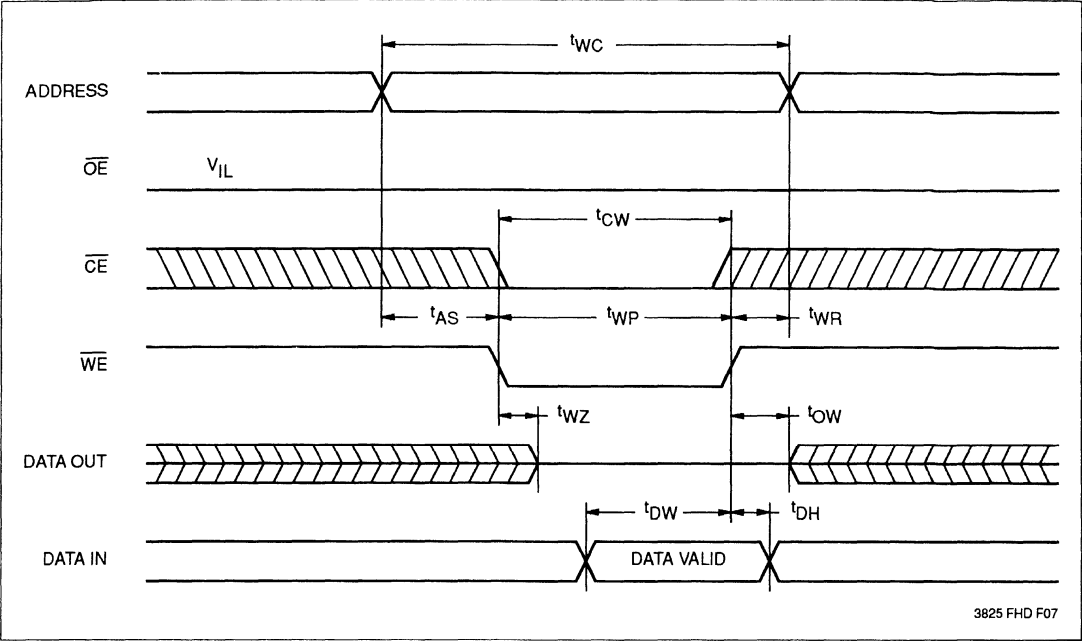


3825 FHD F06

**Note:** (4)  $t_{WZ}$ ,  $t_{OW}$ , and  $t_{OZ}$  are periodically sampled and not 100% tested.

**X20C04**

**$\overline{\text{CE}}$  Controlled Write Cycle**



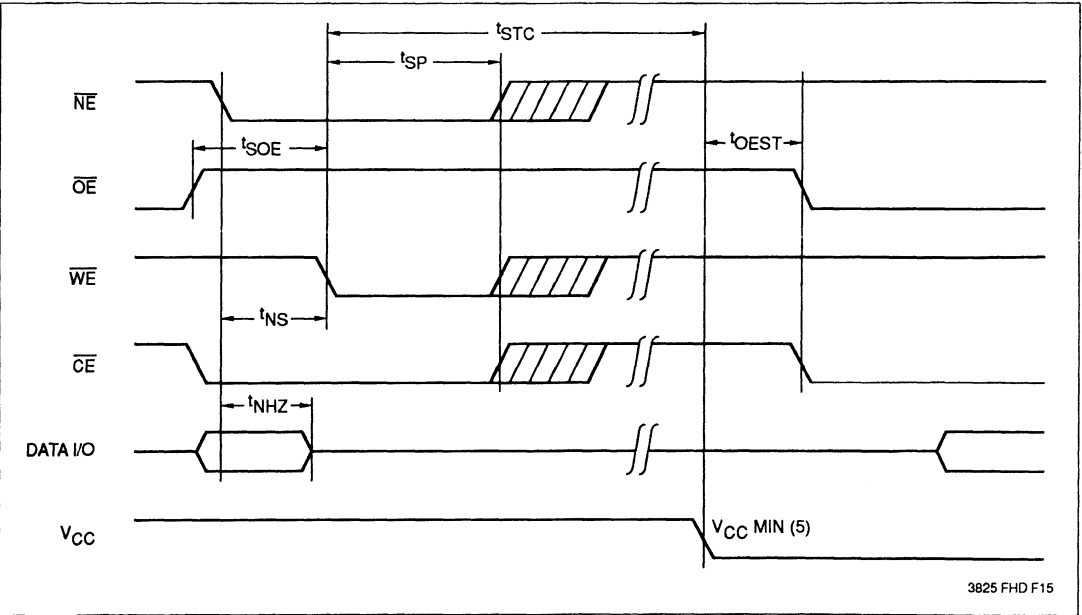
# X20C04

## STORE CYCLE LIMITS

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{STC}$	Store Cycle Time		5		5		5		5	ms
$t_{SP}$	Store Pulse Width	100		120		150		200		ns
$t_{NHZ}$	Nonvolatile Enable to Output in High Z		80		100		100		100	ns
$t_{OEST}$	Output Enable From End of Store	10		10		10		10		ns
$t_{SOE}$	OE Disable to Store Function	20		20		20		20		ns
$t_{NS}$	NE Setup Time from WE	0		0		0		0		ns

3825 PGM T09

## Store Timing



3825 FHD F15

**Note:** (5) X20C04  $V_{CC}$  Min. = 4.5V

The Store Pulse Width ( $t_{SP}$ ) is a minimum time that  $\overline{NE}$ ,  $\overline{WE}$  and  $\overline{CE}$  must be LOW simultaneously. To insure data integrity,  $\overline{NE}$  and  $\overline{CE}$  must return HIGH after

initiation of and throughout the duration ( $t_{STC}$ ) of the Store operation. During  $t_{STC}$ ,  $\overline{OE}$  and  $\overline{WE}$  may go LOW providing the host system access to other devices in the system.

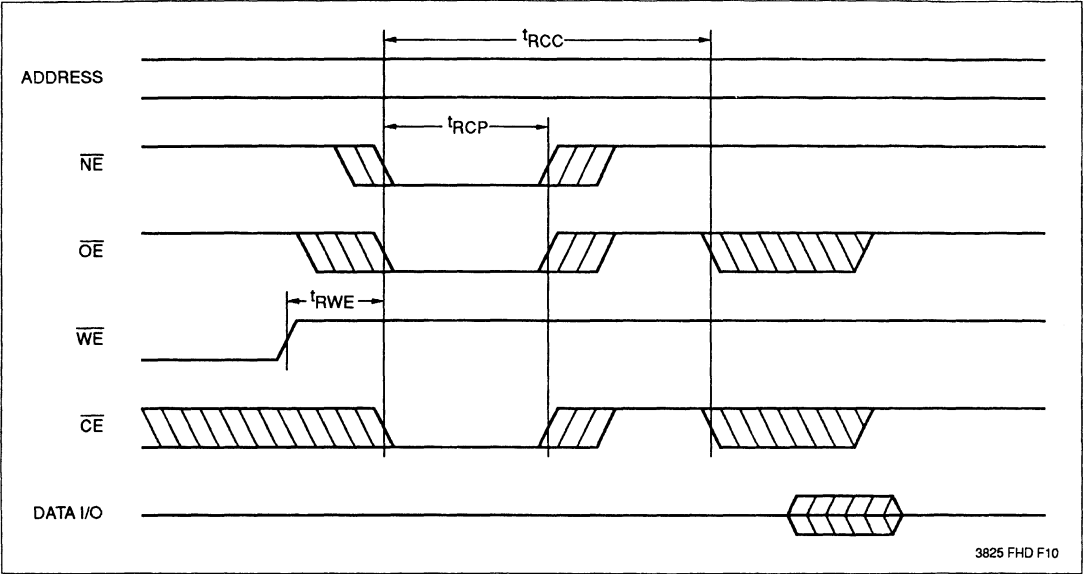
# X20C04

## ARRAY RECALL CYCLE LIMITS

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RCC}$	Array Recall Cycle Time		5		5		5		5	$\mu s$
$t_{RCP}^{(6)}$	Recall Pulse Width to Initiate Recall	80		120		150		200		ns
$t_{RWE}$	$\overline{WE}$ Setup Time to $\overline{NE}$	0		0		0		0		ns

## Array Recall Cycle

3825 PGM T13



3825 FHD F10

**Note:** (6) The Recall Pulse Width ( $t_{RCP}$ ) is a minimum time that  $\overline{NE}$ ,  $\overline{OE}$  and  $\overline{CE}$  must be LOW simultaneously. To insure data integrity,  $\overline{NE}$  and  $\overline{CE}$  must return HIGH after initiation of and through the duration ( $t_{RCC}$ ) of the Recall operation. During  $t_{RCC}$ ,  $\overline{OE}$  and  $\overline{WE}$  may go LOW providing the host access to other devices in the system.



## Advance Information

4K

X20C05

512 x 8

### High Speed AUTOSTORE™ NOVRAM

#### FEATURES

- Fast Access Time: 35ns, 45ns, 55ns
- High Reliability
  - Endurance: 1,000,000 Store Operations
  - Retention: 100 Years Minimum
- Power-on Recall
  - E<sup>2</sup>PROM Data Automatically Recalled Into SRAM Upon Power-up
- AUTOSTORE™ NOVRAM
  - User Enabled Option
  - Automatically Stores SRAM Data Into the E<sup>2</sup>PROM Array When V<sub>CC</sub> Low Threshold Is Detected
  - Open Drain AUTOSTORE Status Output Pin
- Software Data Protection
  - Locks Out Inadvertent Store Operations
- Low Power CMOS
  - Standby: 250μA
- Infinite E<sup>2</sup>PROM Array Recall, and RAM Read and Write Cycles
- Upward compatible with X20C16 (16K)

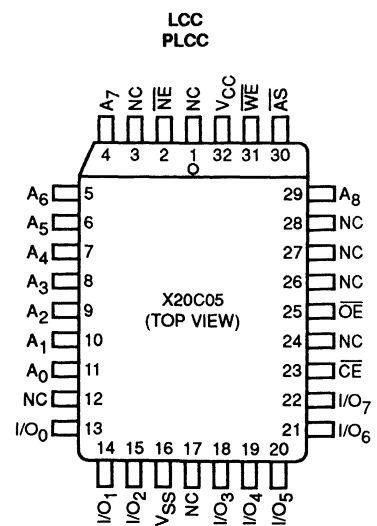
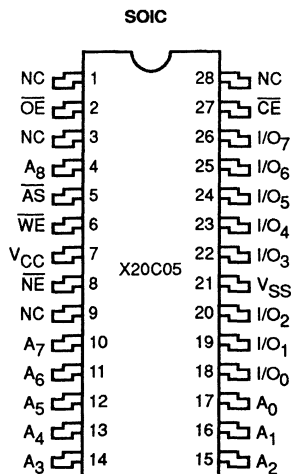
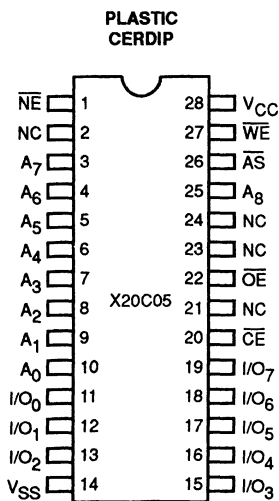
#### DESCRIPTION

The Xicor X20C05 is a 512 x 8 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a non-volatile electrically erasable PROM (E<sup>2</sup>PROM). The X20C05 is fabricated with advanced CMOS floating gate technology to achieve high speed with low power and wide power-supply margin. The X20C05 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, EPROMs and E<sup>2</sup>PROMs.

The NOVRAM design allows data to be easily transferred from RAM to E<sup>2</sup>PROM (store) and E<sup>2</sup>PROM to RAM (recall). The store operation is completed in 5 ms or less and the recall operation is completed in 5 μs or less.

Xicor NOVRAMS are designed for unlimited write operations to RAM, either from the host or recalls from E<sup>2</sup>PROM, and a minimum 1,000,000 store operations to the E<sup>2</sup>PROM. Data retention is specified to be greater than 100 years.

#### PIN CONFIGURATION



AUTOSTORE™ NOVRAM is a trademark of Xicor, Inc.

©Xicor, 1991 Patents Pending



X20C05

PIN DESCRIPTIONS

Addresses (A<sub>0</sub>–A<sub>8</sub>)

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ( $\overline{CE}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH, power consumption is reduced.

Output Enable ( $\overline{OE}$ )

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of  $\overline{CE}$ ,  $\overline{WE}$  or  $\overline{NE}$ .

Data In/Data Out (I/O<sub>0</sub>–I/O<sub>7</sub>)

Data is written to or read from the X20C05 through the I/O pins. The I/O pins are placed in the high impedance state when either  $\overline{CE}$  or  $\overline{OE}$  is HIGH or when  $\overline{NE}$  is LOW.

Write Enable ( $\overline{WE}$ )

The Write Enable input controls the writing of data to the static RAM.

Nonvolatile Enable ( $\overline{NE}$ )

The Nonvolatile Enable input controls the recall function to the E<sup>2</sup>PROM array.

AUTOSTORE Output ( $\overline{AS}$ )

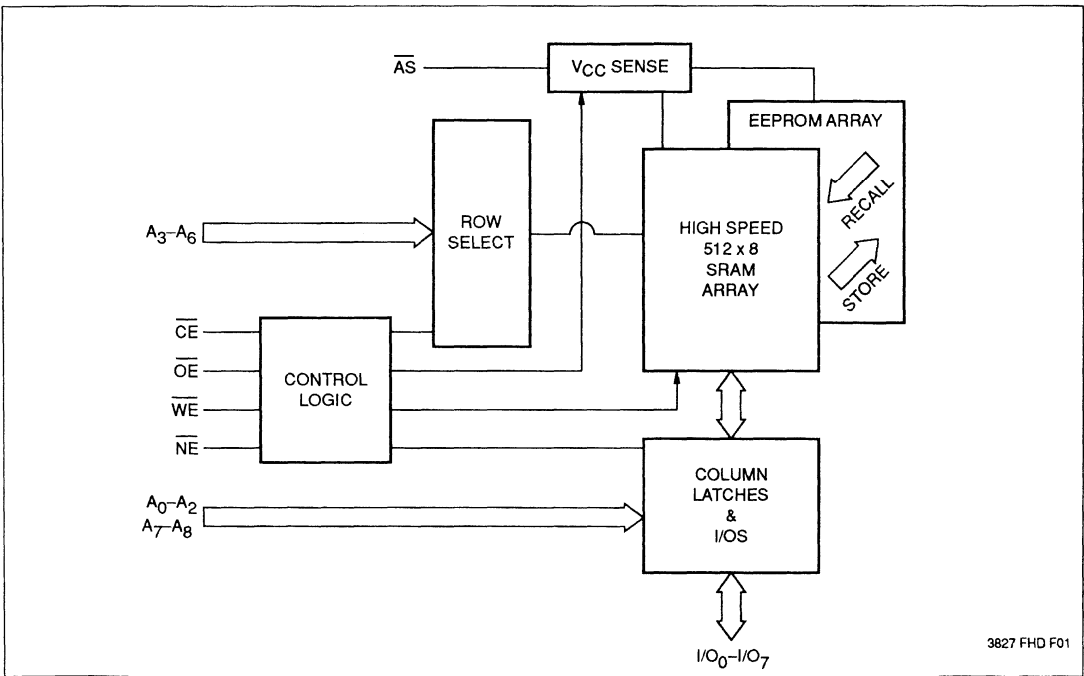
$\overline{AS}$  is an open drain output which, when asserted indicates  $V_{CC}$  has fallen below the AUTOSTORE threshold ( $V_{ASTH}$ ).  $\overline{AS}$  may be wire-ORed with multiple open drain outputs and used as an interrupt input to a microcontroller or as an input to a low power reset circuit.

PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>8</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{NE}$	Nonvolatile Enable
$\overline{AS}$	AUTOSTORE Output
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

3827 PGM T01

FUNCTIONAL DIAGRAM



3827 FHD F01

# X20C05

## DEVICE OPERATION

The  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{WE}$  and  $\overline{NE}$  inputs control the X20C05 operation. The X20C05 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH, or when  $\overline{NE}$  is LOW.

## RAM Operations

RAM read and write operations are performed as they would be with any static RAM. A read operation requires  $\overline{CE}$  and  $\overline{OE}$  to be LOW with  $\overline{WE}$  and  $\overline{NE}$  HIGH. A write operation requires  $\overline{CE}$  and  $\overline{WE}$  to be LOW with  $\overline{NE}$  HIGH. There is no limit to the number of read or write operations performed to the RAM portion of the X20C05.

## MEMORY TRANSFER OPERATIONS

There are two memory transfer operations: a recall operation whereby the data stored in the E<sup>2</sup>PROM array is transferred to the SRAM array; and a store operation which causes the entire contents of the SRAM array to be stored in the E<sup>2</sup>PROM array.

Recall operations are performed automatically upon power-up and under host system control when  $\overline{NE}$ ,  $\overline{OE}$  and  $\overline{CE}$  are LOW and  $\overline{WE}$  is HIGH. The recall operation takes a maximum of 5 $\mu$ s.

There are two methods of initiating a store operation. The first is the software store command. This command takes the place of the hardware store employed on the X20C04. This command is issued by entering into the special command mode:  $\overline{NE}$ ,  $\overline{CE}$  and  $\overline{WE}$  strobe LOW while at the same time a specific address and data combination is sent to the device. This is a three step

operation: the first address/data combination is 555[H]/AA[H]; the second combination is 2AA[H]/55[H]; and the final command combination is 555[H]/33[H]. This sequence of pseudo write operations will immediately initiate a store operation. Refer to the software command timing diagrams for details on set and hold times for the various signals.

The second method of storing data is through the AUTOSTORE command. When enabled, data is automatically stored from the RAM into the E<sup>2</sup>PROM array whenever  $V_{CC}$  falls below the preset AUTOSTORE threshold. This feature is enabled by performing the first two steps for the software store with the command combination being 555[H]/CC[H].

The AUTOSTORE feature is disabled by issuing the three step command sequence with the command combination being 555[H]/CD[H]. The AUTOSTORE feature will also be reset if  $V_{CC}$  falls below the power-on reset threshold (approximately 3.5V) and is then raised back into the operating range.






## DATA PROTECTION

The X20C16 supports two methods of protecting the nonvolatile data.

—If after power-up neither the software store nor AUTOSTORE feature are enabled, no store can occur.

—If after power-up no SRAM write operations have occurred no store operation can be initiated. The software store and AUTOSTORE commands will be ignored.

## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

# X20C05

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	–65°C to +135°C
Storage Temperature .....	–65°C to +150°C
Voltage on any Pin with Respect to Ground .....	–1.0V to +7V
D.C. Output Current .....	10mA

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3827 PGM T02

## \*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Supply Voltage	Limits
X20C05	5V ±10%

3827 PGM T03

## D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I <sub>CC1</sub>	V <sub>CC</sub> Current (Active)		100	mA	$\overline{NE} = \overline{WE} = V_{IH}$ , $\overline{CE} = \overline{OE} = V_{IL}$ Address Inputs = 0.4V/2.4V Levels @ f = 20MHz. All I/Os = Open
I <sub>CC2</sub>	V <sub>CC</sub> Current During Store		5	mA	All Inputs = V <sub>IH</sub>
I <sub>CC3</sub>	V <sub>CC</sub> Current During AUTOSTORE		2.5	mA	All I/Os = Open
I <sub>SB1</sub>	V <sub>CC</sub> Standby Current (TTL Input)		10	mA	$\overline{CE} = V_{IH}$ All Other Inputs = V <sub>IH</sub> , All I/Os = Open
I <sub>SB2</sub>	V <sub>CC</sub> Standby Current (CMOS Input)		250	μA	All Inputs = V <sub>CC</sub> – 0.3 All I/Os = Open
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , $\overline{CE} = V_{IH}$
V <sub>IL</sub> (1)	Input Low Voltage	–1.0	0.8	V	
V <sub>IH</sub> (1)	Input High Voltage	2.0	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 5mA
V <sub>OLAS</sub>	AUTOSTORE Output		0.4	V	I <sub>OLAS</sub> = 1mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = –4mA

3827 PGM T04

## POWER-UP TIMING

Symbol	Parameter	Max.	Units
t <sub>PUR</sub> (2)	Power-Up to RAM Operation	100	μs
t <sub>Puw</sub> (2)	Power-Up to Nonvolatile Operation	5	ms

3827 PGM T05

## CAPACITANCE T<sub>A</sub> = 25°C, F = 1.0MHz, V<sub>CC</sub> = 5V.

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (2)	Input/Output Capacitance	10	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (2)	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

3827 PGM T06

Notes: (1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.

# X20C05

## ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Changes/Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

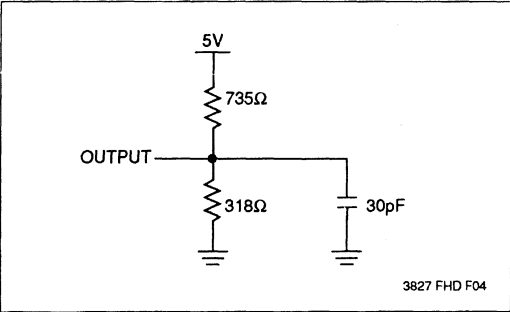
3827 PGM T07

## MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{NE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	H	L	Read RAM	Output Data	Active
L	L	H	X	Write "1" RAM	Input Data High	Active
L	L	H	X	Write "0" RAM	Input Data Low	Active
L	H	L	L	Array Recall	Output High Z	Active
L	L	L	H	Software Command	Input Data	Active
L	H	H	H	Output Disabled	Output High Z	Active
L	L	L	L	Not Allowed	Output High Z	Active
L	H	L	H	No Operation	Output High Z	Active

3827 PGM T09

## EQUIVALENT A.C. LOAD CIRCUIT



## A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	1.5V

3827 PGM T08

X20C05

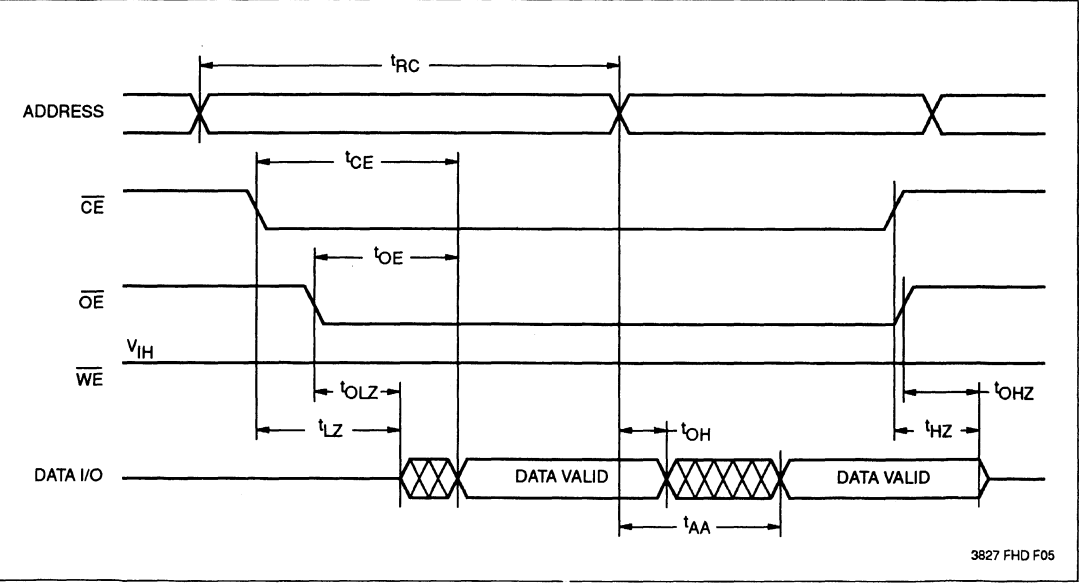
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	X20C05-35		X20C05-45		X20C05-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	35		45		55		ns
t <sub>CE</sub>	Chip Enable Access Time		35		45		55	ns
t <sub>AA</sub>	Address Access Time		35		45		55	ns
t <sub>OE</sub>	Output Enable Access Time		20		25		30	ns
t <sub>LZ</sub> <sup>(3)</sup>	Chip Enable to Output in Low Z	0		0		0		ns
t <sub>OLZ</sub> <sup>(3)</sup>	Output Enable to Output in Low Z	0		0		0		ns
t <sub>HZ</sub> <sup>(3)</sup>	Chip Disable to Output in High Z		15		20		25	ns
t <sub>OHZ</sub> <sup>(3)</sup>	Output Disable to Output in High Z		15		20		25	ns
t <sub>OH</sub>	Output Hold From Address Change	0		0		0		ns

3827 PGM T10

Read Cycle



3827 FHD F05

**Note:** (3)  $t_{LZ}$  min.,  $t_{HZ}$ ,  $t_{OLZ}$  min., and  $t_{OHZ}$  are periodically sampled and not 100% tested.  $t_{HZ}$  and  $t_{OHZ}$  are measured, with  $C_L = 5\text{pF}$ , from the point when  $\overline{CE}$  or  $\overline{OE}$  return high (whichever occurs first) to the time when the output is no longer driven.

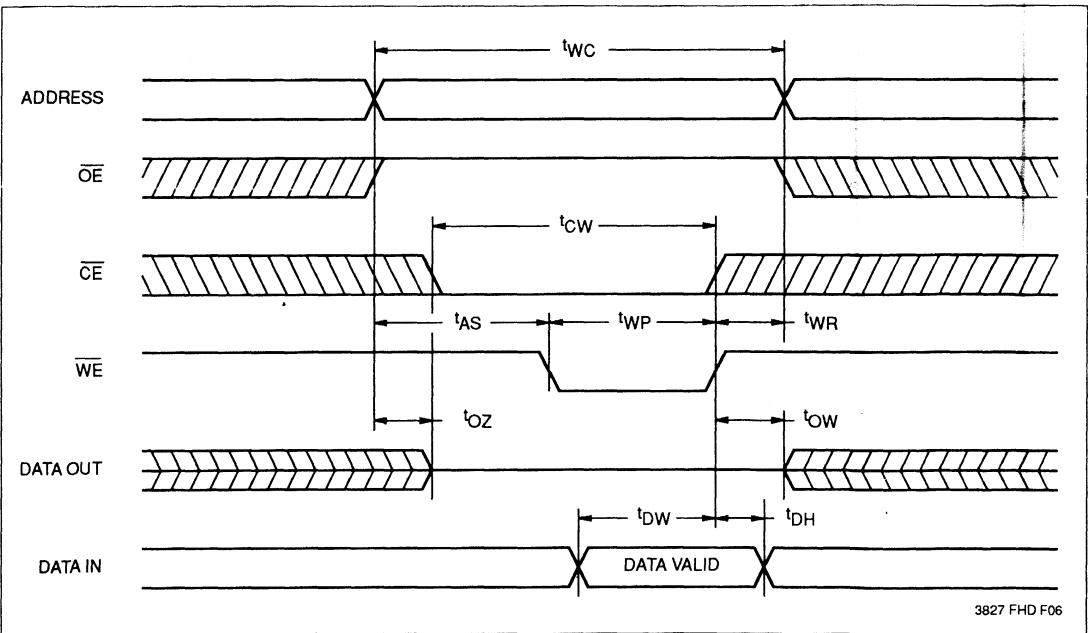
# X20C05

## Write Cycle Limits

Symbol	Parameter	X20C05-35		X20C05-45		X20C05-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{WC}$	Write Cycle Time	35		45		55		ns
$t_{CW}$	Chip Enable to End of Write Input	30		35		40		ns
$t_{AS}$	Address Setup Time	0		0		0		ns
$t_{WP}$	Write Pulse Width	30		35		40		ns
$t_{WR}$	Write Recovery Time	0		0		0		ns
$t_{DW}$	Data Setup to End of Write	15		20		25		ns
$t_{DH}$	Data Hold Time	0		3		3		ns
$t_{WZ}^{(4)}$	Write Enable to Output in High Z		15		20		25	ns
$t_{OW}^{(4)}$	Output Active from End of Write	5		5		5		ns
$t_{OZ}^{(4)}$	Output Enable to Output in High Z		15		20		25	ns

3827 PGM T11

## WE Controlled Write Cycle

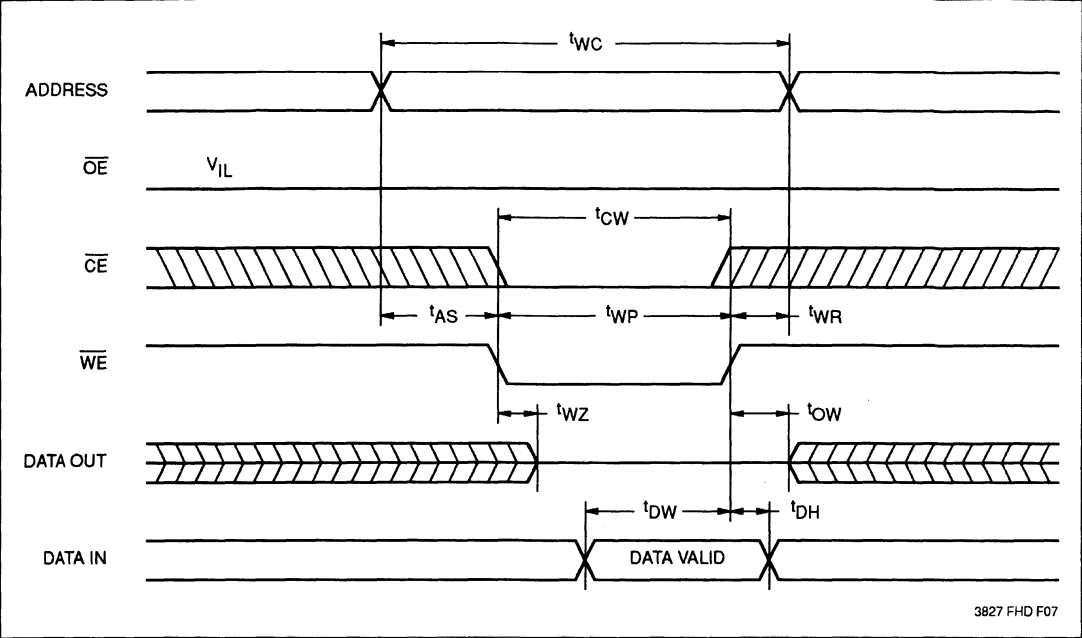


3827 FHD F06

**Note:** (4)  $t_{WZ}$ ,  $t_{OW}$  and  $t_{OZ}$  are periodically sampled and not 100% tested.

**X20C05**

**$\overline{\text{CE}}$  Controlled Write Cycle**



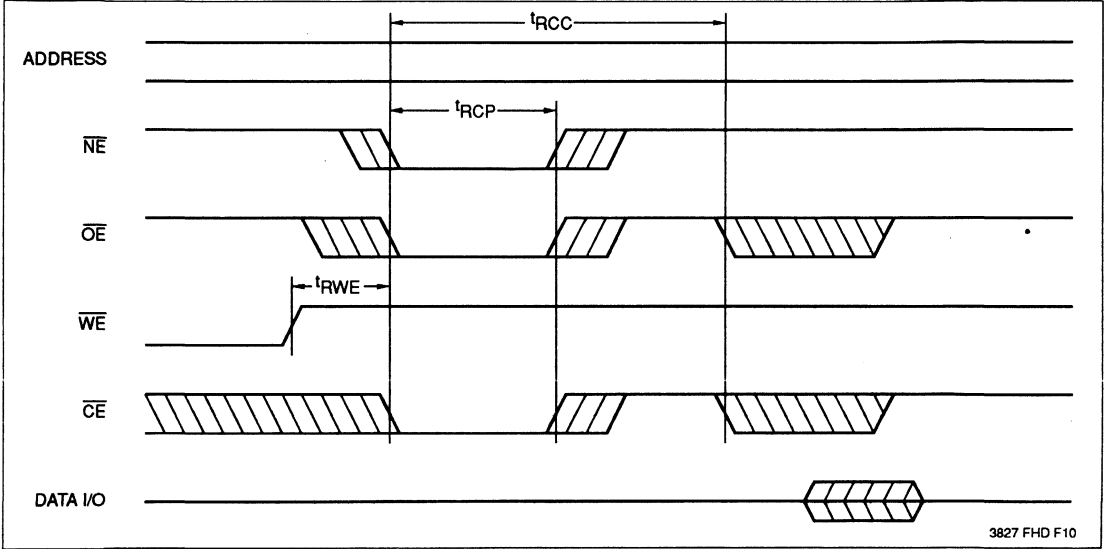
X20C05

Array Recall Cycle Limits

Symbol	Parameter	X20C05-35		X20C05-45		X20C05-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RCC}$	Array Recall Cycle Time		5		5		5	$\mu s$
$t_{RCP}^{(7)}$	Recall Pulse Width to Initiate Recall	30		40		50		ns
$t_{RWE}$	WE Setup Time to $\overline{NE}$	0		0		0		ns

3827 PGM T13

Array Recall Cycle



3827 FHD F10

**Note:** (7) The Recall Pulse Width ( $t_{RCP}$ ) is a minimum time that  $\overline{NE}$ ,  $\overline{OE}$  and  $\overline{CE}$  must be LOW simultaneously. To insure data integrity,  $\overline{NE}$  and  $\overline{CE}$  must remain HIGH after initiation of and through the duration ( $t_{RCC}$ ) of the Recall operation. During  $t_{RCC}$ ,  $\overline{OE}$  and  $\overline{WE}$  may go LOW providing the host access to other devices in the system.



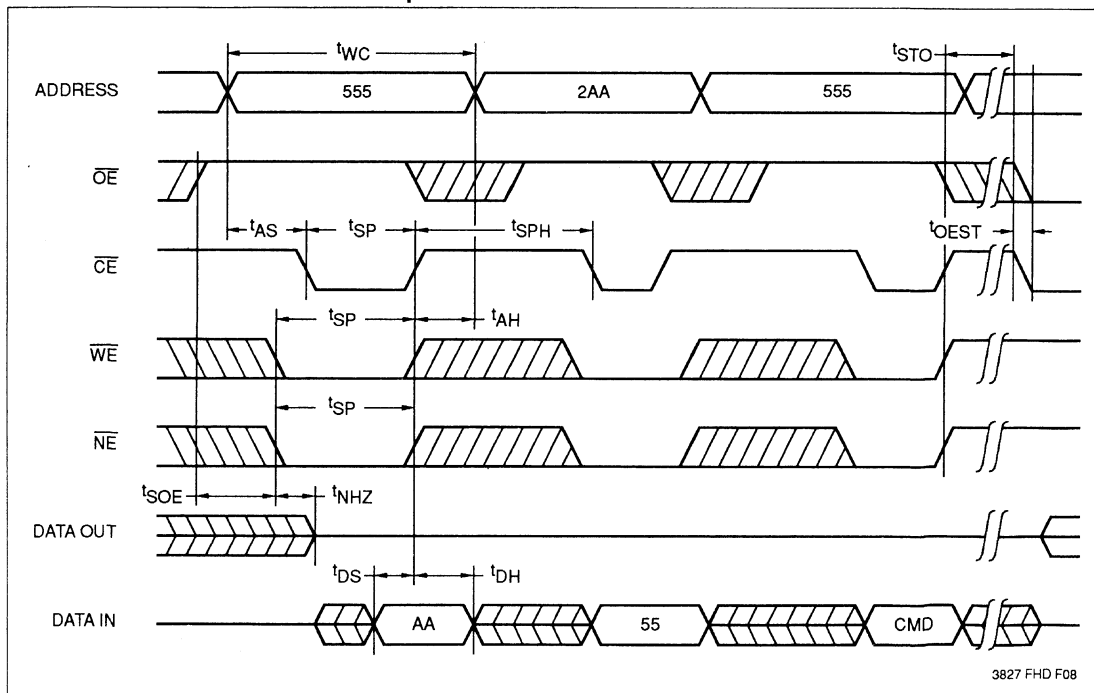
## X20C05

### Software Command Timing Limits

Symbol	Parameter	X20C05-35		X20C05-45		X20C05-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{STO}$	Store Cycle Time		5		5		5	ms
$t_{SP}^{(5)}$	Store Pulse Width	30		40		50		ns
$t_{SPH}$	Store Pulse Hold Time	35		45		55		ns
$t_{WC}$	Write Cycle Time	35		45		55		ns
$t_{AS}$	Address Setup Time	0		0		0		ns
$t_{AH}$	Address Hold time	0		0		0		ns
$t_{DS}$	Data Setup Time	15		20		25		ns
$t_{DH}$	Data Hold Time	0		3		3		ns
$t_{SOE}^{(6)}$	OE Disable to Store Function	20		20		20		ns
$t_{OEST}^{(6)}$	Output Enable from End of Store	10		10		10		ns
$t_{NHZ}^{(6)}$	Nonvolatile Enable to Output in High Z		15		20		25	ns

3827 PGM T12

### CE Controlled Software Command Sequence



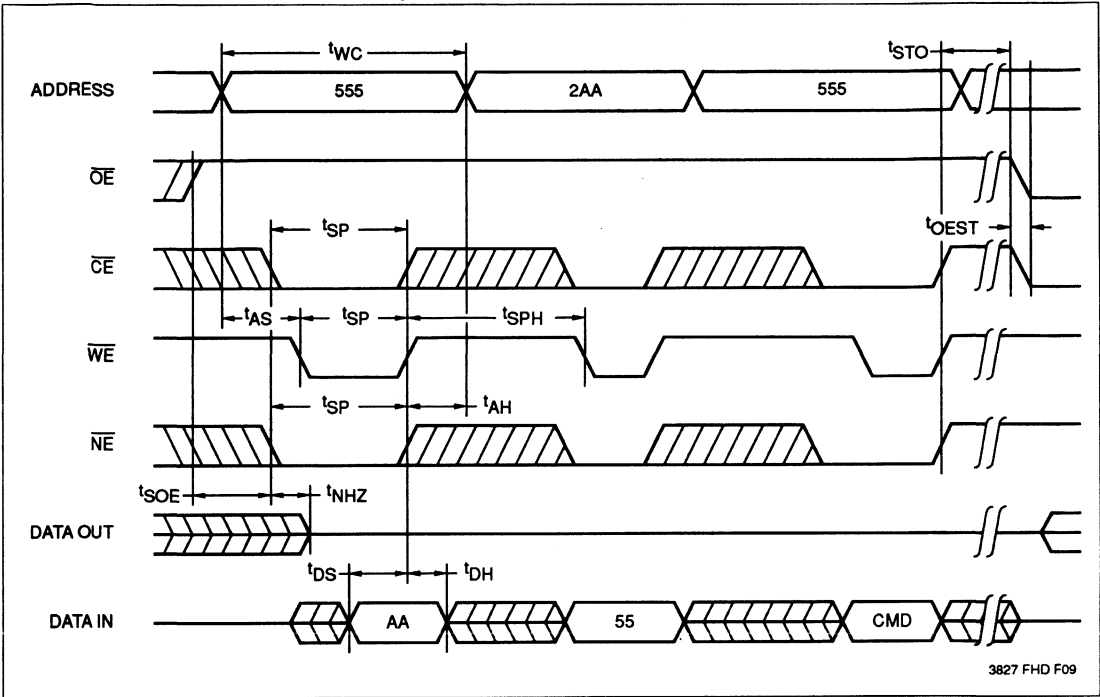
3827 FHD F08

**Notes:** (5) The Store Pulse Width ( $t_{SP}$ ) is a minimum time that  $\overline{NE}$ ,  $\overline{WE}$  and  $\overline{CE}$  must be LOW simultaneously. To insure data integrity,  $\overline{NE}$  and  $\overline{CE}$  must remain HIGH after initiation of and throughout the duration ( $t_{STO}$ ) of the Store operation. During  $t_{STO}$ ,  $\overline{OE}$  and  $\overline{WE}$  may go LOW providing the host system access to other devices in the system.

(6)  $t_{SOE}$ ,  $t_{OEST}$  and  $t_{NHZ}$  are periodically sampled and not 100% tested.

X20C05

WE Controlled Software Command Sequence



1

# X20C05

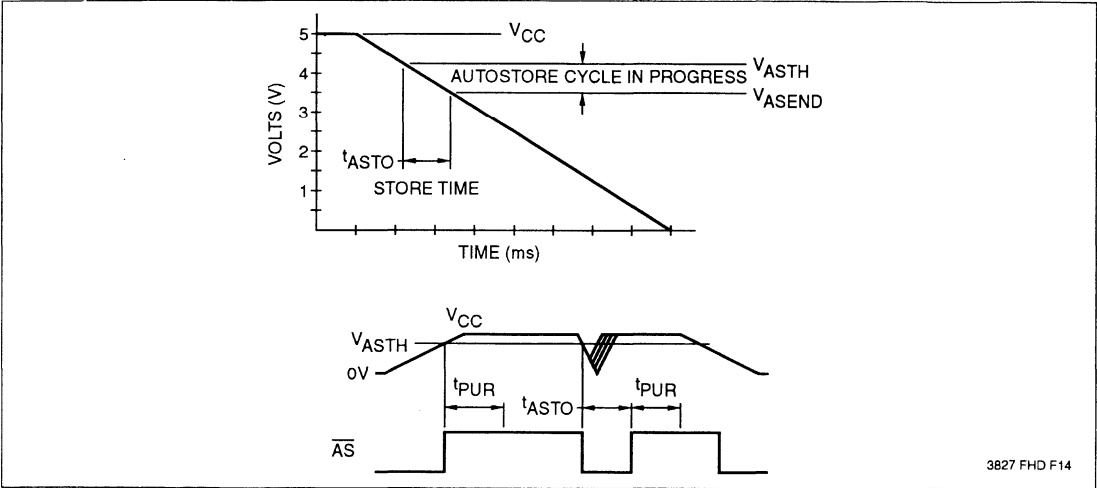
## AUTOSTORE Feature

The AUTOSTORE feature automatically saves the contents of the X20C05's Static RAM to the on-board bit-for-bit shadow E<sup>2</sup>PROM at power down. This circuitry insures that no data is lost during accidental power downs or general system crashes, and is ideal for microprocessor caching systems, embedded software systems, and general system back-up memory.

The AUTOSTORE instruction (EAS) to the SDP register sets the AUTOSTORE enable latch, allowing the X20C05

to automatically perform a store operation whenever  $V_{CC}$  falls below the AUTOSTORE threshold ( $V_{ASTH}$ ).  $V_{CC}$  must remain above the AUTOSTORE Cycle End Voltage ( $V_{ASEND}$ ) for the duration of the store cycle ( $t_{ASTO}$ ). The detailed timing for this feature is illustrated in the AUTOSTORE timing diagram, below. Once the AUTOSTORE cycle is initiated, all other device functions are inhibited.

## AUTOSTORE CYCLE Timing Diagrams

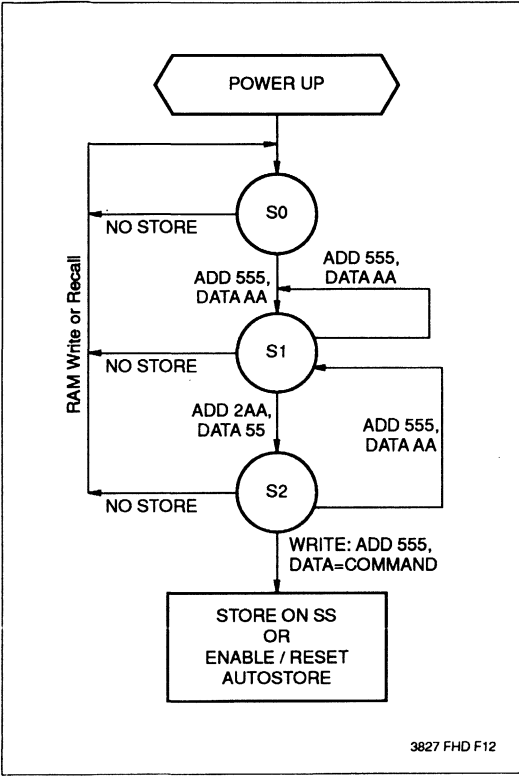


## AUTOSTORE CYCLE LIMITS

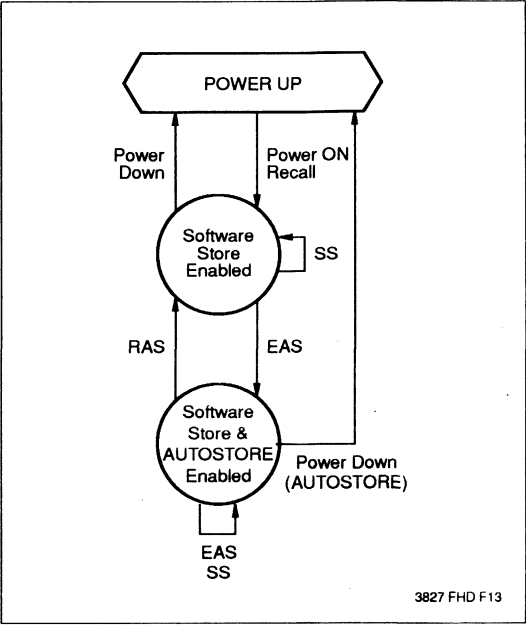
Symbol	Parameter	X20C05		Units
		Min.	Max.	
$t_{ASTO}$	AUTOSTORE Cycle Time		2.5	ms
$V_{ASTH}$	AUTOSTORE Threshold Voltage	4.0	4.3	V
$V_{ASEND}$	AUTOSTORE Cycle End Voltage	3.5		V

3827 PGM T15

SDP (Software Data Protection)



Store State Diagram



1

SOFTWARE DATA PROTECTION COMMANDS

Command		Data [Hex]
EAS	Enable AUTOSTORE	CC
RAS	Reset AUTOSTORE	CD
SS	Software Store	33

3827 PGM T14

**X20C05**

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**NOTES**



## Advance Information

16K

X20C16

2K x 8 Bit

## High Speed AUTOSTORE™ NOVRAM

### FEATURES

- **Fast Access Time:** 35ns, 45ns, 55ns
- **High Reliability**
  - **Endurance:** 1,000,000 Store Operations
  - **Retention:** 100 Years Minimum
- **AUTOSTORE™ NOVRAM**
  - **Automatically Stores SRAM Data Into the E<sup>2</sup>PROM Array When V<sub>CC</sub> Low Threshold Is Detected**
  - **User Enabled Option**
  - **Open Drain AUTOSTORE Status Output Pin**
- **Power-on Recall**
  - **E<sup>2</sup>PROM Data Automatically Recalled Into SRAM Upon Power-up**
- **Software Data Protection**
  - **Locks Out Inadvertent Store Operations**
- **Low Power CMOS**
  - **Standby: 250μA**
- **Infinite E<sup>2</sup>PROM Array Recall, and RAM Read and Write Cycles**

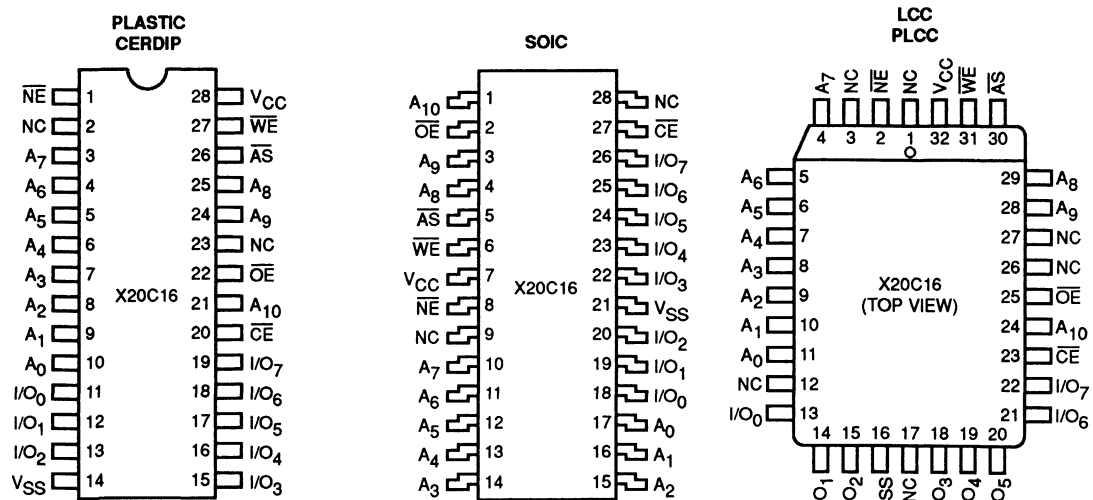
### DESCRIPTION

The Xicor X20C16 is a 2K x 8 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E<sup>2</sup>PROM) and the AUTOSTORE feature which automatically saves the RAM contents to E<sup>2</sup>PROM at power-down. The X20C16 is fabricated with advanced CMOS floating gate technology to achieve high speed with low power and wide power-supply margin. The X20C16 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, EPROMs and E<sup>2</sup>PROMs.

The NOVRAM design allows data to be easily transferred from RAM to E<sup>2</sup>PROM (store) and E<sup>2</sup>PROM to RAM (recall). The store operation is completed in 5 ms or less and the recall operation is completed in 10 μs or less. An automatic array recall operation reloads the contents of the E<sup>2</sup>PROM into RAM upon power-up.

Xicor NOVRAMS are designed for unlimited write operations to RAM, either from the host or recalls from E<sup>2</sup>PROM, and a minimum 1,000,000 store operations to the E<sup>2</sup>PROM. Data retention is specified to be greater than 100 years.

### PIN CONFIGURATION



3826 FHD F02

3826 FHD F15

3826 FHD F03

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# X20C16

## PIN DESCRIPTIONS

### Addresses ( $A_0$ – $A_{10}$ )

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{CE}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH, power consumption is reduced.

### Output Enable ( $\overline{OE}$ )

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of  $\overline{CE}$ ,  $\overline{WE}$  or  $\overline{NE}$ .

### Data In/Data Out ( $I/O_0$ – $I/O_7$ )

Data is written to or read from the X20C16 through the I/O pins. The I/O pins are placed in the high impedance state when either  $\overline{CE}$  or  $\overline{OE}$  is HIGH or when  $\overline{NE}$  is LOW.

### Write Enable ( $\overline{WE}$ )

The Write Enable input controls the writing of data to the static RAM.

### Nonvolatile Enable ( $\overline{NE}$ )

The Nonvolatile Enable input controls the recall function to the E<sup>2</sup>PROM array.

### AUTOSTORE Output ( $\overline{AS}$ )

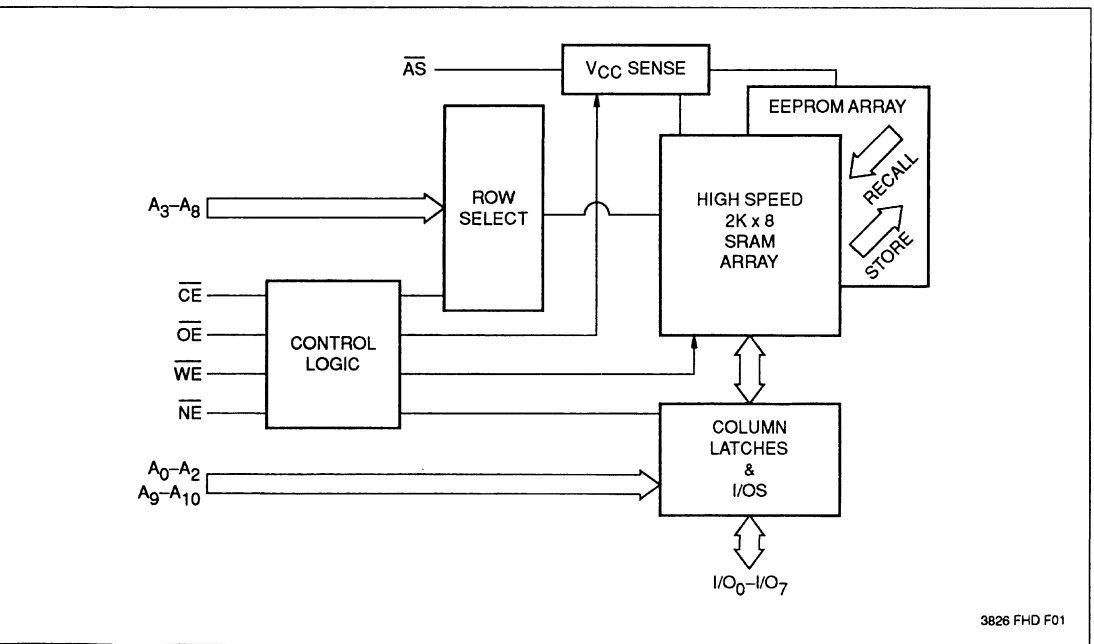
$\overline{AS}$  is an open drain output which, when asserted indicates  $V_{CC}$  has fallen below the AUTOSTORE threshold ( $V_{ASTH}$ ).  $\overline{AS}$  may be wire-ORed with multiple open drain outputs and used as an interrupt input to a microcontroller or as an input to a low power reset circuit.

## PIN NAMES

Symbol	Description
$A_0$ – $A_{10}$	Address Inputs
$I/O_0$ – $I/O_7$	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{NE}$	Nonvolatile Enable
$\overline{AS}$	AUTOSTORE Output
$V_{CC}$	+5V
$V_{SS}$	Ground
NC	No Connect

3826 PGM T01

## FUNCTIONAL DIAGRAM



3826 FHD F01

# X20C16

## DEVICE OPERATION

The  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{WE}$  and  $\overline{NE}$  inputs control the X20C16 operation. The X20C16 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH, or when  $\overline{NE}$  is LOW.

## RAM Operations

RAM read and write operations are performed as they would be with any static RAM. A read operation requires  $\overline{CE}$  and  $\overline{OE}$  to be LOW with  $\overline{WE}$  and  $\overline{NE}$  HIGH. A write operation requires  $\overline{CE}$  and  $\overline{WE}$  to be LOW with  $\overline{NE}$  HIGH. There is no limit to the number of read or write operations performed to the RAM portion of the X20C16.

## Memory Transfer Operations

There are two memory transfer operations: a recall operation whereby the data stored in the E<sup>2</sup>PROM array is transferred to the SRAM array; and a store operation which causes the entire contents of the SRAM array to be stored in the E<sup>2</sup>PROM array.

Recall operations are performed automatically upon power-up and under host system control when  $\overline{NE}$ ,  $\overline{OE}$  and  $\overline{CE}$  are LOW and  $\overline{WE}$  is HIGH. The recall operation takes a maximum of 5 $\mu$ s.

There are two methods of initiating a store operation. The first is the software store command. This command takes the place of the hardware store employed on the X20C04. This command is issued by entering into the special command mode:  $\overline{NE}$ ,  $\overline{CE}$  and  $\overline{WE}$  strobe LOW while at the same time a specific address and data combination is sent to the device. This is a three step operation: the first address/data combination is 555[H]/AA[H]; the second combination is 2AA[H]/55[H]; and the final command combination is 555[H]/33[H]. This sequence of pseudo write operations will immediately initiate a store operation. Refer to the software command timing diagrams for details on set and hold times for the various signals.

The second method of storing data is thru the autostore command. When enabled, data is automatically stored from the RAM into the E<sup>2</sup>PROM array whenever  $V_{CC}$  falls below the preset Autostore threshold. This feature

is enabled by performing the first two steps for the software store with the command combination being 555[H]/CC[H].

The AUTOSTORE feature is disabled by issuing the three step command sequence with the command combination being 555[H]/CD[H]. The Autostore feature will also be reset if  $V_{CC}$  falls below the power-on reset threshold (approximately 3.5V) and is then raised back into the operation range.






## Data Protection

The X20C16 supports two methods of protecting the nonvolatile data.

- If after power-up neither the software store nor the Autostore feature are enabled, no store can occur.
- If after power-up no SRAM write operations have occurred no store operation can be initiated. The software store and autostore commands will be ignored.

## SYMBOL TABLE

The following symbol table provides a key to understanding the conventions used in the device timing diagrams. The diagrams should be used in conjunction with the device timing specifications to determine actual device operation and performance, as well as device suitability for user's application.

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance



## X20C16

### ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	–65°C to +135°C
Storage Temperature .....	–65°C to +150°C
Voltage on any Pin with Respect to Ground .....	–1.0V to +7V
D.C. Output Current .....	10mA

### \*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any conditions other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3826 PGM T02

Supply Voltage	Limits
X20C16	5V ±10%

3826 PGM T03

### D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I <sub>CC1</sub>	V <sub>CC</sub> Current (Active)		100	mA	$\overline{NE} = \overline{WE} = V_{IH}$ , $\overline{CE} = \overline{OE} = V_{IL}$ Address Inputs = 0.4V/2.4V Levels @ f = 20MHz All I/Os = Open
I <sub>CC2</sub>	V <sub>CC</sub> Current During Store		5	mA	All Inputs = V <sub>IH</sub> All I/Os = Open
I <sub>CC3</sub>	V <sub>CC</sub> Current During AUTOSTORE		2.5	mA	
I <sub>SB1</sub>	V <sub>CC</sub> Standby Current (TTL Input)		10	mA	$\overline{CE} = V_{IH}$ All Other Inputs = V <sub>IH</sub> , All I/Os = Open
I <sub>SB2</sub>	V <sub>CC</sub> Standby Current (CMOS Input)		250	µA	All Inputs = V <sub>CC</sub> – 0.3 All I/Os = Open
I <sub>LI</sub>	Input Leakage Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , $\overline{CE} = V_{IH}$
V <sub>IL</sub> (1)	Input Low Voltage	–1.0	0.8	V	
V <sub>IH</sub> (1)	Input High Voltage	2.0	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 5mA
V <sub>OLAS</sub>	AUTOSTORE Output		0.4	V	I <sub>OLAS</sub> = 1mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = –4mA

3826 PGM T04

### POWER-UP TIMING

Symbol	Parameter	Max.	Units
t <sub>PUR</sub> (2)	Power-Up to RAM Operation	100	µs
t <sub>PWW</sub> (2)	Power-Up to Nonvolatile Operation	1	ms

3826 PGM T05

### CAPACITANCE T<sub>A</sub> = 25°C, F = 1.0MHZ, V<sub>CC</sub> = 5V.

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (2)	Input/Output Capacitance	10	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (2)	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

Notes: (1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.

3826 PGM T06

X20C16

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Changes/Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

3826 PGM T07

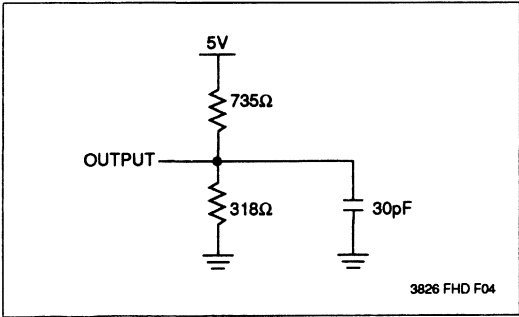
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MODE SELECTION

CE	WE	NE	OE	Mode	I/O	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	H	L	Read RAM	Output Data	Active
L	L	H	X	Write "1" RAM	Input Data High	Active
L	L	H	X	Write "0" RAM	Input Data Low	Active
L	H	L	L	Array Recall	Output High Z	Active
L	L	L	H	Software Command	Input Data	Active
L	H	H	H	Output Disabled	Output High Z	Active
L	L	L	L	Not Allowed	Output High Z	Active
L	H	L	H	No Operation	Output High Z	Active

3826 PGM T09

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	1.5V

3826 PGM T08

# X20C16

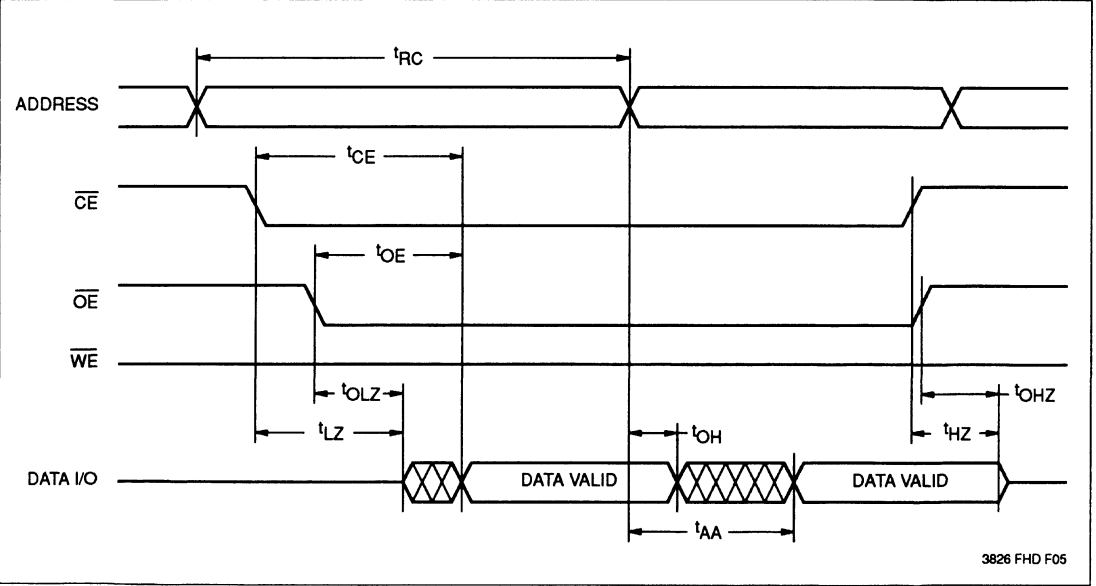
## A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

### Read Cycle Limits

Symbol	Parameter	X20C16-35		X20C16-45		X20C16-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	35		45		55		ns
$t_{CE}$	Chip Enable Access Time		35		45		55	ns
$t_{AA}$	Address Access Time		35		45		55	ns
$t_{OE}$	Output Enable Access Time		20		25		30	ns
$t_{LZ}^{(3)}$	Chip Enable to Output in Low Z	0		0		0		ns
$t_{OLZ}^{(3)}$	Output Enable to Output in Low Z	0		0		0		ns
$t_{HZ}^{(3)}$	Chip Disable to Output in High Z	0	15	0	20	0	25	ns
$t_{OHZ}^{(3)}$	Output Disable to Output in High Z	0	15	0	20	0	25	ns
$t_{OH}$	Output Hold From Address Change	0		0		0		ns

3826 PGM T10

### Read Cycle



3826 FHD F05

**Note:** (3)  $t_{LZ}$  min.,  $t_{HZ}$ ,  $t_{OLZ}$  min., and  $t_{OHZ}$  are periodically sampled and not 100% tested.  $t_{HZ}$  max. and  $t_{OHZ}$  max. are measured, with  $C_L = 5pF$ , from the point when  $\overline{CE}$  or  $\overline{OE}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

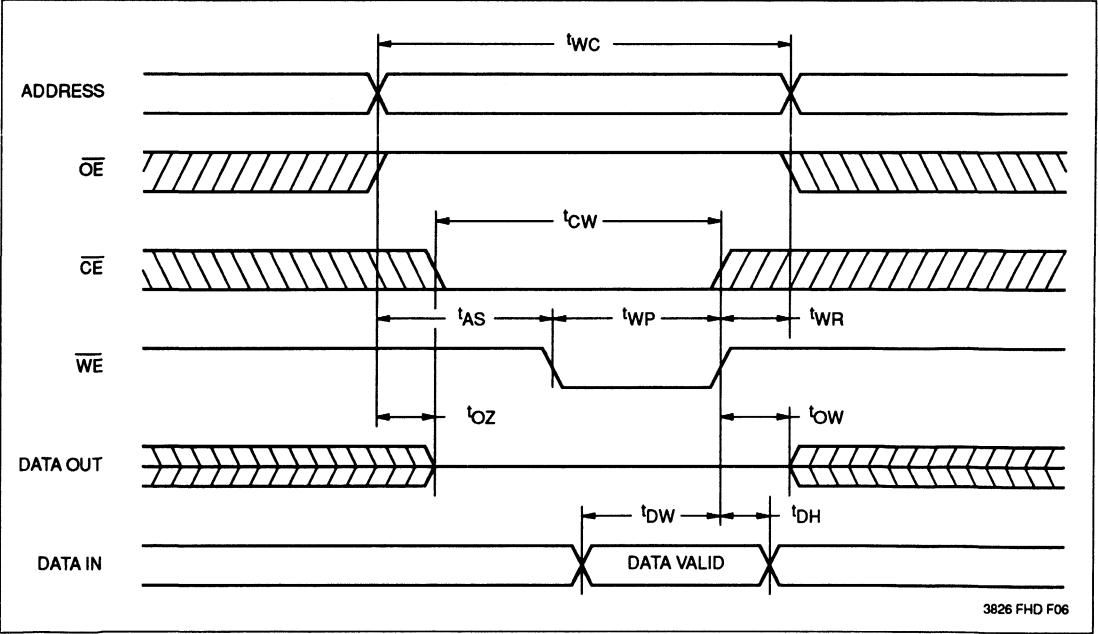
# X20C16

## Write Cycle Limits

Symbol	Parameter	X20C16-35		X20C16-45		X20C16-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	35		45		55		ns
t <sub>CW</sub>	Chip Enable to End of Write Input	30		35		40		ns
t <sub>AS</sub>	Address Setup Time	0		0		0		ns
t <sub>WP</sub>	Write Pulse Width	30		35		40		ns
t <sub>WR</sub>	Write Recovery Time	0		0		0		ns
t <sub>DW</sub>	Data Setup to End of Write	15		20		25		ns
t <sub>DH</sub>	Data Hold Time	0		3		3		ns
t <sub>WZ</sub> <sup>(4)</sup>	Write Enable to Output in High Z		15		20		25	ns
t <sub>OW</sub> <sup>(4)</sup>	Output Active from End of Write	5		5		5		ns
t <sub>OZ</sub> <sup>(4)</sup>	Output Enable to Output in High Z		15		20		25	ns

3826 PGM T11

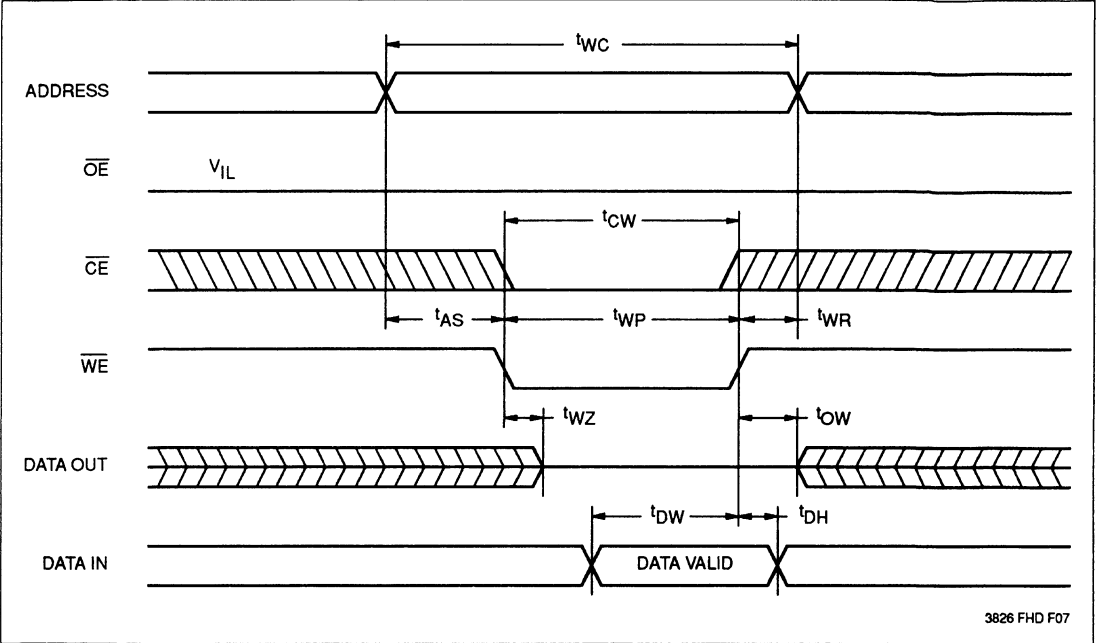
## WE Controlled Write Cycle



**Note:** (4) t<sub>WZ</sub>, t<sub>OW</sub>, t<sub>OZ</sub> are periodically sampled and not 100% tested.

# X20C16

## $\overline{\text{CE}}$ Controlled Write Cycle



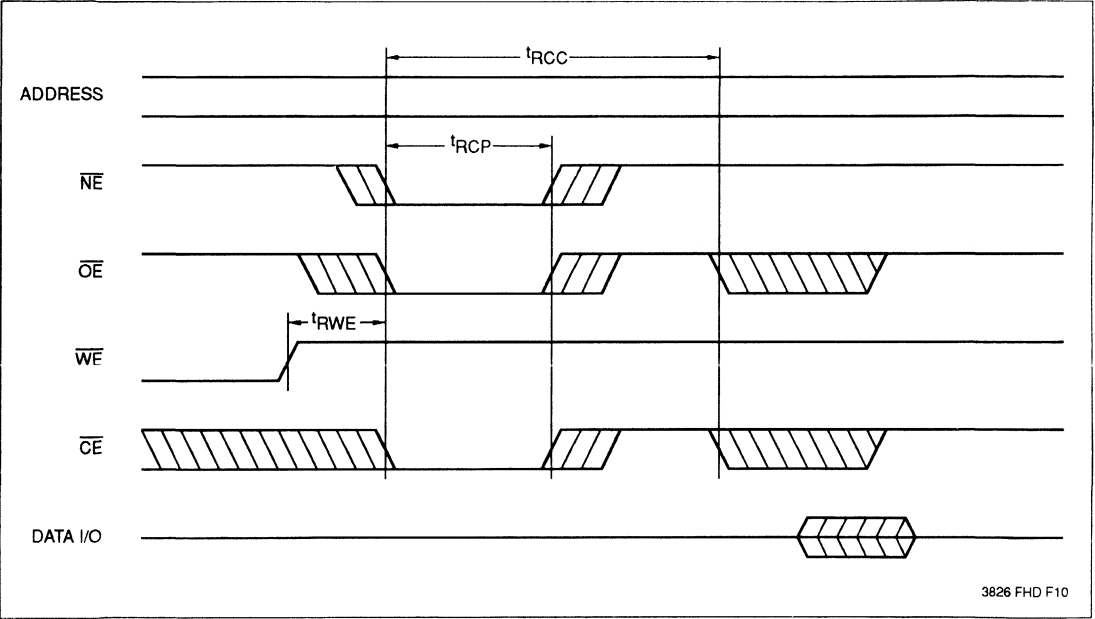
X20C16

ARRAY RECALL CYCLE LIMITS

Symbol	Parameter	X20C16-35		X20C16-45		X20C16-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RCC</sub>	Array Recall Cycle Time		10		10		10	μs
t <sub>RCP</sub> (7)	Recall Pulse Width to Initiate Recall	30		40		50		ns
t <sub>RWE</sub>	WE Setup Time to NE	0		0		0		ns

3826 PGM T13

Array Recall Cycle



3826 FHD F10

**Note:** (7) The Recall Pulse Width (t<sub>RCP</sub>) is a minimum time that  $\overline{NE}$ ,  $\overline{OE}$  and  $\overline{CE}$  must be LOW simultaneously. To insure data integrity,  $\overline{NE}$  and  $\overline{CE}$  must remain HIGH after initiation of and through the duration (t<sub>RCC</sub>) of the Recall operation. During t<sub>RCC</sub>,  $\overline{OE}$  and  $\overline{WE}$  may go LOW providing the host access to other devices in the system.

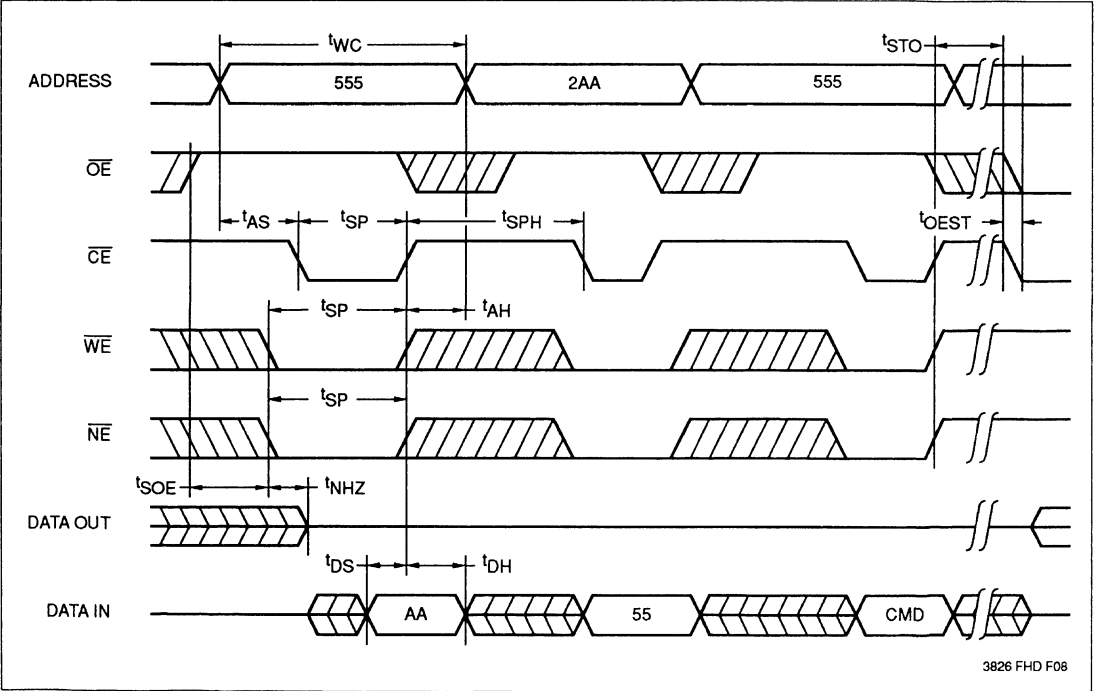
# X20C16

## Software Command Timing Limits

Symbol	Parameter	X20C16-35		X20C16-45		X20C16-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{STO}$	Store Cycle Time		5		5		5	ms
$t_{SP}^{(5)}$	Store Pulse Width	30		40		50		ns
$t_{SPH}$	Store Pulse Hold Time	35		45		55		ns
$t_{WC}$	Write Cycle Time	35		45		55		ns
$t_{AS}$	Address Setup Time	0		0		0		ns
$t_{AH}$	Address Hold time	0		0		0		ns
$t_{DS}$	Data Setup Time	15		20		25		ns
$t_{DH}$	Data Hold Time	0		3		3		ns
$t_{SOE}^{(6)}$	OE Disable to Store Function	20		20		20		ns
$t_{OEST}^{(6)}$	Output Enable from End of Store	10		10		10		ns
$t_{NHZ}^{(6)}$	Nonvolatile Enable to Output in High Z		15		20		25	ns

3826 PGM T12

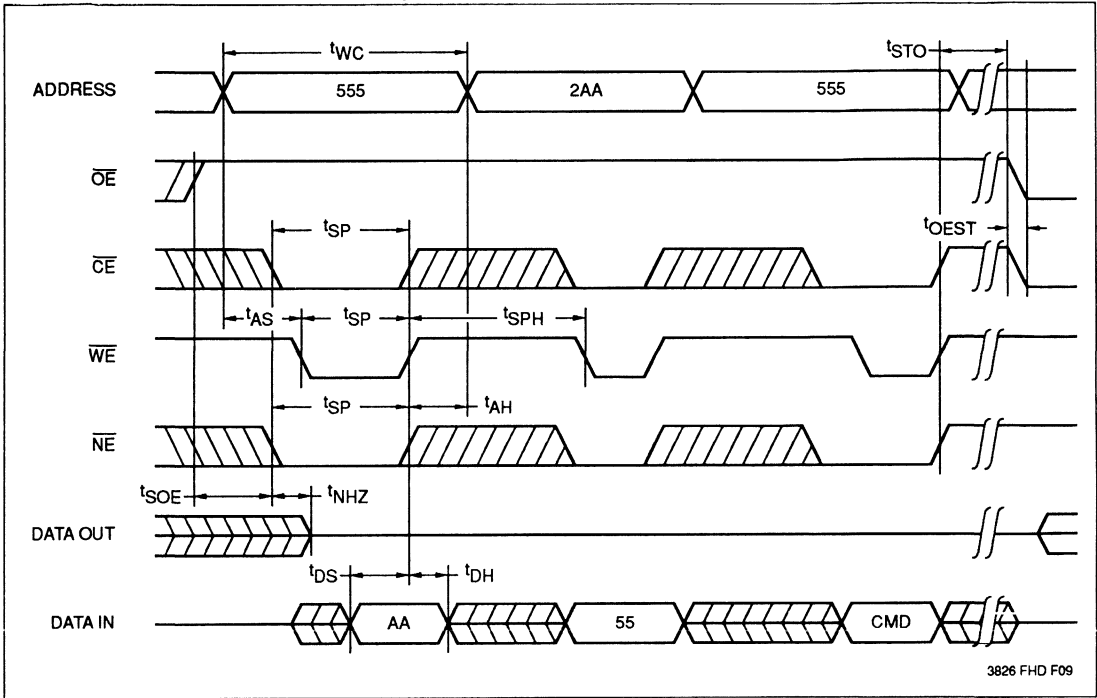
## $\overline{CE}$ Controlled Software Command Sequence



- Note:** (5) The Store Pulse Width ( $t_{SP}$ ) is a minimum time that  $\overline{NE}$ ,  $\overline{WE}$  and  $\overline{CE}$  must be LOW simultaneously. To insure data integrity,  $\overline{NE}$  and  $\overline{CE}$  must remain HIGH after initiation of and throughout the duration ( $t_{STO}$ ) of the Store operation. During  $t_{STO}$ ,  $\overline{OE}$  and  $\overline{WE}$  may go LOW providing the host system access to other devices in the system.
- (6)  $t_{SOE}$ ,  $t_{OEST}$  and  $t_{NHZ}$  are periodically sampled and not 100% tested.

X20C16

WE Controlled Software Command Sequence



1



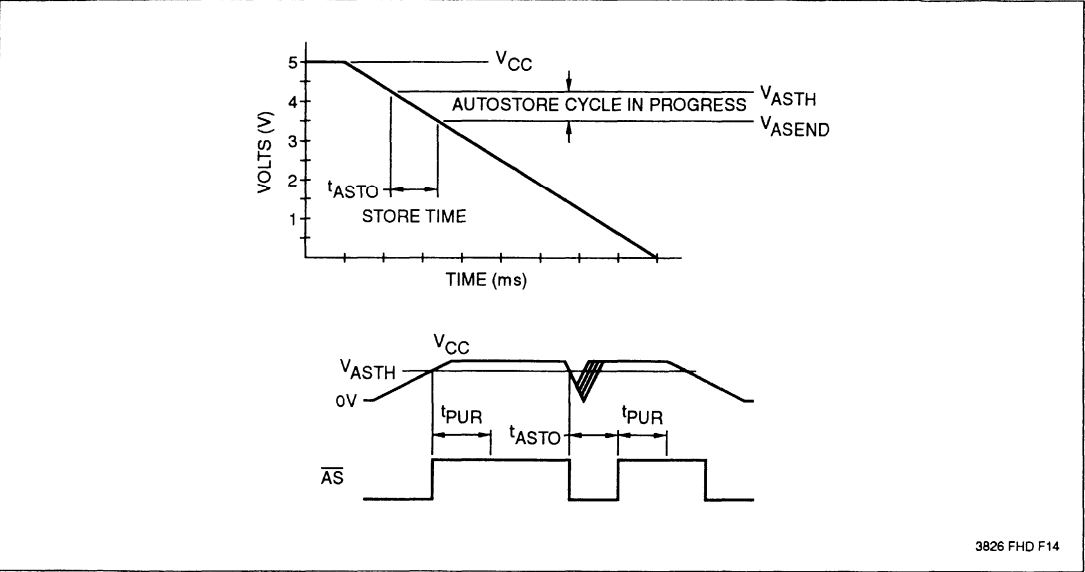
# X20C16

## AUTOSTORE Feature

The AUTOSTORE feature automatically saves the contents of the X20C16's Static RAM to the on-board bit-for-bit shadow E<sup>2</sup>PROM at power down. This circuitry insures that no data is lost during accidental power downs or general system crashes, and is ideal for microprocessor caching systems, embedded software systems, and general system back-up memory.

The AUTOSTORE instruction (EAS) to the SDP register sets the AUTOSTORE enable latch, allowing the X20C16 to automatically perform a store operation whenever  $V_{CC}$  falls below the AUTOSTORE threshold ( $V_{ASTH}$ ).  $V_{CC}$  must remain above the AUTOSTORE Cycle End Voltage ( $V_{ASEND}$ ) for the duration of the store cycle ( $t_{ASTO}$ ). The detailed timing for this feature is illustrated in the AUTOSTORE timing diagram, below. Once the AUTOSTORE cycle is initiated, all other device functions are inhibited.

## AUTOSTORE CYCLE Timing Diagrams

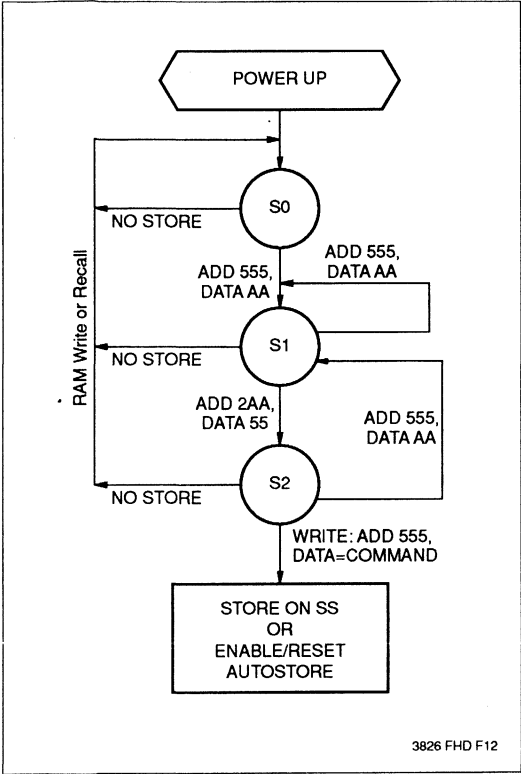


## AUTOSTORE CYCLE LIMITS

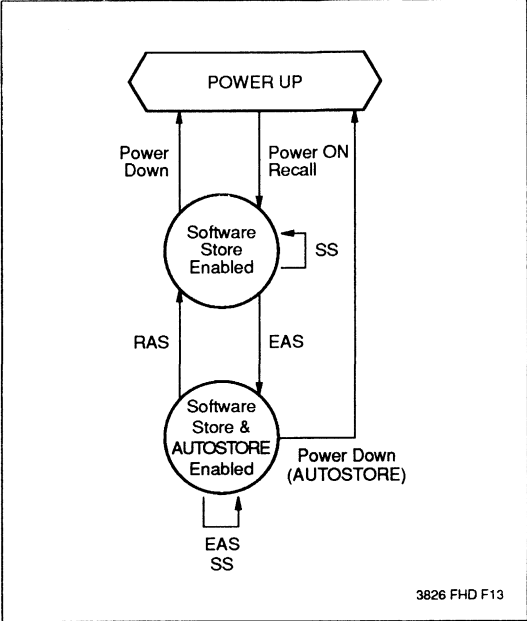
Symbol	Parameter	X20C16		Units
		Min.	Max.	
$t_{ASTO}$	AUTOSTORE Cycle Time		2.5	ms
$V_{ASTH}$	AUTOSTORE Threshold Voltage	4.0	4.3	V
$V_{ASEND}$	AUTOSTORE Cycle End Voltage	3.5		V

3826 PGM T15

SDP (Software Data Protection)



Store State Diagram



1

SOFTWARE DATA PROTECTION COMMANDS

Command		Data [Hex]
EAS	Enable AUTOSTORE	CC
RAS	Reset AUTOSTORE	CD
SS	Software Store	33

3826 PGM T14

**X20C16**

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**NOTES**



<b>NOVRAM* Data Sheets</b>	<b>1</b>
<b>Serial Products Data Sheets</b>	<b>2</b>
<b>E<sup>2</sup>PROM Data Sheets</b>	<b>3</b>
<b>E<sup>2</sup>POT™ Data Sheets</b>	<b>4</b>
<b>Microcontroller Peripheral Products</b>	<b>5</b>
<b>Memory Subsystems</b>	<b>6</b>
<b>Military Products</b>	<b>7</b>
<b>Die Products</b>	<b>8</b>
<b>Application Notes and Briefs</b>	<b>9</b>
<b>Reliability</b>	<b>10</b>
<b>General Information</b>	<b>11</b>





## Preliminary Information

256 Bit

X24C44

16 x 16 Bit

## Serial Nonvolatile Static RAM

### FEATURES

- Advanced CMOS Version of Xicor's X2444
- 16 x 16 Organization
- Single 5 Volt Supply
- Ideal for use with Single Chip Microcomputers
  - Static Timing
  - Minimum I/O Interface
  - Serial Port Compatible (COPS™, 8051)
  - Easily Interfaced to Microcontroller Ports
- Software and Hardware Control of Nonvolatile Functions
- Auto Recall on Power-Up
- TTL and CMOS Compatible
- Low Power Dissipation
  - Active Current: 10 mA Maximum
  - Standby Current: 50  $\mu$ A Maximum
- 8 Pin Mini-DIP and 8 Lead SOIC Packages
- High Reliability
  - Store Cycles: 1,000,000
  - Data Retention: 100 Years

### DESCRIPTION

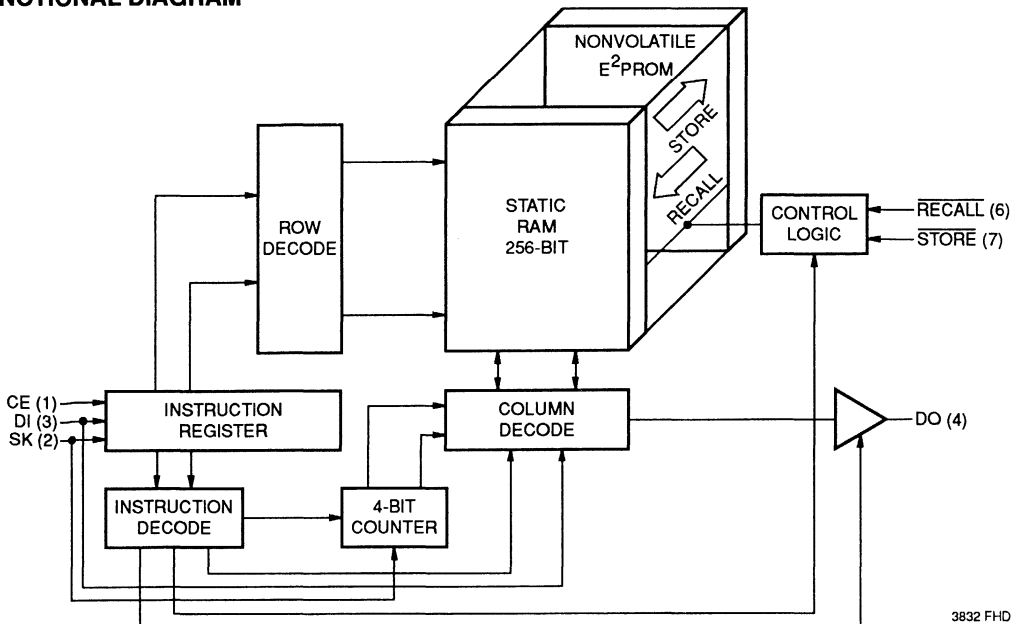
The Xicor X24C44 is a serial 256 bit NOVRAM featuring a static RAM configured 16 x 16, overlaid bit by bit with a nonvolatile E<sup>2</sup>PROM array. The X24C44 is fabricated with Xicor's Advanced CMOS Floating Gate technology.

The Xicor NOVRAM design allows data to be transferred between the two memory arrays by means of software commands or external hardware inputs. A store operation (RAM data to E<sup>2</sup>PROM) is completed in 5 ms or less and a recall operation (E<sup>2</sup>PROM data to RAM) is completed in 2  $\mu$ s or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E<sup>2</sup>PROM and a minimum 1,000,000 store operations. Inherent data retention is specified to be greater than 100 years.

2

### FUNCTIONAL DIAGRAM



3832 FHD F01

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2-1

Characteristics subject to change without notice

3832-1

# X24C44

## PIN DESCRIPTIONS

### Chip Enable (CE)

The Chip Enable input must be HIGH to enable all read/write operations. CE must remain HIGH following a Read or Write command until the data transfer is complete. CE LOW places the X24C44 in the low power standby mode and resets the instruction register. Therefore, CE must be brought LOW after the completion of an operation in order to reset the instruction register in preparation for the next command.

### Serial Clock (SK)

The Serial Clock input is used to clock all data into and out of the device.

### Data In (DI)

Data In is the serial data input.

### Data Out (DO)

Data Out is the serial data output. It is in the high impedance state except during data output cycles in response to a READ instruction.

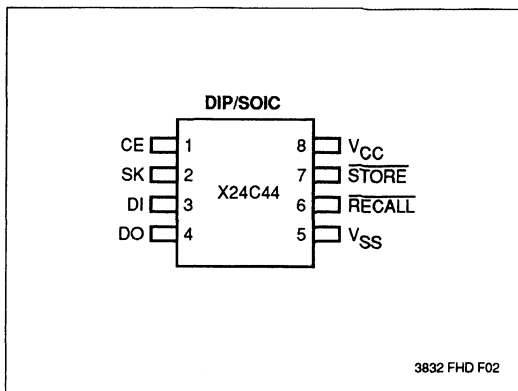
### STORE

STORE LOW will initiate an internal transfer of data from RAM to the E<sup>2</sup>PROM array.

### RECALL

RECALL LOW will initiate an internal transfer of data from E<sup>2</sup>PROM to the RAM array.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
CE	Chip Enable
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
RECALL	Recall Input
STORE	Store Input
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground

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# X24C44

## DEVICE OPERATION

The X24C44 contains an 8-bit instruction register. It is accessed via the DI input, with data being clocked in on the rising edge of SK. CE must be HIGH during the entire data transfer operation.

Table 1 contains a list of the instructions and their operation codes. The most significant bit (MSB) of all instructions is a logic one (HIGH), bits 6 through 3 are either RAM address (A) or don't care (X) and bits 2 through 0 are the operation codes. The X24C44 requires the instruction to be shifted in with the MSB first.

After CE is HIGH, the X24C44 will not begin to interpret the data stream until a logic one has been shifted in on DI. Therefore, CE may be brought HIGH with SK running and DI LOW. DI must then go HIGH to indicate the start condition of an instruction before the X24C44 will begin any action.

In addition, the SK clock is totally static. The user can completely stop the clock and data shifting will be stopped. Restarting the clock will resume shifting of data.

### RCL and RECALL

Either a software RCL instruction or a LOW on the RECALL input will initiate a transfer of E<sup>2</sup>PROM data into RAM. This software or hardware recall operation sets an internal "previous recall" latch. This latch is reset upon power-on and must be intentionally set by the user to enable any write or store operations. Although a recall operation is performed upon power-up, the previous recall latch is not set by this operation.

### WRDS and WREN

Internally the X24C44 contains a "write enable" latch. This latch must be set for either writes to the RAM or store

operations to the E<sup>2</sup>PROM. The WREN instruction sets the latch and the WRDS instruction resets the latch, disabling both RAM writes and E<sup>2</sup>PROM stores, effectively protecting the nonvolatile data from corruption. The write enable latch is automatically reset on power-up.

### STO and STORE

Either the software STO instruction or a LOW on the STORE input will initiate a transfer of data from RAM to E<sup>2</sup>PROM. In order to safeguard against unwanted store operations, the following conditions must be true:

- STO instruction issued or STORE input is LOW.
- The internal write enable latch must be set (WREN instruction issued).
- The "previous recall" latch must be set (either a software or hardware recall operation).

Once the store cycle is initiated, all other device functions are inhibited. Upon completion of the store cycle, the write enable latch is reset. Refer to Figure 4 for a state diagram description of enabling/disabling conditions for store operations.

### WRITE

The WRITE instruction contains the 4 bit address of the word to be written. The write instruction is immediately followed by the 16-bit word to be written. CE must remain HIGH during the entire operation. CE must go LOW before the next rising edge of SK. If CE is brought LOW prematurely (after the instruction but before 16 bits of data are transferred), the instruction register will be reset and the data that was shifted-in will be written to RAM.

If CE is kept HIGH for more than 24 SK clock cycles (8-bit instruction plus 16-bit data), the data already shifted-in will be overwritten.

2

Table 1: Instruction Set

Instruction	Format, I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	Operation
WRDS (Figure 3)	1XXXX000	Reset Write Enable Latch (Disables Writes and Stores)
STO (Figure 3)	1XXXX001	Store RAM Data in E <sup>2</sup> PROM
Reserved	1XXXX010	N/A
WRITE (Figure 2)	1AAAA011	Write Data into RAM Address AAAA
WREN (Figure 3)	1XXXX100	Set Write Enable Latch (Enables Writes and Stores)
RCL (Figure 3)	1XXXX101	Recall E <sup>2</sup> PROM Data into RAM
READ (Figure 1)	1AAAA11X	Read Data from RAM Address AAAA

X = Don't Care  
A = Address

3832 PGM T13



## X24C44

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### READ

The READ instruction contains the 4 bit address of the word to be accessed. Unlike the other six instructions,  $I_0$  of the instruction word is a "don't care". This provides two advantages. In a design that ties both DI and DO together, the absence of an eighth bit in the instruction allows the host time to convert an I/O line from an output to an input. Secondly, it allows for valid data output during the ninth SK clock cycle.

DO, the first bit output during a read operation, is truncated. That is, it is internally clocked by the falling edge of the eighth SK clock; whereas, all succeeding bits are clocked by the rising edge of SK (refer to Read Cycle Diagram).

### LOW POWER MODE

When CE is LOW, non-critical internal devices are powered-down, placing the device in the standby power mode, thereby minimizing power consumption.

### SLEEP

Because the X24C44 is a low power CMOS device, the SLEEP instruction implemented on the first generation NMOS device has been deleted. For systems converting from the X2444 to the X24C44 the software need not be changed; the instruction will be ignored.

### WRITE PROTECTION

The X24C44 provides two software write protection mechanisms to prevent inadvertent stores of unknown data.

#### Power-Up Condition

Write Enable Latch. Upon power-up the "write enable" latch is in the reset state, disabling any store operation.

#### Unknown Data Store

Previous Recall Latch. The "previous recall" latch must be set after power-up. It may be set only by performing a software or hardware recall operation, which assures that data in all RAM locations is valid.

### SYSTEM CONSIDERATIONS

#### Power-On Recall

The X24C44 performs a power-on recall that transfers the E<sup>2</sup>PROM contents to the RAM array. Although the data may be read from the RAM array, this recall does not set the "previous recall" latch. During this power-on recall operation, all commands are ignored. Therefore, the host should delay any operations with the X24C44 a minimum of  $t_{PUR}$  after  $V_{CC}$  is stable.

#### Power-Down Data Protection

Because the X24C44 is a 5V only nonvolatile memory device it may be susceptible to inadvertent stores to the E<sup>2</sup>PROM array during power-down cycles. Power-up cycles are not a problem because the previous recall latch and write enable latch are reset, preventing any possible corruption of E<sup>2</sup>PROM data.

#### Software Power-Down Protection

If the  $\overline{\text{STORE}}$  and  $\overline{\text{RECALL}}$  pins are tied to  $V_{CC}$  through a pullup resistor and only software operations are performed to initiate stores, there is little likelihood of an inadvertent store. However, if these two lines are under microprocessor control, positive action should be employed to negate the possibility of these control lines bouncing and generating an unwanted store. The safest method is to issue the WRDS command after a write sequence and also following store operations. Note: an internal store may take up to 5 ms; therefore, the host microprocessor should delay 5 ms after initiating the store prior to issuing the WRDS command.

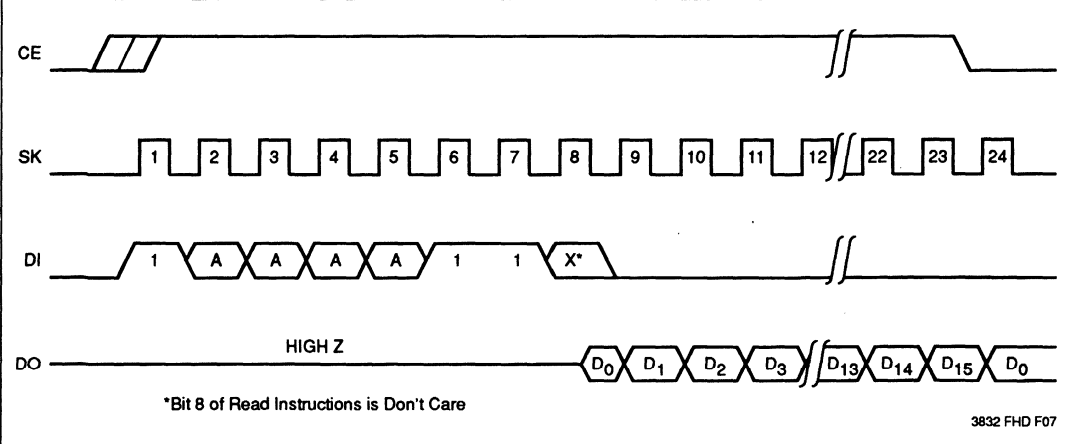
#### Hardware Power-Down Protection

(when the "write enable" latch and "previous recall" latch are **not in the reset state**):

Write Inhibit. Holding either  $\overline{\text{RECALL}}$  LOW, CE LOW or  $\overline{\text{STORE}}$  HIGH during power-down will prevent an inadvertent store.

# X24C44

Figure 1. RAM Read



2

Figure 2. RAM Write

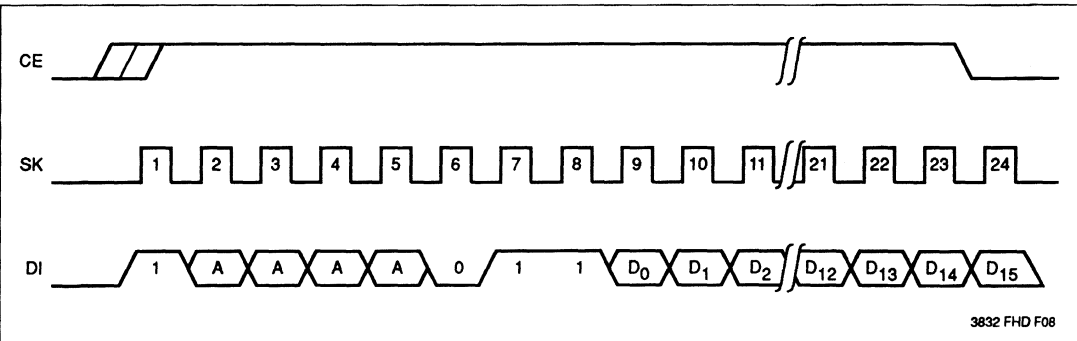
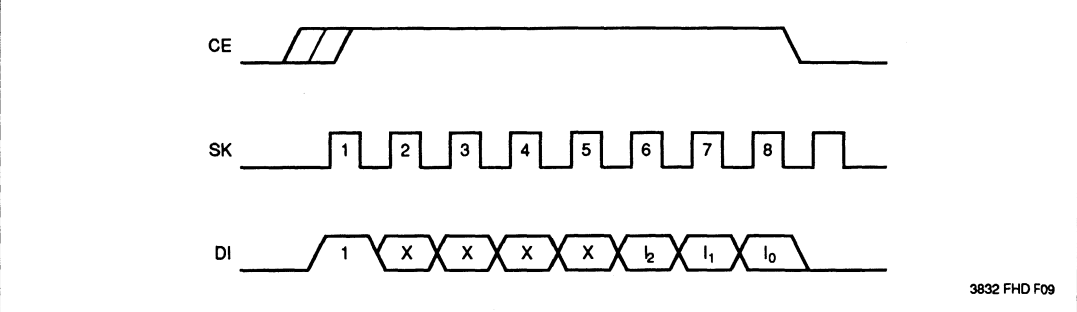
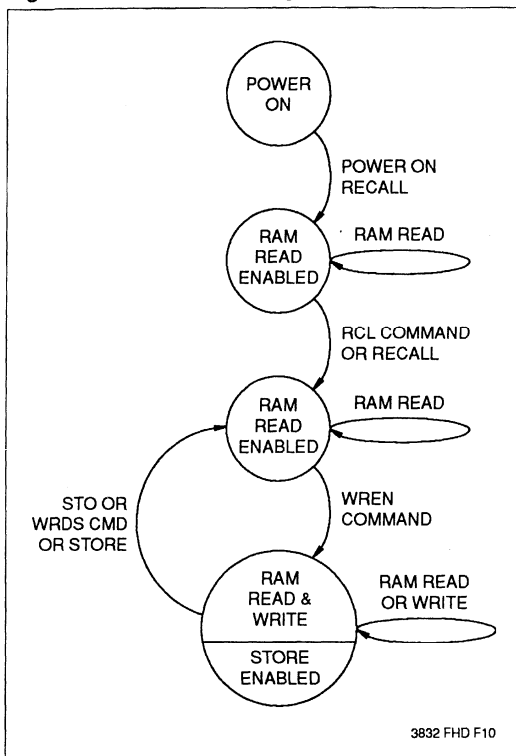


Figure 3. Non-Data Operations



## X24C44

Figure 4. X24C44 State Diagram



# X24C44

2

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	-65°C to +135°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin with Respect to Ground .....	-1.0V to +7.0V
D.C. Output Current .....	5 mA
Lead Temperature (Soldering, 10 Seconds) .....	300°C

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

Supply Voltage	Limits
X24C44	5V ± 10%

3832 PGM T03

## D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Supply Current (TTL Inputs)		10	mA	SK = 0.4V/2.4V Levels @ 1 MHz, DO = Open, All Other Inputs = V <sub>IH</sub>
I <sub>SB1</sub>	V <sub>CC</sub> Standby Current (TTL Inputs)		1	mA	DO = Open, CE = V <sub>IL</sub> , All Other Inputs = V <sub>IH</sub>
I <sub>SB2</sub>	V <sub>CC</sub> Standby Current (CMOS Inputs)		50	µA	DO = Open, CE = GND, All Other Inputs = V <sub>CC</sub> - 0.3V
I <sub>LI</sub>	Input Load Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> (1)	Input Low Voltage	-1.0	0.8	V	
V <sub>IH</sub> (1)	Input High Voltage	2.0	V <sub>CC</sub> + 1	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 4.2 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -2mA

3832 PGM T04

## ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

3832 PGM T05

## CAPACITANCE T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 5V

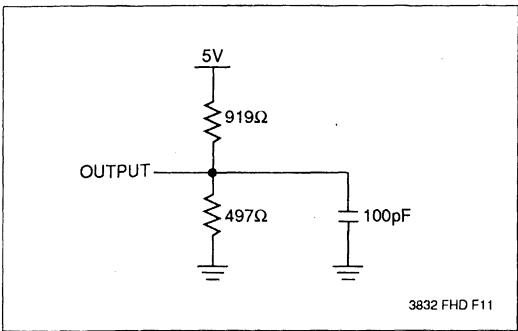
Symbol	Parameter	Max.	Units	Test Conditions
C <sub>OUT</sub> (2)	Output Capacitance	8	pF	V <sub>OUT</sub> = 0V
C <sub>IN</sub> (2)	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

3832 PGM T06

Notes: (1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.

# X24C44

## EQUIVALENT A.C. LOAD CIRCUIT



## A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V

3832 PGM T07

## A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

### Read and Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
$F_{SK}^{(3)}$	SK Frequency		1.0	MHz
$t_{SKH}$	SK Positive Pulse Width	400		ns
$t_{SKL}$	SK Negative Pulse Width	400		ns
$t_{DS}$	Data Setup Time	400		ns
$t_{DH}$	Data Hold Time	80		ns
$t_{PD1}$	SK to Data Bit 0 Valid		375	ns
$t_{PD}$	SK to Data Valid		375	ns
$t_z$	Chip Enable to Output High Z		1.0	μs
$t_{CES}$	Chip Enable Setup	800		ns
$t_{CEH}$	Chip Enable Hold	350		ns
$t_{CDS}$	Chip Deselect	800		ns

3832 PGM T08

## POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(4)}$	Power-up to Read Operation	200	μs
$t_{PUW}^{(4)}$	Power-up to Write or Store Operation	5	ms

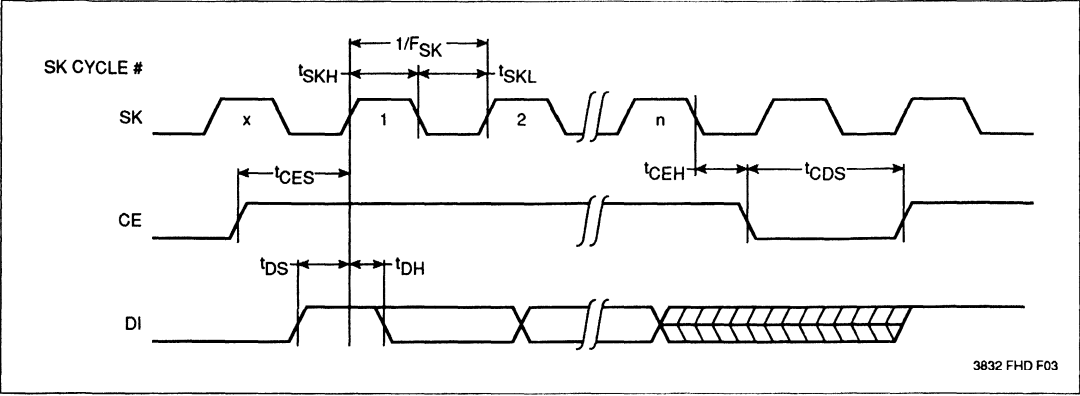
3832 PGM T09

**Notes:** (3) SK rise and fall times must be less than 50 ns.

(4)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

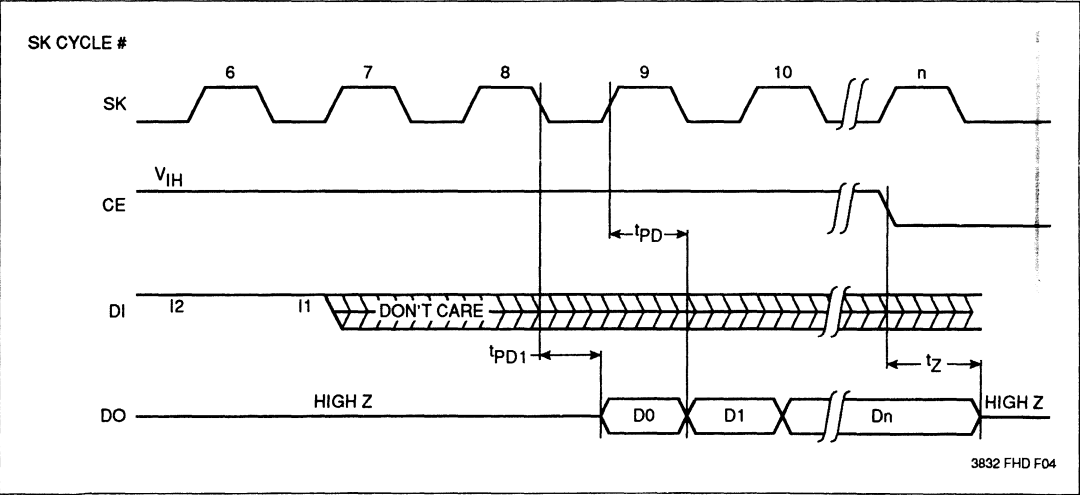
**X24C44**

**Write Cycle**



2

**Read Cycle**



# X24C44

## NONVOLATILE OPERATIONS

Operation	$\overline{\text{STORE}}$	$\overline{\text{RECALL}}$	Software Instruction	Write Enable Latch State	Previous Recall Latch State
Hardware Recall	1	0	NOP <sup>(5)</sup>	X	X
Software Recall	1	1	RCL	X	X
Hardware Store	0	1	NOP <sup>(5)</sup>	SET	SET
Software Store	1	1	STO	SET	SET

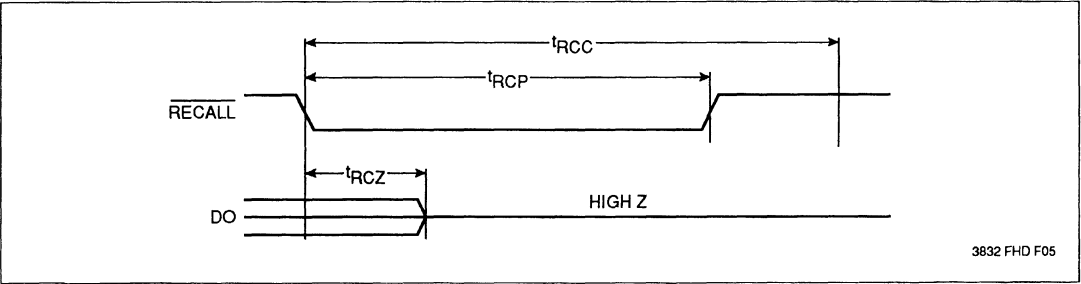
3832 PGM T10

## ARRAY RECALL LIMITS

Symbol	Parameter	Min.	Max.	Units
$t_{\text{RCC}}$	Recall Cycle Time	2		$\mu\text{s}$
$t_{\text{RCP}}$	Recall Pulse Width <sup>(6)</sup>	500		ns
$t_{\text{RCZ}}$	Recall to Output in High Z		500	ns

3832 PGM T11

## Recall Timing



3832 FHD F05

- Notes:** (5) NOP designates when the X24C44 is not currently executing an instruction.  
(6) Recall rise time must be  $<10\mu\text{s}$ .

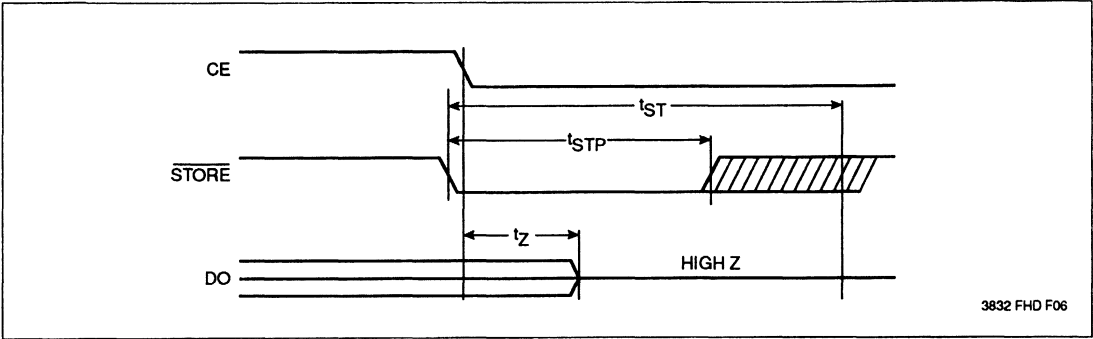
X24C44

STORE CYCLE LIMITS

Symbol	Parameter	Min.	Typ.(7)	Max.	Units
t <sub>ST</sub>	Store Time		2	5	ms
t <sub>STP</sub>	Store Pulse Width	200			ns
t <sub>z</sub>	CE to Output in High Z			1	μs
V <sub>CC</sub>	Store Inhibit		3		V

3832 PGM T12

Store Timing



**Note:** (7) Typical values are for  $T_A = 25^{\circ}\text{C}$  and nominal supply voltage.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance



**X24C44**

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**NOTES**



## Serial AUTOSTORE™ NOVRAM

## FEATURES

- **AUTOSTORE™ NOVRAM**
  - Automatically Performs a Store Operation Upon Loss of  $V_{CC}$
- **Single 5 Volt Supply**
- **Ideal for use with Single Chip Microcomputers**
  - Minimum I/O Interface
  - Serial Port Compatible (COPS™, 8051)
  - Easily Interfaced to Microcontroller Ports
- **Software and Hardware Control of Nonvolatile Functions**
- **Auto Recall on Power-Up**
- **TTL and CMOS Compatible**
- **Low Power Dissipation**
  - Active Current: 10 mA
  - Standby Current: 50  $\mu$ A
- **8 Pin Mini-DIP and 8 Lead SOIC Packages**
- **High Reliability**
  - Store Cycles: 1,000,000
  - Data Retention: 100 Years

## DESCRIPTION

The Xicor X24C45 is a serial 256 bit NOVRAM featuring a static RAM configured 16 x 16, overlaid bit by bit with a nonvolatile E<sup>2</sup>PROM array. The X24C45 is fabricated with Xicor's Advanced CMOS Floating Gate technology.

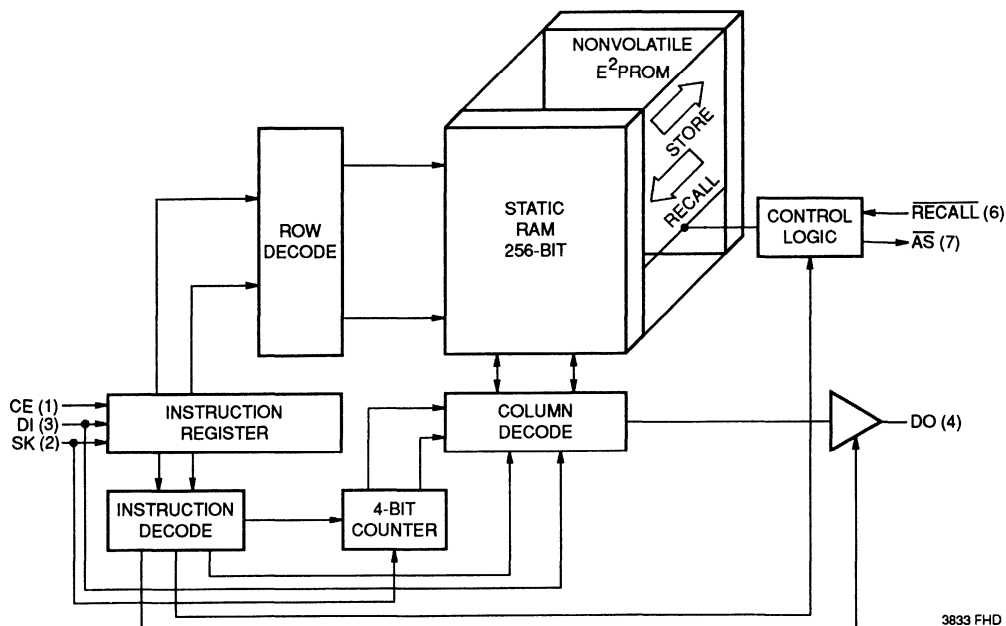
The Xicor NOVRAM design allows data to be transferred between the two memory arrays by means of software commands or external hardware inputs. A store operation (RAM data to E<sup>2</sup>PROM) is completed in 5 ms or less and a recall operation (E<sup>2</sup>PROM data to RAM) is completed in 2  $\mu$ s or less.

The X24C45 also includes the AUTOSTORE feature, a user selectable feature that automatically performs a store operation when  $V_{CC}$  falls below a preset threshold.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E<sup>2</sup>PROM and a minimum 1,000,000 store operations. Inherent data retention is specified to be greater than 100 years.

2

## FUNCTIONAL DIAGRAM



3833 FHD F01

AUTOSTORE™ NOVRAM is a trademark of Xicor, Inc.  
COPS is a trademark of National Semiconductor Corp.

# X24C45

## PIN DESCRIPTIONS

### Chip Enable (CE)

The Chip Enable input must be HIGH to enable all read/write operations. CE must remain HIGH following a Read or Write command until the data transfer is complete. CE LOW places the X24C45 in the low power standby mode and resets the instruction register. Therefore, CE must be brought LOW after the completion of an operation in order to reset the instruction register in preparation for the next command.

### Serial Clock (SK)

The Serial Clock input is used to clock all data into and out of the device.

### Data In (DI)

Data In is the serial data input.

### Data Out (DO)

Data Out is the serial data output. It is in the high impedance state except during data output cycles in response to a READ instruction.

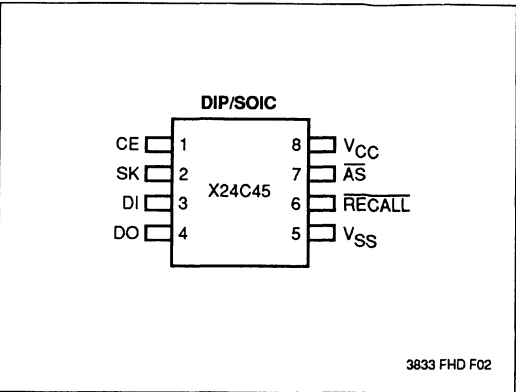
### AUTOSTORE Output ( $\overline{AS}$ )

$\overline{AS}$  is an open drain output which, when asserted indicates  $V_{CC}$  has fallen below the AUTOSTORE threshold ( $V_{ASTH}$ ).  $\overline{AS}$  may be wire-ORed with multiple open drain outputs and used as an interrupt input to a microcontroller or as an input to a low power reset circuit.

### RECALL

RECALL LOW will initiate an internal transfer of data from E2PROM to the RAM array.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
CE	Chip Enable
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
RECALL	Recall Input
$\overline{AS}$	AUTOSTORE Output
VCC	+5V
VSS	Ground

3833 PGM T01

# X24C45

## DEVICE OPERATION

The X24C45 contains an 8-bit instruction register. It is accessed via the DI input, with data being clocked in on the rising edge of SK. CE must be HIGH during the entire data transfer operation.

Table 1 contains a list of the instructions and their operation codes. The most significant bit (MSB) of all instructions is a logic one (HIGH), bits 6 through 3 are either RAM address (A) or don't care (X) and bits 2 through 0 are the operation codes. The X24C45 requires the instruction to be shifted in with the MSB first.

After CE is HIGH, the X24C45 will not begin to interpret the data stream until a logic one has been shifted in on DI. Therefore, CE may be brought HIGH with SK running and DI LOW. DI must then go HIGH to indicate the start condition of an instruction before the X24C45 will begin any action.

In addition, the SK clock is totally static. The user can completely stop the clock and data shifting will be stopped. Restarting the clock will resume shifting of data.

## RCL and RECALL

Either a software RCL instruction or a LOW on the RECALL input will initiate a transfer of E2PROM data into RAM. This software or hardware recall operation sets an internal "previous recall" latch. This latch is reset upon power-on and must be intentionally set by the user

to enable any write or store operations. Although a recall operation is performed upon power-up, the previous recall latch is not set by this operation.

## WRDS and WREN

Internally the X24C45 contains a "write enable" latch. This latch must be set for either writes to the RAM or store operations to the E2PROM. The WREN instruction sets the latch and the WRDS instruction resets the latch, disabling both RAM writes and E2PROM stores, effectively protecting the nonvolatile data from corruption. The write enable latch is automatically reset on power-up.

## STO

The software STO instruction will initiate a transfer of data from RAM to E2PROM. In order to safeguard against unwanted store operations, the following conditions must be true:

- STO instruction issued.
- The internal write enable latch must be set (WREN instruction issued).
- The "previous recall" latch must be set (either a software or hardware recall operation).

Once the store cycle is initiated, all other device functions are inhibited. Upon completion of the store cycle, the write enable latch is reset. Refer to Figure 4 for a state diagram description of enabling/disabling conditions for store operations.

TABLE 1. INSTRUCTION SET

Instruction	Format, I <sub>2</sub> I <sub>1</sub> I <sub>0</sub>	Operation
WRDS (Figure 3)	1XXXX000	Reset Write Enable Latch (Disables Writes and Stores)
STO (Figure 3)	1XXXX001	Store RAM Data in E2PROM
ENAS	1XXXX010	Enable AUTOSTORE Feature
WRITE (Figure 2)	1AAAA011	Write Data into RAM Address AAAA
WREN (Figure 3)	1XXXX100	Set Write Enable Latch (Enables Writes and Stores)
RCL (Figure 3)	1XXXX101	Recall E2PROM Data into RAM
READ (Figure 1)	1AAAA11X	Read Data from RAM Address AAAA

3833 PGM T11

X = Don't Care  
A = Address

## X24C45

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### WRITE

The WRITE instruction contains the 4 bit address of the word to be written. The write instruction is immediately followed by the 16-bit word to be written. CE must remain HIGH during the entire operation. CE must go LOW before the next rising edge of SK. If CE is brought LOW prematurely (after the instruction but before 16 bits of data are transferred), the instruction register will be reset and the data that was shifted-in will be written to RAM.

If CE is kept HIGH for more than 24 SK clock cycles (8-bit instruction plus 16-bit data), the data already shifted-in will be overwritten.

### READ

The READ instruction contains the 4 bit address of the word to be accessed. Unlike the other six instructions, I<sub>0</sub> of the instruction word is a "don't care". This provides two advantages. In a design that ties both DI and DO together, the absence of an eighth bit in the instruction allows the host time to convert an I/O line from an output to an input. Secondly, it allows for valid data output during the ninth SK clock cycle.

D<sub>0</sub>, the first bit output during a read operation, is truncated. That is, it is internally clocked by the falling edge of the eighth SK clock; whereas, all succeeding bits are clocked by the rising edge of SK (refer to Read Cycle Diagram).

### LOW POWER MODE

When CE is LOW, non-critical internal devices are powered-down, placing the device in the standby power mode, thereby minimizing power consumption.

### AUTOSTORE Feature

The AUTOSTORE instruction (ENAS) sets the AUTOSTORE enable latch, allowing the X24C45 to automatically perform a store operation when V<sub>CC</sub> falls below the AUTOSTORE threshold (V<sub>ASTH</sub>).

### WRITE PROTECTION

The X24C45 provides two software write protection mechanisms to prevent inadvertent stores of unknown data.

### Power-Up Condition

Upon power-up the "write enable" and "AUTOSTORE" latches are in the reset state, disabling any store operation.

### Unknown Data Store

Previous Recall Latch. The "previous recall" latch must be set after power-up. It may be set only by performing a software or hardware recall operation, which assures that data in all RAM locations is valid.

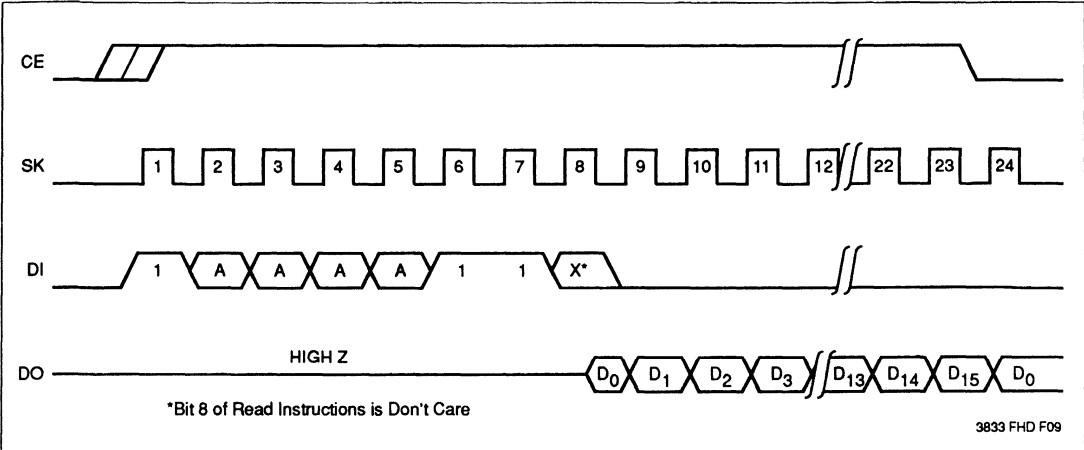
### SYSTEM CONSIDERATIONS

#### Power-On Recall

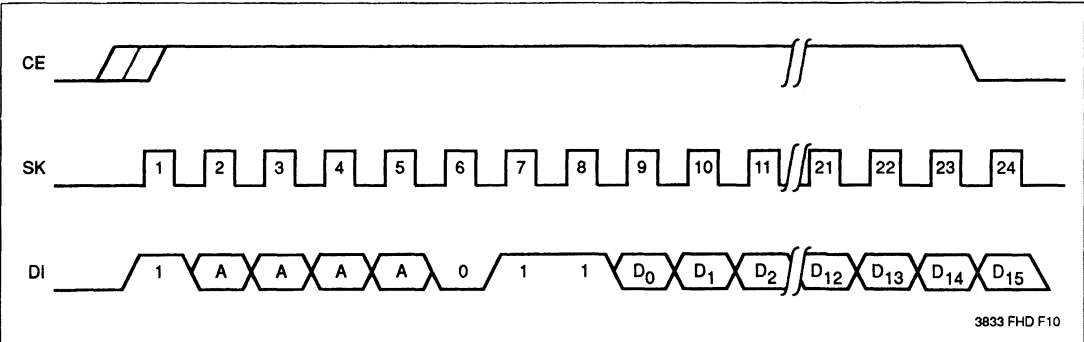
The X24C45 performs a power-on recall that transfers the E<sup>2</sup>PROM contents to the RAM array. Although the data may be read from the RAM array, this recall does not set the "previous recall" latch. During this power-on recall operation, all commands are ignored. Therefore, the host should delay any operations with the X24C45 a minimum of t<sub>PUR</sub> after V<sub>CC</sub> is stable.

**X24C45**

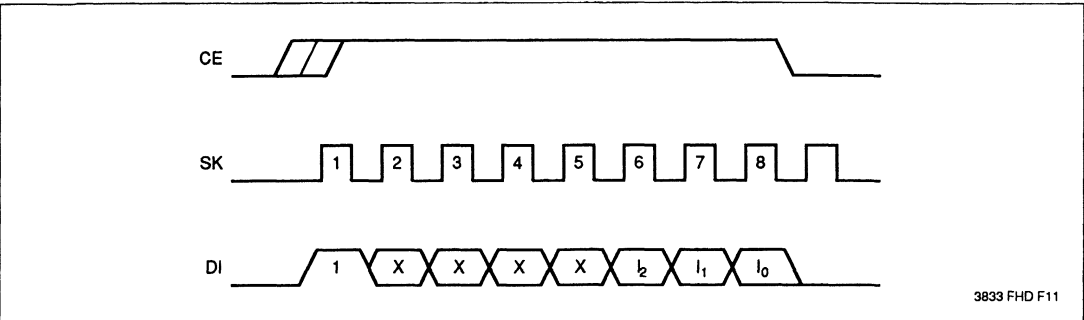
**Figure 1. RAM Read**



**Figure 2. RAM Write**

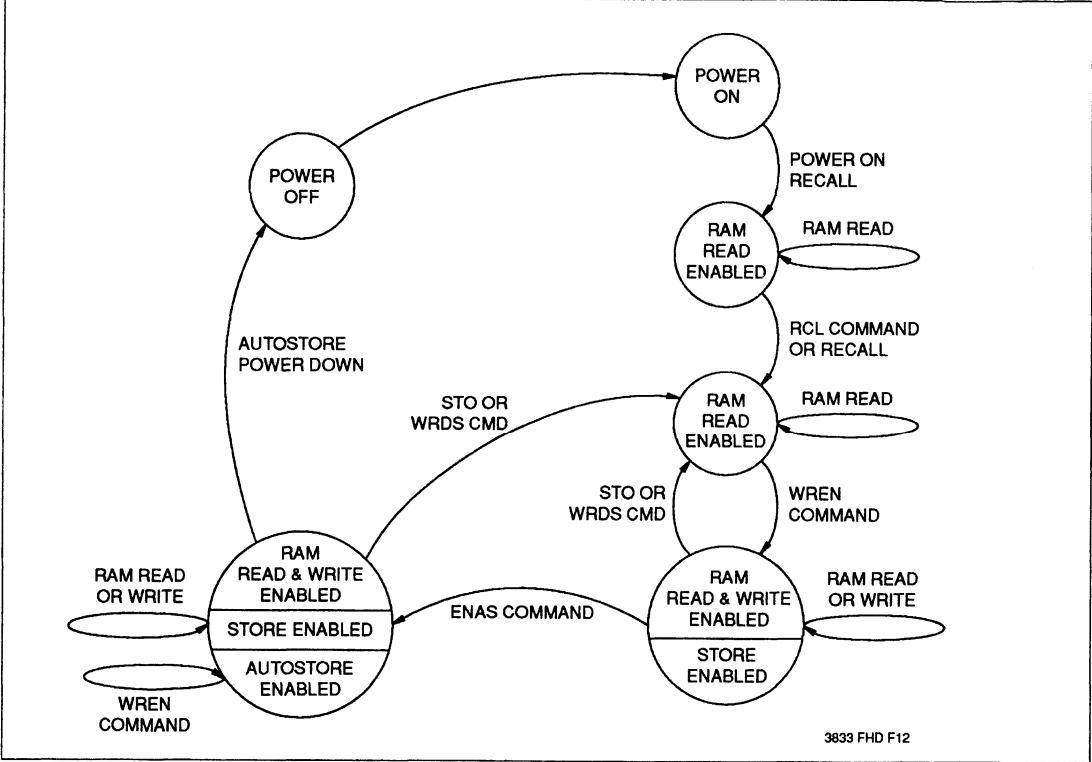


**Figure 3. Non-Data Operations**



**X24C45**

**Figure 4. X24C45 State Diagram**



# X24C45

### ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	–65°C to +135°C
Storage Temperature .....	–65°C to +150°C
Voltage on any Pin with Respect to Ground .....	–1.0V to +7.0V
D.C. Output Current .....	5 mA
Lead Temperature (Soldering, 10 Seconds) .....	300°C

### \*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3833 PGM T02

Supply Voltage	Limits
X24C45	5V ± 10%

3833 PGM T03

### D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC1</sub>	V <sub>CC</sub> Supply Current (TTL Inputs)		10	mA	SK = 0.4V/2.4V Levels @ 1 MHz, DO = Open, All Other Inputs = V <sub>IH</sub>
I <sub>CC2</sub>	V <sub>CC</sub> Supply Current (During AUTOSTORE)		2	mA	All Inputs = V <sub>IH</sub> , CE = V <sub>IL</sub> , DO = Open, V <sub>CC</sub> = 4.3V
I <sub>SB1</sub>	V <sub>CC</sub> Standby Current (TTL Inputs)		1	mA	DO = Open, CE = V <sub>IL</sub> , All Other Inputs = V <sub>IH</sub>
I <sub>SB2</sub>	V <sub>CC</sub> Standby Current (CMOS Inputs)		50	µA	DO = Open, CE = GND, All Other Inputs = V <sub>CC</sub> – 0.3V
I <sub>LI</sub>	Input Load Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> (1)	Input Low Voltage	–1.0	0.8	V	
V <sub>IH</sub> (1)	Input High Voltage	2.0	V <sub>CC</sub> + 1	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 4.2 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = –2mA
V <sub>OL(AS)</sub>	Output Low Voltage (AS)		0.4	V	I <sub>OL</sub> (AS) = 1.0mA

3833 PGM T04

### ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

3833 PGM T05

### CAPACITANCE T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C <sub>OUT</sub> (2)	Output Capacitance	8	pF	V <sub>OUT</sub> = 0V
C <sub>IN</sub> (2)	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

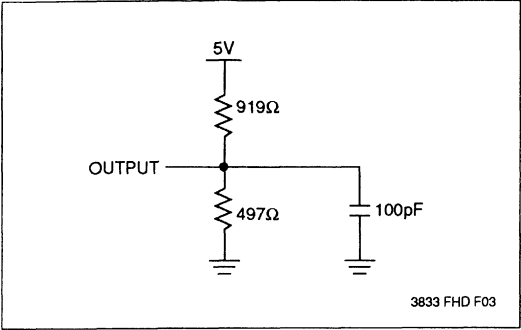
3833 PGM T06

Notes: (1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.



# X24C45

## EQUIVALENT A.C. LOAD CIRCUIT



## A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V

3833 PGM T07

## A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

### Read and Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
$F_{SK}^{(3)}$	SK Frequency		1.0	MHz
$t_{SKH}$	SK Positive Pulse Width	400		ns
$t_{SKL}$	SK Negative Pulse Width	400		ns
$t_{DS}$	Data Setup Time	400		ns
$t_{DH}$	Data Hold Time	80		ns
$t_{PD1}$	SK to Data Bit 0 Valid		375	ns
$t_{PD}$	SK to Data Valid		375	ns
$t_z$	Chip Enable to Output High Z		1.0	$\mu s$
$t_{CES}$	Chip Enable Setup	800		ns
$t_{CEH}$	Chip Enable Hold	350		ns
$t_{CDS}$	Chip Deselect	800		ns

3833 PGM T08

## POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(4)}$	Power-up to Read Operation	200	$\mu s$
$t_{PUW}^{(4)}$	Power-up to Write or Store Operation	5	ms

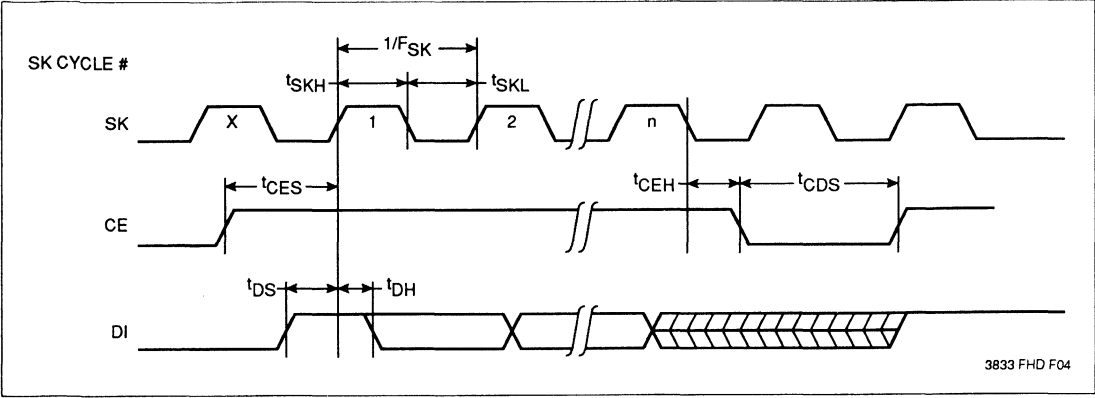
3833 PGM T09

**Notes:** (3) SK rise and fall times must be less than 50 ns.

(4)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

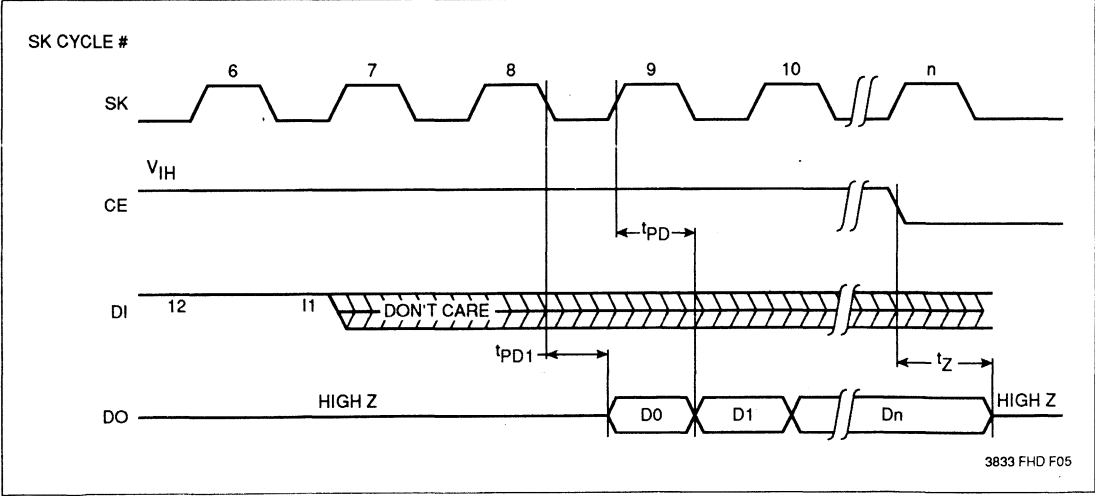
**X24C45**

**Write Cycle**



2

**Read Cycle**



X24C45

NONVOLATILE OPERATIONS

Operation	RECALL	Software Instruction	Write Enable Latch State	Previous Recall Latch State
Hardware Recall	0	NOP <sup>(5)</sup>	X	X
Software Recall	1	RCL	X	X
Software Store	1	STO	SET	SET

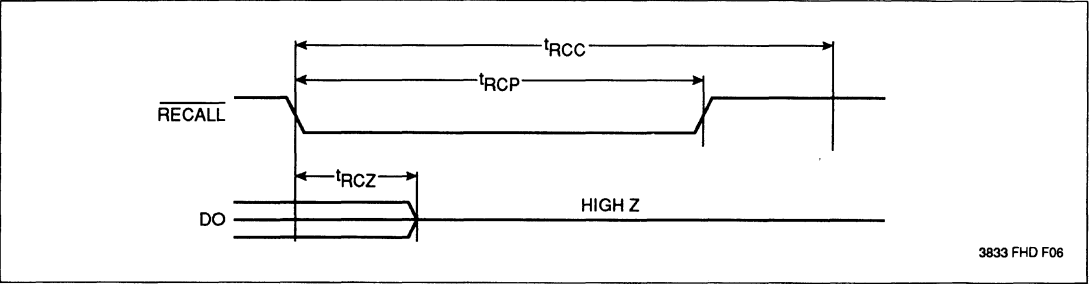
3833 PGM T10

ARRAY RECALL LIMITS

Symbol	Parameter	Min.	Max.	Units
t <sub>RCC</sub>	Recall Cycle Time	2		μs
t <sub>RCP</sub>	Recall Pulse Width <sup>(6)</sup>	500		ns
t <sub>RCZ</sub>	Recall to Output in High Z		500	ns

3833 PGM T11

Recall Timing



3833 FHD F06

SOFTWARE STORE CYCLE LIMITS

Symbol	Parameter	Min.	Typ. <sup>(7)</sup>	Max.	Units
t <sub>ST</sub>	Store Time After Clock 8 of STO CMD		2	5	ms

3833 PGM T12

- Notes: (5) NOP designates when the X24C45 is not currently executing an instruction.  
(6) Recall rise time must be <10μs.  
(7) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage.

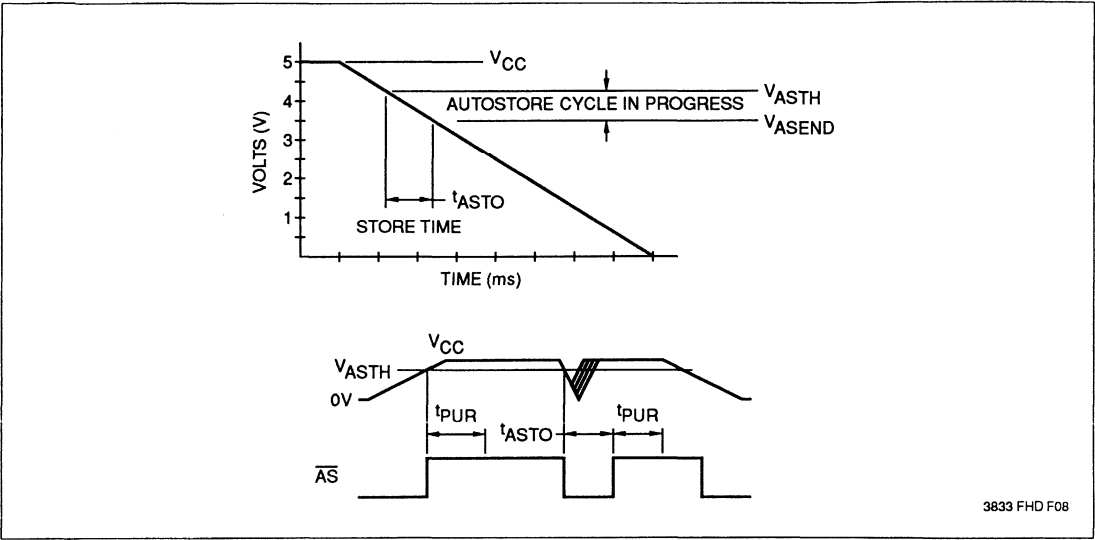
# X24C45

## AUTOSTORE Cycle Limits

Symbol	Parameter	Min.	Max.	Units
V <sub>ASTO</sub>	AUTOSTORE Cycle Time		5	ms
V <sub>ASTH</sub>	AUTOSTORE Threshold Voltage	4.0	4.3	V
V <sub>ASEND</sub>	AUTOSTORE Cycle End Voltage	3.5		V

3833 PGM T13

## AUTOSTORE Cycle Timing Diagrams



3833 FHD F08

## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**X24C45**

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**NOTES**



## Preliminary Information

128 Bit

X24C00

16 x 8 Bit

## Serial E<sup>2</sup>PROM

### FEATURES

- 3V to 5.5V Power Supply
- 128 Bit Serial E<sup>2</sup>PROM
- Low Power CMOS
  - Active Current Less Than 3 mA
  - Standby Current Less Than 50  $\mu$ A
- Internally Organized 16 x 8
- 2 Wire Serial Interface
  - Bidirectional Data Transfer Protocol
- Byte Mode Write
- Self Timed Write Cycle
  - Typical Write Cycle Time of 5 ms
- Push/Pull Output
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 100 Years
- 8-Pin Mini-DIP and 8-PIN SOIC Packages

### DESCRIPTION

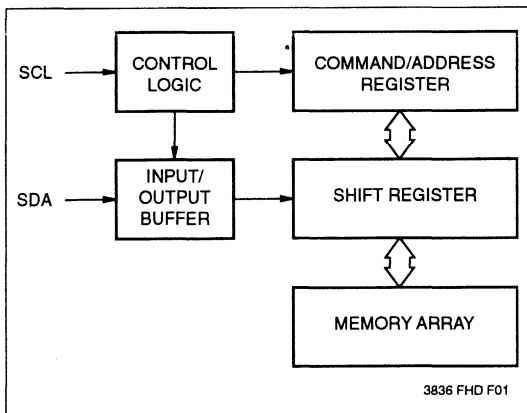
The X24C00 is a CMOS 128 bit serial E<sup>2</sup>PROM, internally organized as 16 x 8. The X24C00 features a serial interface and software protocol allowing operation on a simple two wire bus.

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

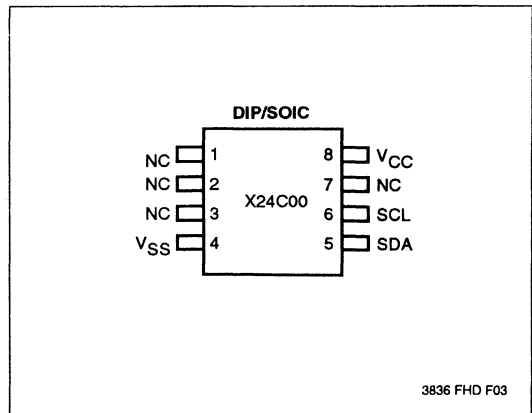
The X24C00 is fabricated with Xicor's Advanced CMOS Floating Gate technology.

2

### FUNCTIONAL DIAGRAM



### PIN CONFIGURATION



### PIN DESCRIPTIONS

#### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

#### Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is a push/pull output and does not require the use of a pull-up resistor.

### PIN NAMES

Symbol	Description
NC	No Connect
V <sub>SS</sub>	Ground
V <sub>CC</sub>	Supply Voltage
SDA	Serial Data
SCL	Serial Clock

3836 PGM T01

## X24C00

### DEVICE OPERATION

The X24C00 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X24C00 will be considered a slave in all applications.

### Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

### Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C00 continuously monitors the SDA and

SCL lines for the start condition and will not respond to any command until this condition has been met.

A start may be issued to terminate the input of a control word or the input of data to be written. This will reset the device and leave it ready to begin a new read or write command. Because of the push/pull output a start cannot be generated while the part is outputting data. Starts are also inhibited while a write is in progress.

### Stop Condition

The stop condition is a low to high transition of SDA when SCL is high. The stop condition is used to reset the device during a command or data input sequence and will leave the device in the standby mode. As with starts, stops are inhibited when outputting data and while a write is in progress.

### Write Operation

The byte write operation is initiated with a start condition. The start condition is followed by an eight bit control byte which consists of a two bit write command (0,1), four address bits, and two "don't care" bits (Figure 3).

Figure 1. Data Validity

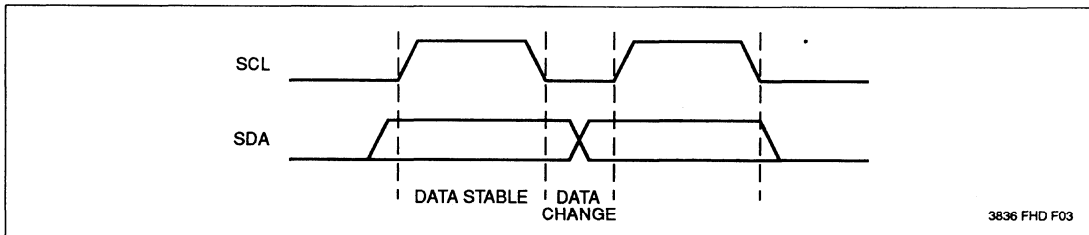


Figure 2. Definition of Start and Stop Conditions

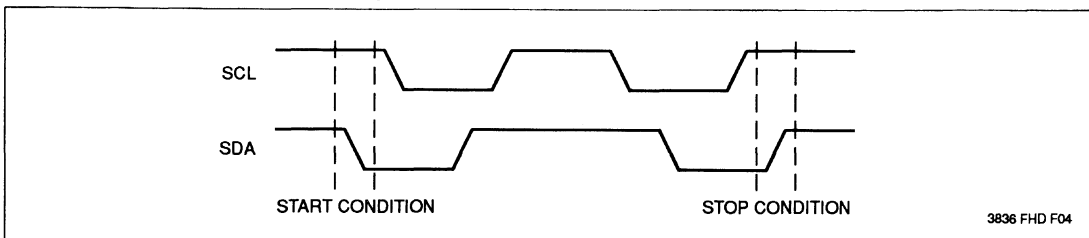
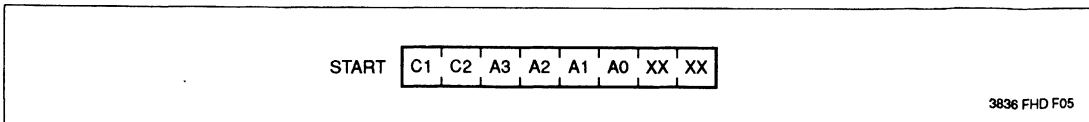


Figure 3. Control Byte



# X24C00

After receipt of the control byte the X24C00 will enter the write mode and await the data to be written. This data is shifted into the device on the next eight SCL clocks. Once eight clocks have been received the data in the shift register will be written into the memory array. While the write is in progress the X24C00 will not respond to any inputs. At any time prior to clocking in the last data bit a stop command or a new start command will terminate the operation. If a start command is given the X24C00 will reset all counters and will prepare to clock in the next control byte. If a stop command is given the X24C00 will reset all counters and await the next start command.

At the end of the write the X24C00 will automatically reset all counters and enter the standby mode. (Figure 4).

## Read Operation

The byte read operation is initiated with a start condition. The start condition is followed by an eight bit control byte which consists of a two bit read command (1,0), four address bits, and two "don't care" bits. After receipt of the control byte the X24C00 will enter the read mode and transfer data into the shift register from the array. This data is shifted out of the device on the next eight SCL clocks. At the end of the read all counters are reset and the X24C00 will enter the standby mode. As with a write, the read operation can be interrupted by a start or stop condition while the command or address is being clocked in. While clocking data out, starts or stops cannot be generated.

During the second don't care clock cycle, starts and stops are ignored. The master must free the bus prior to the end of this clock cycle to allow the X24C00 to begin outputting data (Figures 5 and 6).

2

Figure 4. Write Sequence

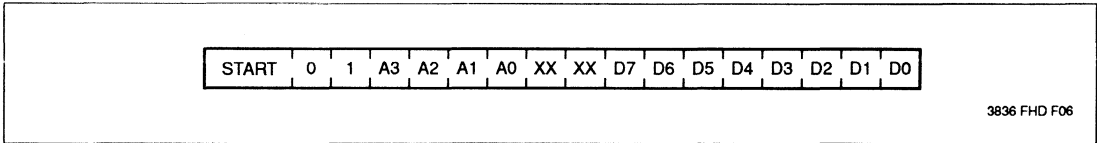


Figure 5. Read Sequence

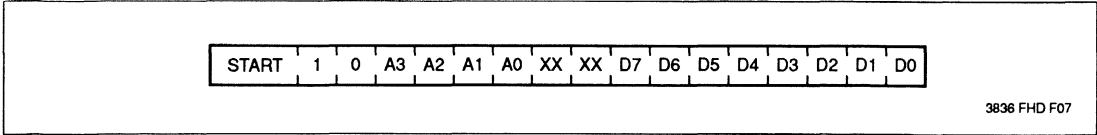
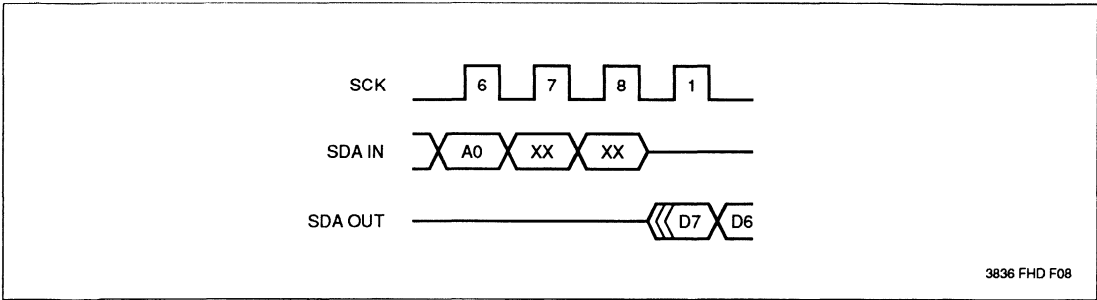


Figure 6. Read Cycle Timing





# X24C00

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X24C00 .....	-65°C to +135°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin with	
Respect to $V_{SS}$ .....	-1.0V to +7.0V
D.C. Output Current .....	5 mA
Lead Temperature	
(Soldering, 10 Seconds) .....	300°C

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

3836 PGM T02

Supply Voltage	Limits
X24C00	5V $\pm$ 10%
X24C00-3	3V to 5.5V

3836 PGM T03

## D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
$I_{CC1}$	$V_{CC}$ Supply Current Read		1	mA	SCL = $V_{CC} \times 0.1/V_{CC} \times 0.9$ Levels @ 1MHz, SDA = Open
$I_{CC2}$	$V_{CC}$ Supply Current Write		3		
$I_{SB1}$	$V_{CC}$ Standby Current		100	$\mu$ A	SCL = SDA = $V_{CC}$ $V_{CC} = 5V \pm 10\%$
$I_{SB2}$	$V_{CC}$ Standby Current		50	$\mu$ A	SCL = SDA = $V_{CC}$ $V_{CC} = 3V$
$I_{LI}$	Input Leakage Current		10	$\mu$ A	$V_{IN} = GND$ to $V_{CC}$
$I_{LO}$	Output Leakage Current		10	$\mu$ A	$V_{OUT} = GND$ to $V_{CC}$
$V_{IL}^{(1)}$	Input Low Voltage	-1.0	$V_{CC} \times 0.3$	V	
$V_{IH}^{(1)}$	Input High Voltage	$V_{CC} \times 0.7$	$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage		0.4	V	$I_{OL} = 2.1$ mA
$V_{OH}$	Output High Voltage	$V_{CC} - 0.8$		V	$I_{OH} = 1.0$ mA

3841 PGM T04

## CAPACITANCE $T_A = 25^\circ\text{C}$ , $f = 1.0$ MHz, $V_{CC} = 5V$

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}^{(2)}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0V$
$C_{IN}^{(2)}$	Input Capacitance (SCL)	6	pF	$V_{IN} = 0V$

3836 PGM T05

Notes: (1)  $V_{IL}$  min. and  $V_{IH}$  max. are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.

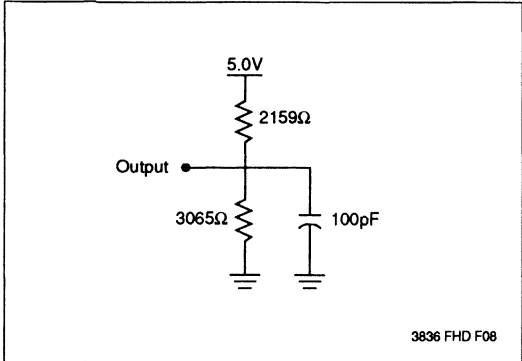
X24C00

POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(3)}$	Power-up to Read Operation	2	ms
$t_{PUW}^{(3)}$	Power-up to Write Operation	5	ms

3836 PGM T08

EQUIVALENT A.C. LOAD CIRCUIT



3836 FHD F08

A.C. CONDITIONS OF TEST

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$

3836 PGM T06

2

A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Read & Write Cycle Limits

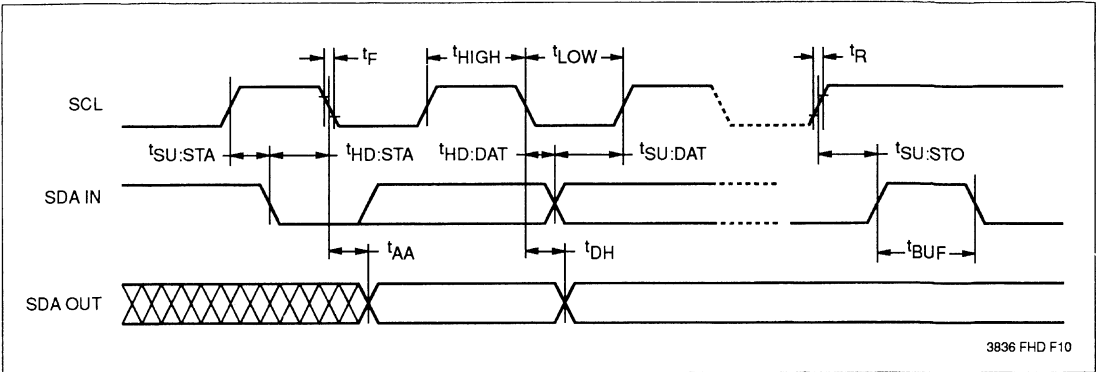
Symbol	Parameter	Min.	Max.	Units
$f_{SCL}$	SCL Clock Frequency	0	1	MHz
$t_{AA}$	SCL Low to SDA Data Out Valid		350	ns
$t_{BUF}$	Time the Bus Must Be Free Before a New Transmission Can Start	500		ns
$t_{HD:STA}$	Start Condition Hold Time	250		ns
$t_{LOW}$	Clock Low Period	500		ns
$t_{HIGH}$	Clock High Period	500		ns
$t_{SU:STA}$	Start Condition Setup Time	250		ns
$t_{HD:DAT}$	Data In Hold Time	0		μs
$t_{SU:DAT}$	Data In Setup Time	250		ns
$t_R$	SDA and SCL Rise Time		1	μs
$t_F$	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	250		ns
$t_{DH}$	Data Out Hold Time	50		ns

3836 PGM T07

**Note:** (3)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

# X24C00

## Bus Timing

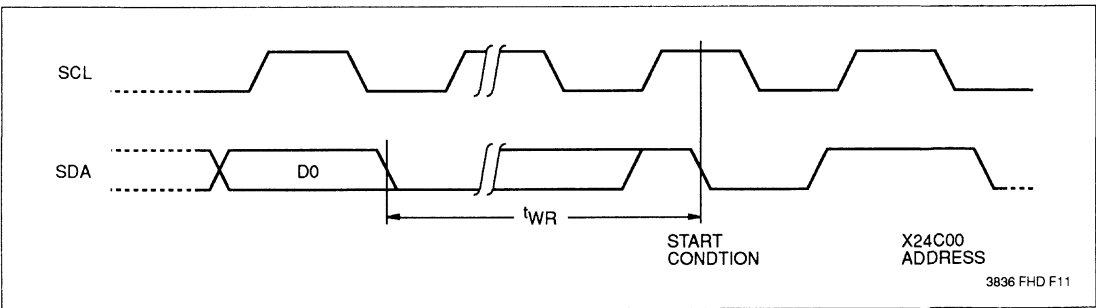


## WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Max.	Units
$t_{WR}^{(4)}$	Write Cycle Time		5	ms

3836 PGM T09

## Write Cycle Timing



**Note:** (4) The write cycle time is the time from the initiation of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C00 bus interface circuits are disabled, SDA is high impedance, and the device does not respond to start conditions.

## FEATURES

- 2.7V to 5.5V Power Supply
- 128 Bit Serial E<sup>2</sup>PROM
- Low Power CMOS
  - Active Current Less Than 1 mA
  - Standby Current Less Than 50  $\mu$ A
- Internally Organized 16 x 8
- 2 Wire Serial Interface
- High Voltage Programmable Only
  - V<sub>PGM</sub>, 12V to 15V
- Push/Pull Output
- High Reliability
  - Data Retention: 100 Years
- 8-Pin Mini-DIP and 8-PIN SOIC Packages

## DESCRIPTION

The X24001 is a CMOS 128 bit serial E<sup>2</sup>PROM, internally organized as 16 x 8. The X24001 features a serial interface and software protocol allowing operation on a simple two wire bus.

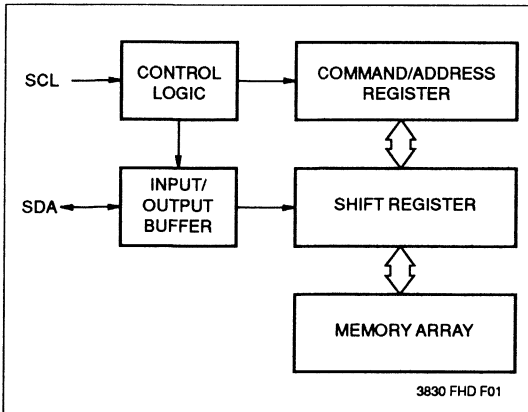
The X24001 is ideally suited for identification applications such as serial numbers or device revision numbers which need to be stored and retrieved electronically.

V<sub>PGM</sub> is used to enable writes to the device. This provides full protection of the data in the user's environment where V<sub>PGM</sub> is not available.

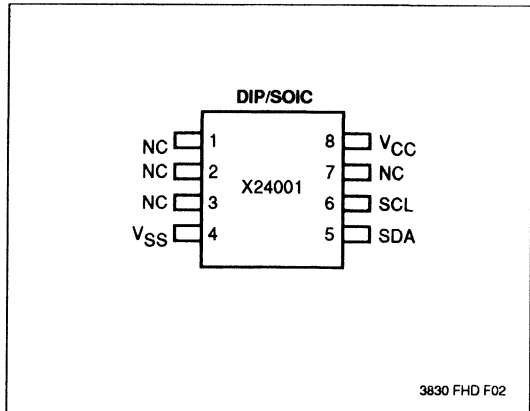
Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

The X24001 is fabricated with Xicor's Advanced CMOS Floating Gate technology.

## FUNCTIONAL DIAGRAM



## PIN CONFIGURATION



## PIN DESCRIPTIONS

### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

### Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is a push/pull output and does not require the use of a pull-up resistor. During the programming operation, SDA is an input.

IDENTI™ PROM is a trademark of Xicor, Inc.

## PIN NAMES

Symbol	Description
NC	No Connect
V <sub>SS</sub>	Ground
V <sub>CC</sub>	Supply Voltage
SDA	Serial Data
SCL	Serial Clock

3830 PGM T01

## X24001

### DEVICE OPERATION

The X24001 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X24001 will be considered a slave in all applications.

### Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

### Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24001 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

A start may be issued to terminate the input of a control word or the input of data to be written. This will reset the device and leave it ready to begin a new read or write command. Because of the push/pull output a start cannot be generated while the part is outputting data. Starts are also inhibited while a write is in progress.

### Stop Condition

The stop condition is a low to high transition of SDA when SCL is high. The stop condition is used to reset the device during a command or data input sequence and will leave the device in the standby mode. As with starts, stops are inhibited when outputting data and while a write is in progress.

Figure 1. Data Validity

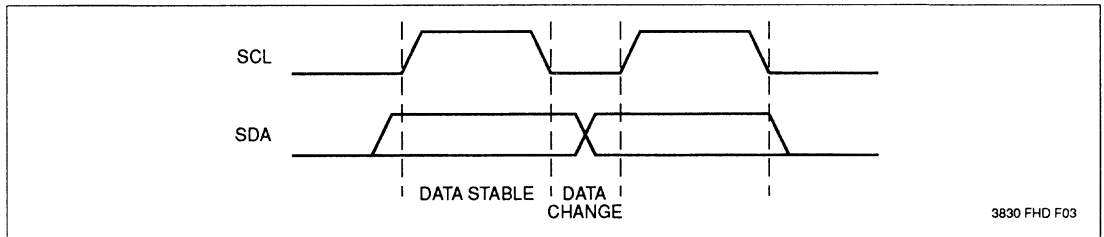
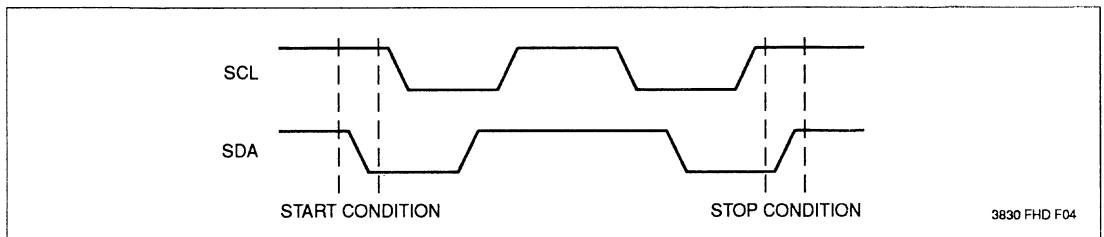


Figure 2. Definition of Start and Stop Conditions



# X24001

## Programming Operation

Programming of the X24001 is performed one byte at a time. After each byte is written a delay equal to the write cycle time of 5ms must be observed before initiating the next write cycle.

The sequence of operations is: first raise the SCL pin to  $V_{PGM}$  and generate a High to LOW transition of SDA (programming mode start); this is followed by eight bits of data containing the program command bits, four address bits and two don't care bits; this is immediately followed by the 8-bit data byte.

The timing of the operation conforms to the standard A.C. timing requirements and follows the sequence shown below. After generating the Programming Mode start condition the SCL High level can be either  $V_{IH}$  or  $V_{PGM}$ .

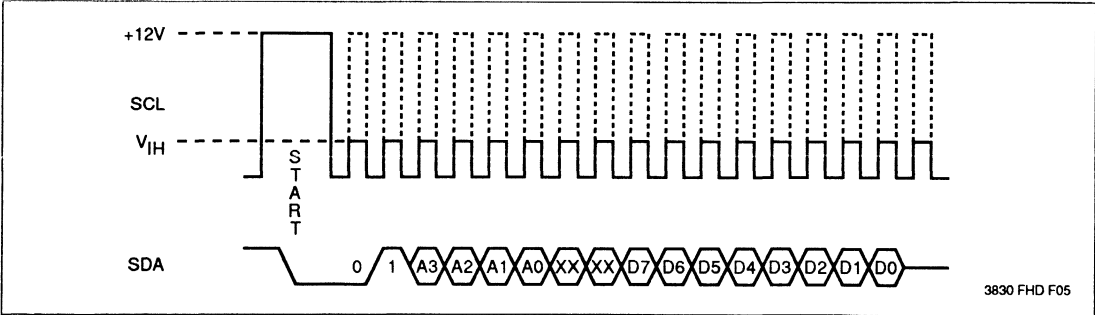
## Factory Programming Service

The X24001 can be programmed with customer specific data prior to shipment. The data programmed can be in two forms: static data pattern where there is no change in the data in a group of devices or sequential data, such as a base number incremented by one for each device tested and shipped.

Customers requiring one of these services should contact their local sales office for ordering procedures and service charges.

2

Figure 3. Programming Sequence



# X24001

## Read Operation

The byte read operation is initiated with a start condition. The start condition is followed by an eight bit control byte which consists of a two bit read command (1,0), four address bits, and two "don't care" bits. After receipt of the control byte the X24001 will enter the read mode and transfer data into the shift register from the array. This data is shifted out of the device on the next eight SCL clocks. At the end of the read all counters are reset and

the X24001 will enter the standby mode. As with a write, the read operation can be interrupted by a start or stop condition while the command or address is being clocked in. While clocking data out, starts or stops cannot be generated.

During the second don't care clock cycle, starts and stops are ignored. The master must free the bus prior to the end of this clock cycle to allow the X24001 to begin outputting data (Figures 4 and 5).

Figure 4. Read Sequence

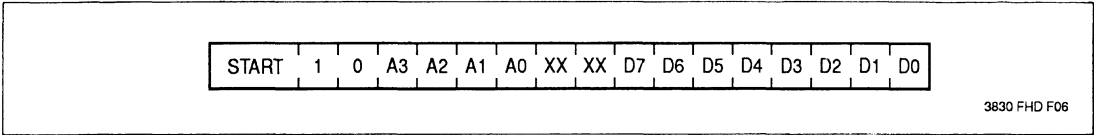
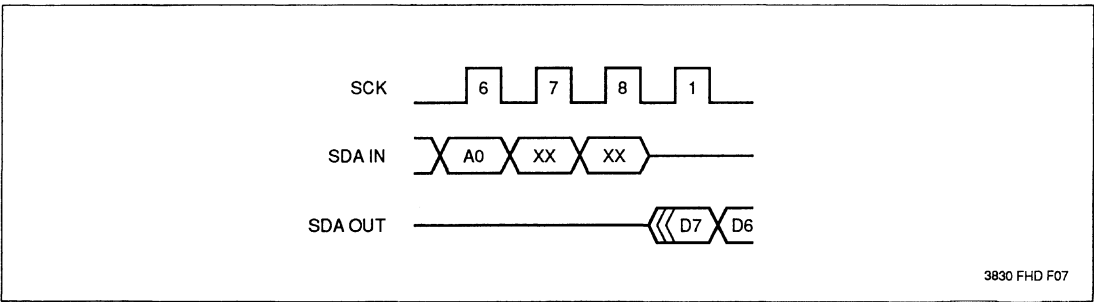


Figure 5. Read Cycle Timing



X24001

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X24001 .....	–65°C to +135°C
Storage Temperature .....	
–65°C to +150°C	
Voltage on any Pin with	
Respect to V <sub>SS</sub> .....	–1.0V to +7.0V
SCL .....	–1.0V to +17V
D.C. Output Current .....	
5 mA	
Lead Temperature	
(Soldering, 10 Seconds) .....	300°C

\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3830 PGM T02

Supply Voltage	Limits
X24001	5V ± 10%
X24001-3	3V to 5.5V
X24001-2.7	2.7V to 5.5V

3830 PGM T03

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC1</sub>	V <sub>CC</sub> Supply Current Read		1	mA	SCL = V <sub>CC</sub> X0.1/V <sub>CC</sub> X0.9 Levels @ 1MHz, SDA = Open
I <sub>SB1</sub>	V <sub>CC</sub> Standby Current		100	µA	SCL = SDA = V <sub>CC</sub> V <sub>CC</sub> = 5V ± 10%
I <sub>SB2</sub>	V <sub>CC</sub> Standby Current		50	µA	SCL = SDA = V <sub>CC</sub> V <sub>CC</sub> = 3V
I <sub>LI</sub>	Input Leakage Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> (1)	Input Low Voltage	–1.0	V <sub>CC</sub> x 0.3	V	
V <sub>IH</sub> (1)	Input High Voltage	V <sub>CC</sub> x 0.7	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> – 0.8		V	I <sub>OH</sub> = 1.0 mA
V <sub>PGM</sub>	Program Enable Voltage	12	15	V	

3830 PGM T04

CAPACITANCE T<sub>A</sub> = 25°C, f = 1.0 MHz, V<sub>CC</sub> = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C <sub>I/O</sub> (2)	Input/Output Capacitance (SDA)	8	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (2)	Input Capacitance (SCL)	6	pF	V <sub>IN</sub> = 0V

3830 PGM T05

Notes: (1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.



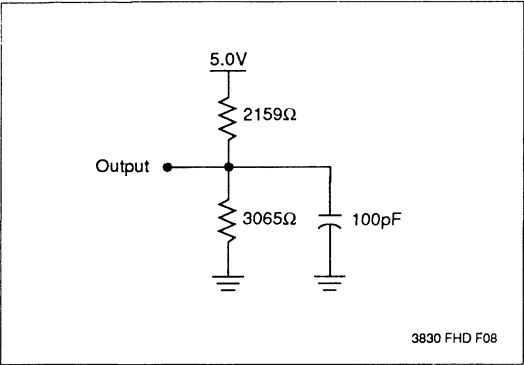
# X24001

## POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(3)}$	Power-up to Read Operation	2	ms
$t_{PUW}^{(3)}$	Power-up to Write Operation	5	ms

3830 PGM T06

## EQUIVALENT A.C. LOAD CIRCUIT



3830 FHD F08

## A.C. CONDITIONS OF TEST

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$

3830 PGM T07

## A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

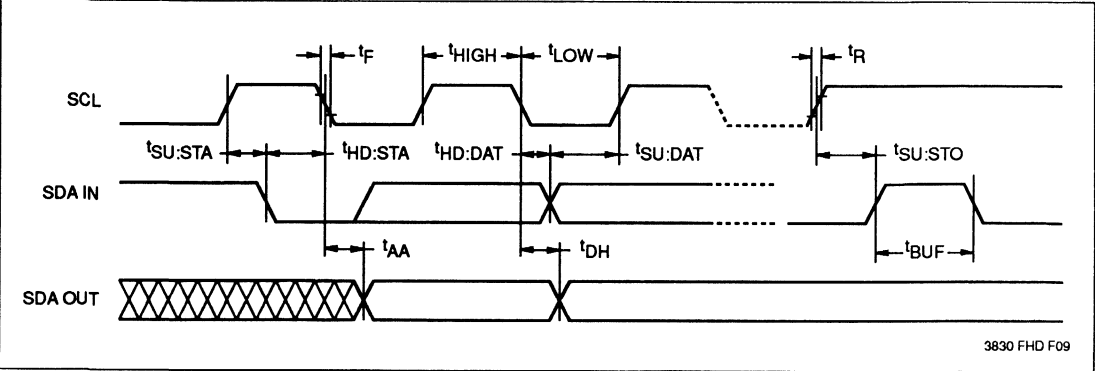
### Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
$f_{SCL}$	SCL Clock Frequency	0	1	MHz
$t_{AA}$	SCL Low to SDA Data Out Valid		350	ns
$t_{BUF}$	Time the Bus Must Be Free Before a New Transmission Can Start	500		ns
$t_{HD:STA}$	Start Condition Hold Time	250		ns
$t_{LOW}$	Clock Low Period	500		ns
$t_{HIGH}$	Clock High Period	500		ns
$t_{SU:STA}$	Start Condition Setup Time	250		ns
$t_{HD:DAT}$	Data In Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	250		ns
$t_R$	SDA and SCL Rise Time		1	μs
$t_F$	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	250		ns
$t_{DH}$	Data Out Hold Time	50		ns

3830 PGM T08

X24001

Bus Timing



3830 FHD F09

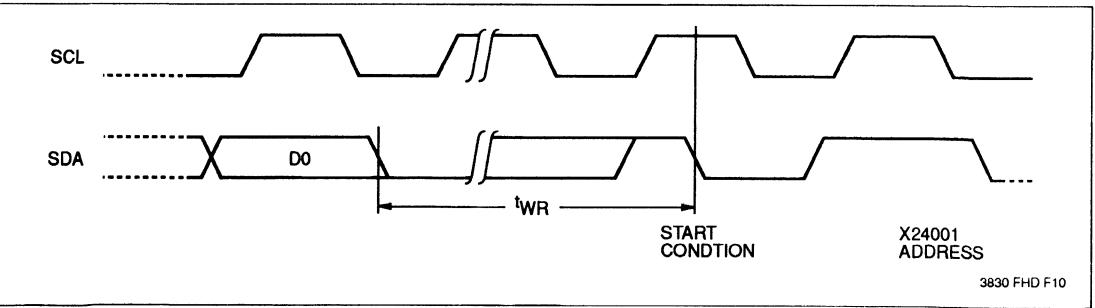
2

WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Max.	Units
$t_{WR}^{(4)}$	Write Cycle Time		5	ms

3830 PGM T09

Write Cycle Timing



3830 FHD F10

- Note:** (3)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.
- (4) The write cycle time is the time from the initiation of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24001 bus interface circuits are disabled, SDA is high impedance, and the device does not respond to start conditions.

**X24001**

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**NOTES**



## Preliminary Information

1K

X24C01

128 x 8 Bit

## Serial E<sup>2</sup>PROM

### FEATURES

- 3V to 5.5V Power Supply
- Low Power CMOS
  - Active Current Less Than 1 mA
  - Standby Current Less Than 50  $\mu$ A
- Internally Organized 128 x 8
- 2 Wire Serial Interface
  - Bidirectional Data Transfer Protocol
- Four Byte Page Write Mode
- Self Timed Write Cycle
  - Typical Write Cycle Time of 5 ms
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 100 Years
- 8-Pin Mini-DIP and 8-PIN SOIC Packages

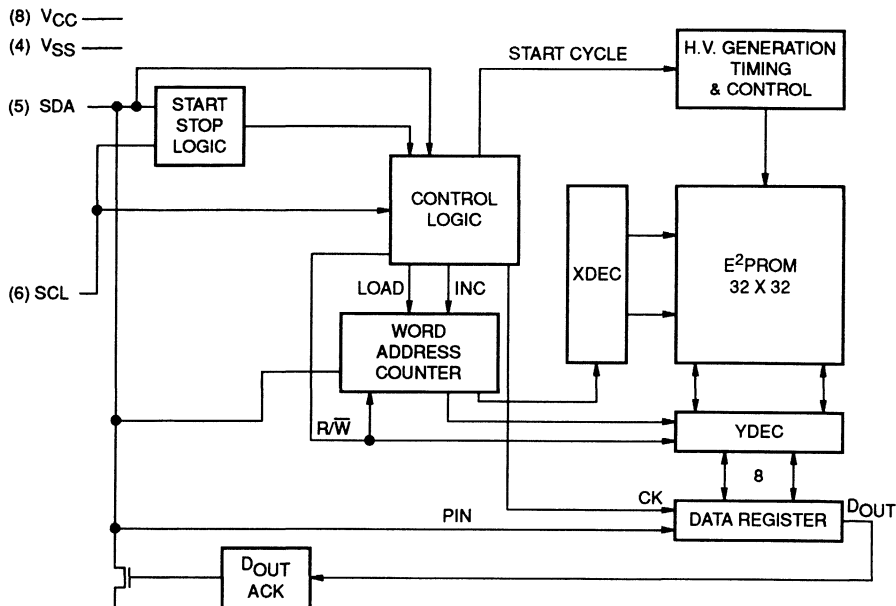
### DESCRIPTION

The X24C01 is a CMOS 1024 bit serial E<sup>2</sup>PROM, internally organized as 128 x 8. The X24C01 features a serial interface and software protocol allowing operation on a simple two wire bus.

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

2

### FUNCTIONAL DIAGRAM



3837 FHD F01

# X24C01

## PIN DESCRIPTIONS

### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

### Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

## PIN NAMES

Symbol	Description
NC	No Connect
V <sub>SS</sub>	Ground
V <sub>CC</sub>	Supply Voltage
SDA	Serial Data
SCL	Serial Clock

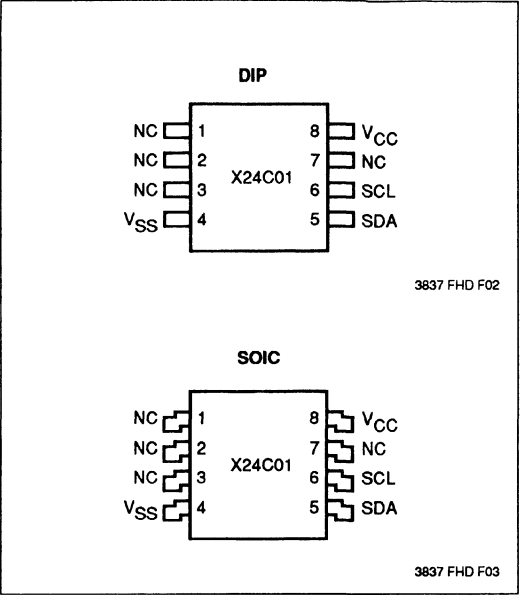
3837 PGM T01

## A.C. CONDITIONS OF TEST

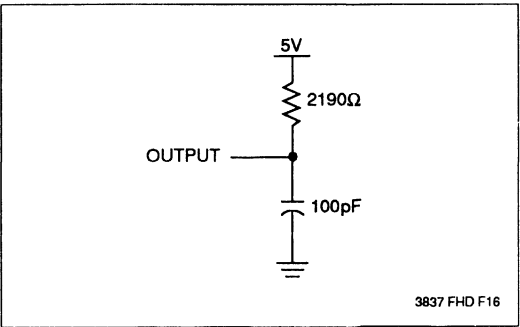
Input Pulse Levels	V <sub>CC</sub> x 0.1 to V <sub>CC</sub> x 0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V <sub>CC</sub> x 0.5

3837 PGM T02

## PIN CONFIGURATION



## EQUIVALENT A.C. LOAD CIRCUIT



# X24C01

## DEVICE OPERATION

The X24C01 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X24C01 will be considered a slave in all applications.

## Clock and Data Conventions

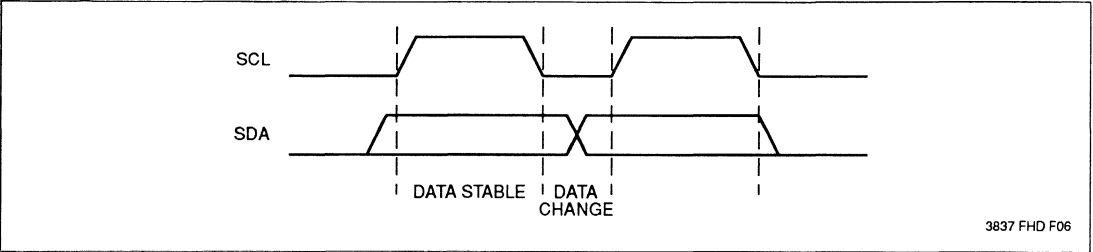
Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

## Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C01 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

2

Figure 1. Data Validity



# X24C01

## Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24C01 to place the device in the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

## Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C01 will respond with an acknowledge after recognition of a start condition, a seven bit word address and a R/W bit. If a write operation has been selected, the X24C01 will respond with an acknowledge after each byte of data is received.

In the read mode the X24C01 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24C01 will continue to transmit data. If an acknowledge is not detected, the X24C01 will terminate further data transmissions. The master must then issue a stop condition to return the X24C01 to the standby power mode and place the device into a known state.

Figure 2. Definition of Start and Stop

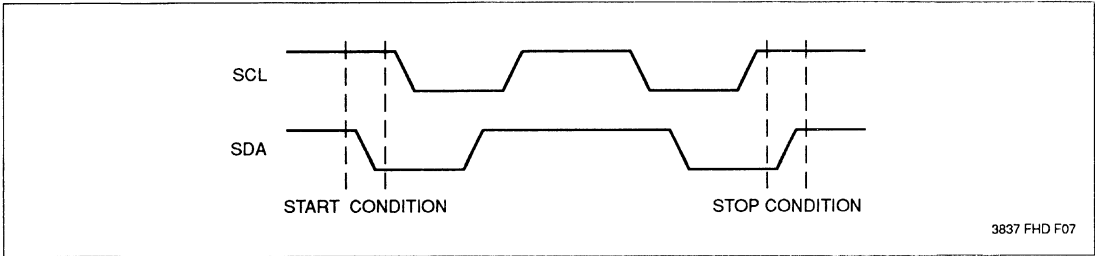
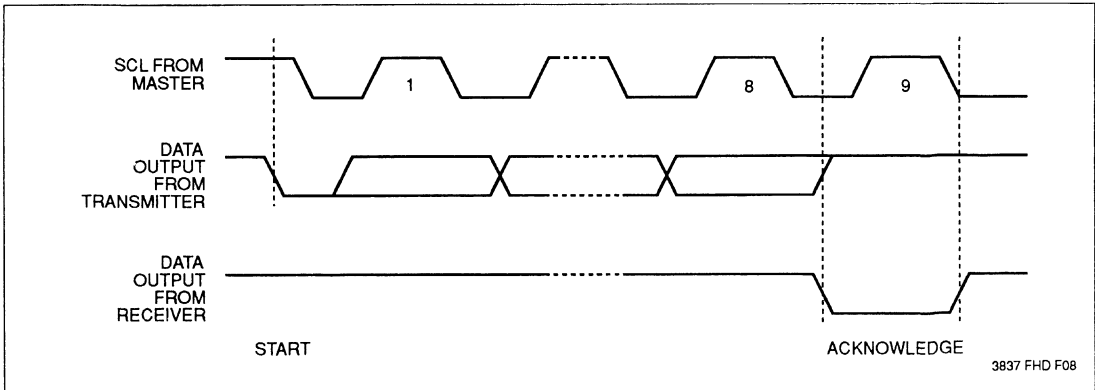


Figure 3. Acknowledge Response From Receiver



# X24C01

## WRITE OPERATIONS

### Byte Write

To initiate a write operation, the master sends a start condition followed by a seven bit word address and a write bit. The X24C01 responds with an acknowledge, then waits for eight bits of data and then responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24C01 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress, the X24C01 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 4 for the address, acknowledge and data transfer sequence.

### Page Write

The most significant five bits of the word address define

the page address. The X24C01 is capable of a four byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the transfer of data after the first data byte, the master can transmit up to three more bytes. After the receipt of each data byte, the X24C01 will respond with an acknowledge.

After the receipt of each data byte, the two low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than four data bytes prior to generating the stop condition, the address counter will "roll over" and the previously transmitted data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

2

Figure 4. Byte Write

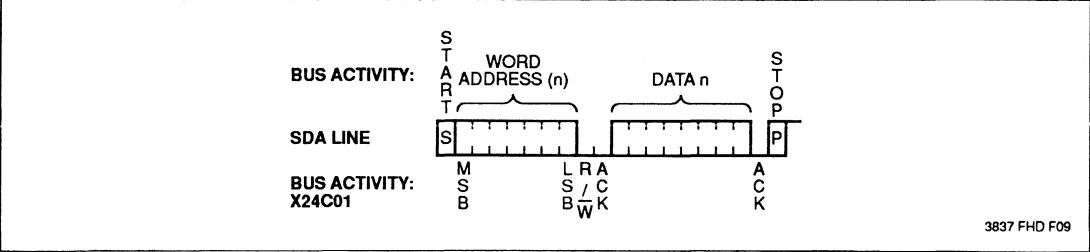
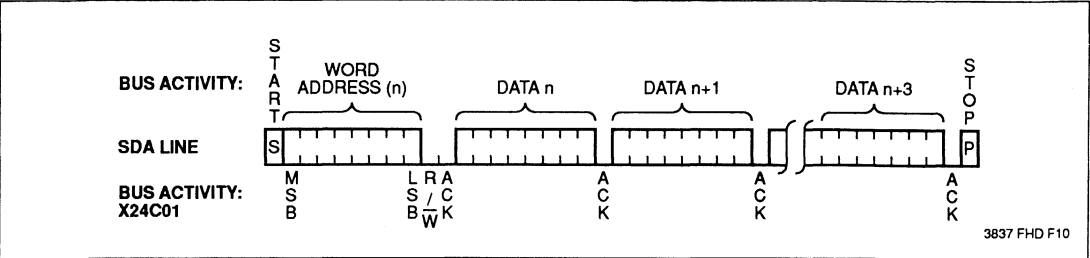


Figure 5. Page Write





## X24C01

### Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24C01 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the word address for a **write operation**. If the X24C01 is still busy with the write operation no ACK will be returned. If the X24C01 has completed the write operation an ACK will be returned and the controller can then proceed with the next read or write operation.

### READ OPERATIONS

Read operations are initiated in the same manner as write operations with exception that the  $R/\bar{W}$  bit of the word address is set to a one. There are two basic read operations: byte read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

#### Byte Read

To initiate a read operation, the master sends a start condition followed by a seven bit word address and a read bit. The X24C01 responds with an acknowledge and then transmits the eight bits of data. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the start, word address, read bit, acknowledge and data transfer sequence.

Figure 6. ACK Polling Sequence

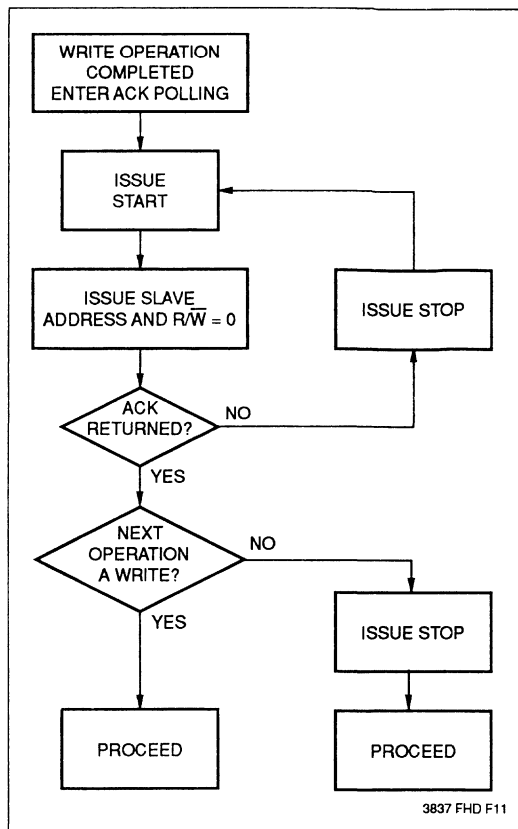
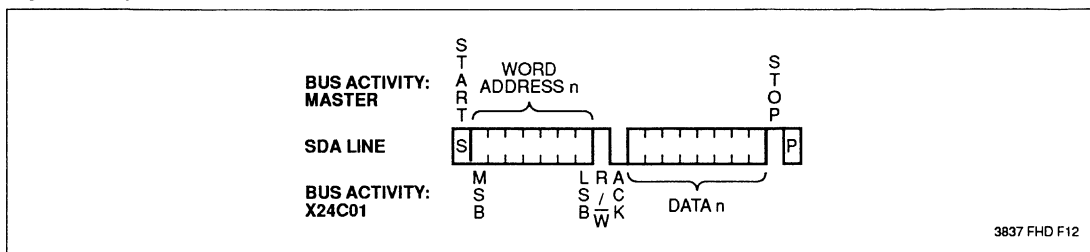


Figure 7. Byte Read



# X24C01

## Sequential Read

Sequential read is initiated in the same manner as the byte read. The first data byte is transmitted as with the byte read mode, however, the master now responds with an acknowledge, indicating it requires additional data. The X24C01 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition.

The data output is sequential, with the data from address  $n$  followed by the data from  $n + 1$ . The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 127) the counter "rolls over" to zero and the X24C01 continues to output data for each acknowledge received. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

2

Figure 8. Sequential Read

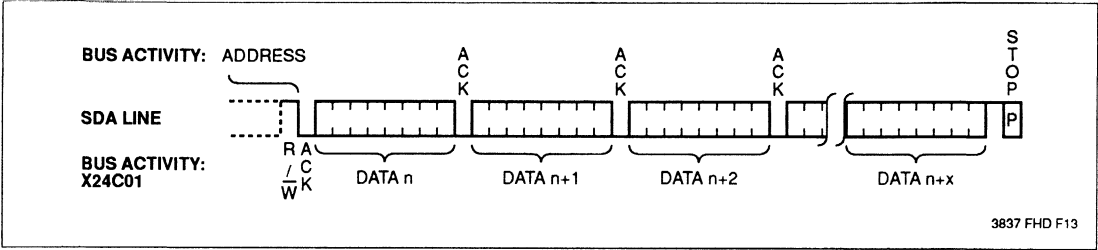
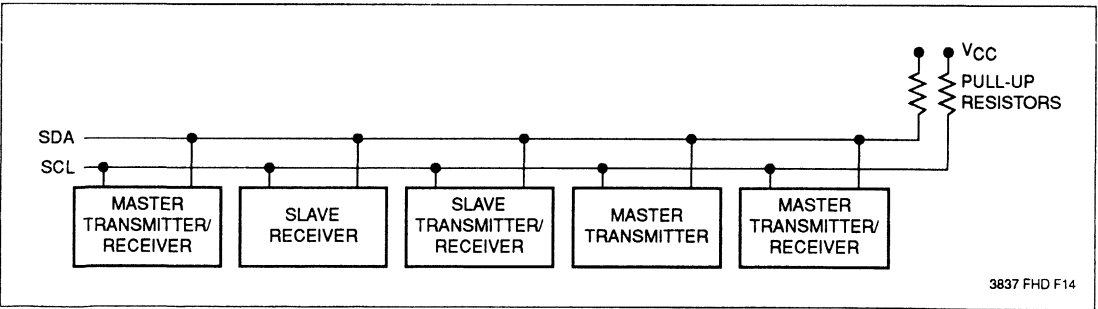


Figure 9. Typical System Configuration



# X24C01

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	-65°C to +135°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin with Respect to V <sub>SS</sub> .....	-1.0V to +7.0V
D.C. Output Current .....	5 mA
Lead Temperature (Soldering, 10 Seconds) .....	300°C

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

Supply Voltage	Limits
X24C01	4.5V to 5.5V
X24C01-3.5	3.5V to 5.5V
X24C01-3	3.0V to 5.5V

## D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub> (1)	V <sub>CC</sub> Supply Current (Read)		1	mA	SCL = V <sub>CC</sub> x 0.1/V <sub>CC</sub> x 0.9 Levels @ 100 KHz, SDA = Open
I <sub>CC</sub> (2)	V <sub>CC</sub> Supply Current (Write)		2		
I <sub>SB1</sub> (1)	V <sub>CC</sub> Standby Current		100	μA	SCL = SDA = V <sub>CC</sub> , V <sub>CC</sub> = 5V ± 10%
I <sub>SB2</sub> (1)	V <sub>CC</sub> Standby Current		50	μA	SCL = SDA = V <sub>CC</sub> , V <sub>CC</sub> = 3V
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> (2)	Input Low Voltage	-1.0	V <sub>CC</sub> x 0.3	V	
V <sub>IH</sub> (2)	Input High Voltage	V <sub>CC</sub> x 0.7	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2.1 mA

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## CAPACITANCE T<sub>A</sub> = 25°C, f = 1.0 MHz, V<sub>CC</sub> = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C <sub>I/O</sub> (3)	Input/Output Capacitance (SDA)	8	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (3)	Input Capacitance (SCL)	6	pF	V <sub>IN</sub> = 0V

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- Notes:** (1) Must perform a stop command prior to measurement.  
 (2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
 (3) This parameter is periodically sampled and not 100% tested.

**X24C01**

**A.C. CHARACTERISTICS** (Over recommended operating conditions, unless otherwise specified)

## Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f <sub>SCL</sub>	SCL Clock Frequency	0	100	KHz
T <sub>I</sub>	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t <sub>AA</sub>	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t <sub>BUF</sub>	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		μs
t <sub>HD:STA</sub>	Start Condition Hold Time	4.0		μs
t <sub>LOW</sub>	Clock Low Period	4.7		μs
t <sub>HIGH</sub>	Clock High Period	4.0		μs
t <sub>SU:STA</sub>	Start Condition Setup Time	4.7		μs
t <sub>HD:DAT</sub>	Data In Hold Time	0		μs
t <sub>SU:DAT</sub>	Data In Setup Time	250		ns
t <sub>R</sub>	SDA and SCL Rise Time		1	μs
t <sub>F</sub>	SDA and SCL Fall Time		300	ns
t <sub>SU:STO</sub>	Stop Condition Setup Time	4.7		μs
t <sub>OH</sub>	Data Out Hold Time	300		ns

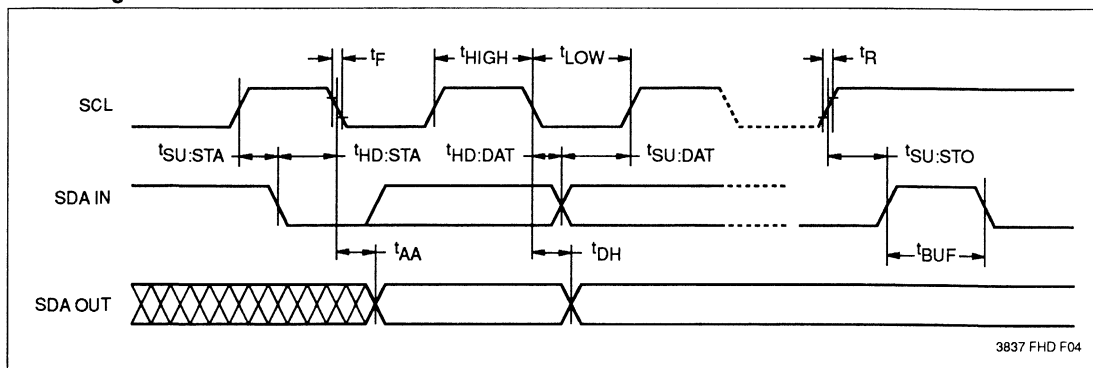
3837 PGM T06

## POWER-UP TIMING

Symbol	Parameter	Max.	Units
t <sub>PUR</sub> <sup>(4)</sup>	Power-up to Read Operation	1	ms
t <sub>PW</sub> <sup>(4)</sup>	Power-up to Write Operation	5	ms

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## Bus Timing



**Note:** (4)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

# X24C01

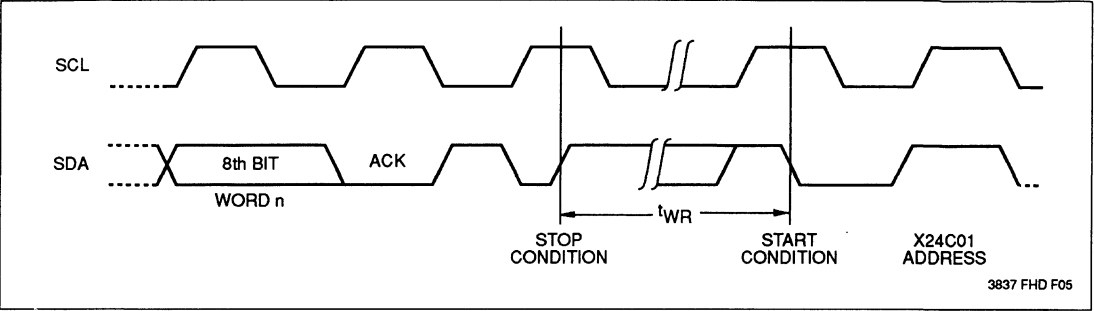
## WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
$t_{WR}^{(6)}$	Write Cycle Time		5	10	ms

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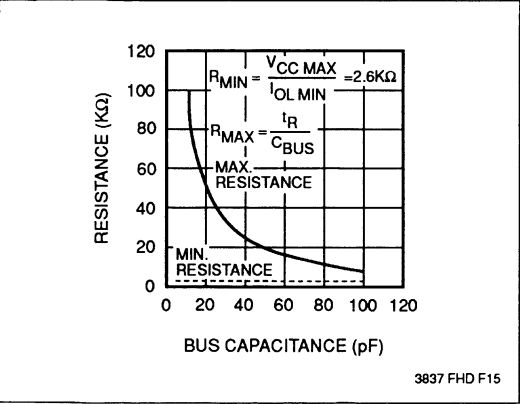
The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C01 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its word address.

## Write Cycle Timing



- Notes:** (5) Typical values are for  $T_A = 25^{\circ}\text{C}$  and nominal supply voltage (5V).  
 (6)  $t_{WR}$  is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

## Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance



## Preliminary Information

1K

X24C01A

128 x 8 Bit

## Serial E<sup>2</sup>PROM

### FEATURES

- 2.7V to 5.5V Power Supply
- Low Power CMOS
  - Active Current Less Than 1 mA
  - Standby Current Less Than 50  $\mu$ A
- Internally Organized 128 x 8
- Self Timed Write Cycle
  - Typical Write Cycle Time of 5 ms
- 2 Wire Serial Interface
  - Bidirectional Data Transfer Protocol
- Four Byte Page Write Operation
  - Minimizes Total Write Time Per Byte
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 100 Years
- New Hardwire – Write Control Function

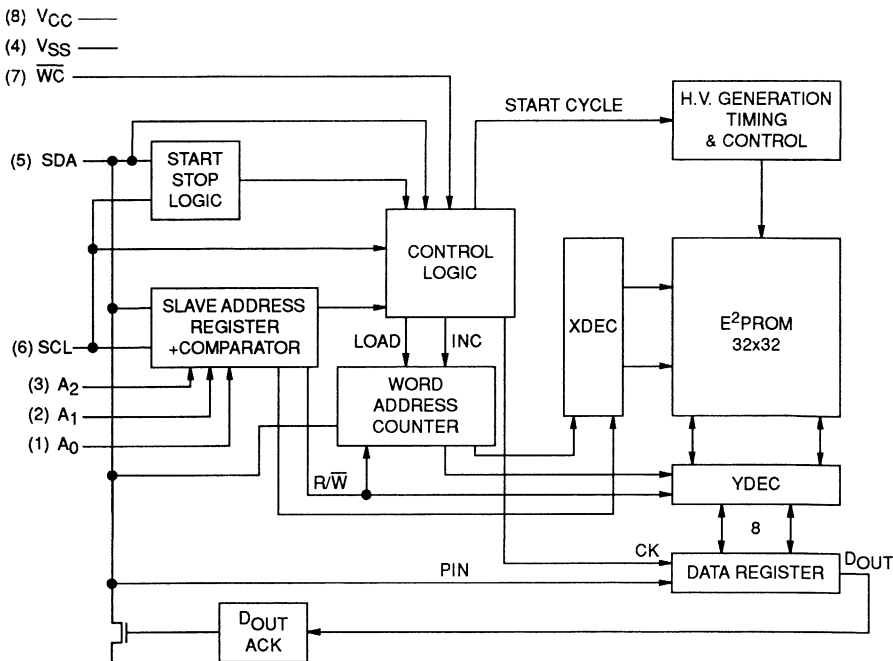
### DESCRIPTION

The X24C01A is a CMOS 1024 bit serial E<sup>2</sup>PROM, internally organized 128 x 8. The X24C01A features a serial interface and software protocol allowing operation on a simple two wire bus. Three address inputs allow up to eight devices to share a common two wire bus.

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years. Available in an eight pin DIP and SOIC package.

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### FUNCTIONAL DIAGRAM



3841 FHD F01

# X24C01A

## PIN DESCRIPTIONS

### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

### Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

### Address (A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub>)

The address inputs are used to set the least significant three bits of the seven bit slave address. These inputs can be static or actively driven. If used statically they must be tied to V<sub>SS</sub> or V<sub>CC</sub> as appropriate. If actively driven, they must be driven to V<sub>SS</sub> or to V<sub>CC</sub>.

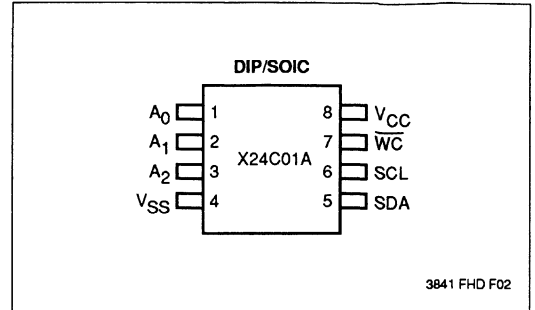
### WRITE CONTROL ( $\overline{WC}$ )

The Write Control input controls the ability to write to the device. When  $\overline{WC}$  is LOW (tied to V<sub>SS</sub>) the X24C01A will be enabled to perform write operations. When  $\overline{WC}$  is HIGH (tied to V<sub>CC</sub>) the internal high voltage circuitry will be disabled and all writes will be disabled.

## DEVICE OPERATION

The X24C01A supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X24C01A will be considered a slave in all applications.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
A <sub>0</sub> -A <sub>2</sub>	Address Inputs
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V <sub>SS</sub>	Ground
V <sub>CC</sub>	+5V

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## Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

### Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C01A continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

# X24C01A

Figure 1. Data Validity

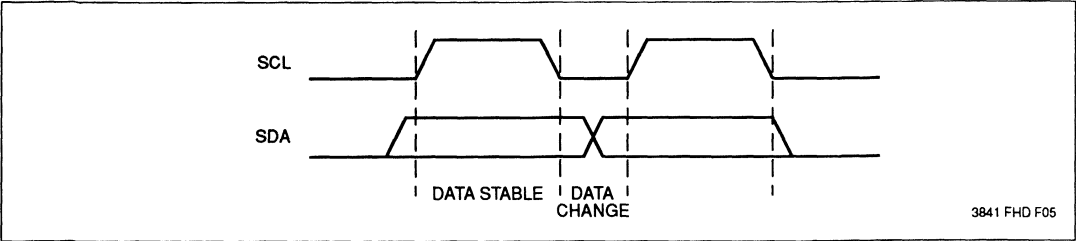
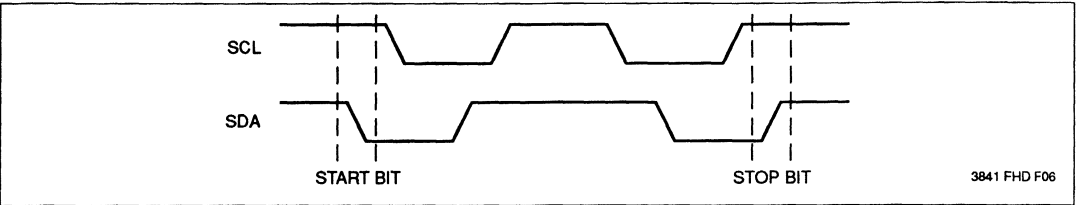


Figure 2. Definition of Start and Stop



## Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24C01A to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

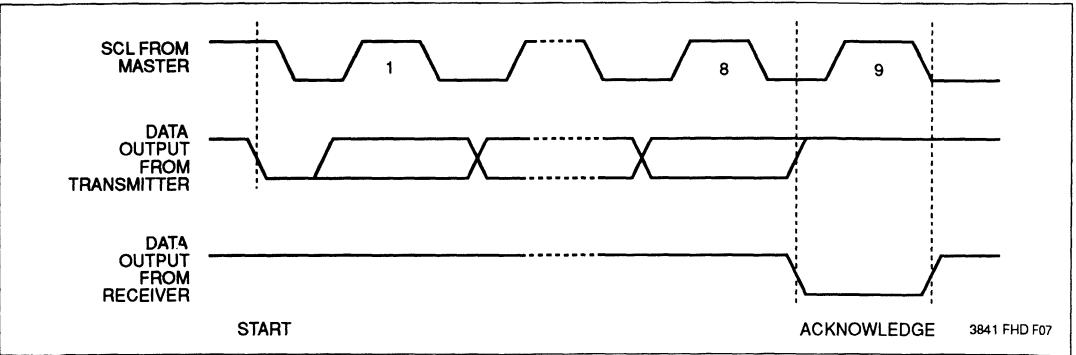
## Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C01A will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24C01A will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24C01A will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24C01A will continue to transmit data. If an acknowledge is not detected, the X24C01A will terminate further data transmissions. The master must then issue a stop condition to return the X24C01A to the standby power mode and place the device into a known state.

Figure 3. Acknowledge Response From Receiver



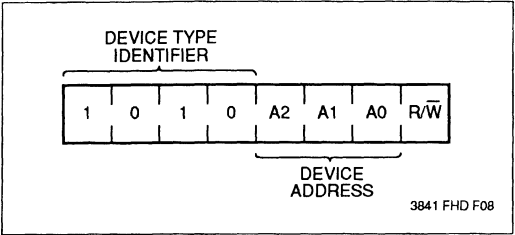


# X24C01A

## DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X24C01A this is fixed as 1010[B].

Figure 4. Slave Address



The next three significant bits address a particular device. A system could have up to eight X24C01A devices on the bus (see Figure 10). The eight addresses are defined by the state of the A<sub>0</sub>, A<sub>1</sub> and A<sub>2</sub> inputs.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

Figure 5. Byte Write

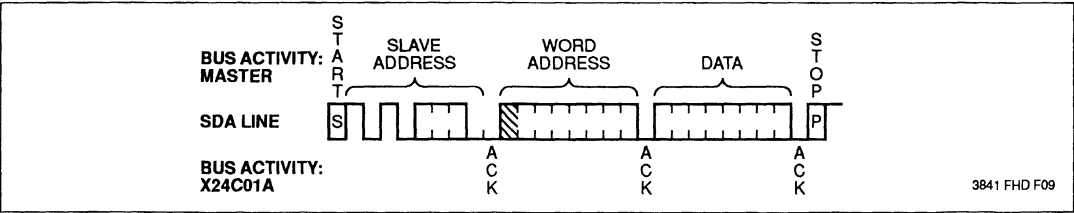
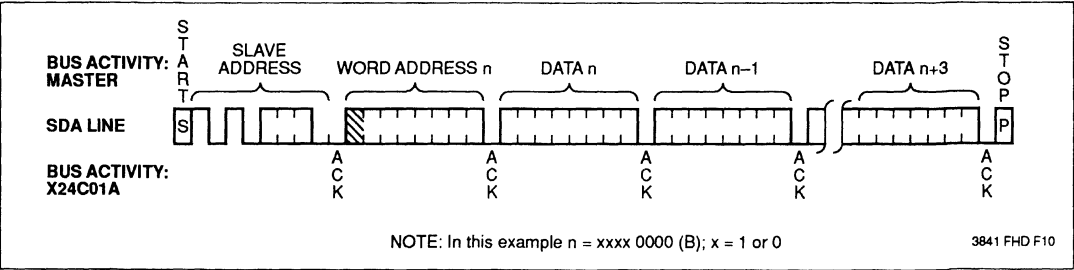


Figure 6. Page Write



Following the start condition, the X24C01A monitors the SDA bus comparing the slave address being transmitted with its slave address (device type and state of A<sub>0</sub>, A<sub>1</sub> and A<sub>2</sub> inputs). Upon a correct compare the X24C01A outputs an acknowledge on the SDA line. Depending on the state of the R/W bit, the X24C01A will execute a read or write operation.

## WRITE OPERATIONS

### Byte Write

For a write operation, the X24C01A requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 128 words of memory. Note: the most significant bit is a don't care. Upon receipt of the word address the X24C01A responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24C01A begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24C01A inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

## X24C01A

### Page Write

The X24C01A is capable of an four byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to three more words. After the receipt of each word, the X24C01A will respond with an acknowledge.

After the receipt of each word, the two low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than four words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

### Acknowledge Polling

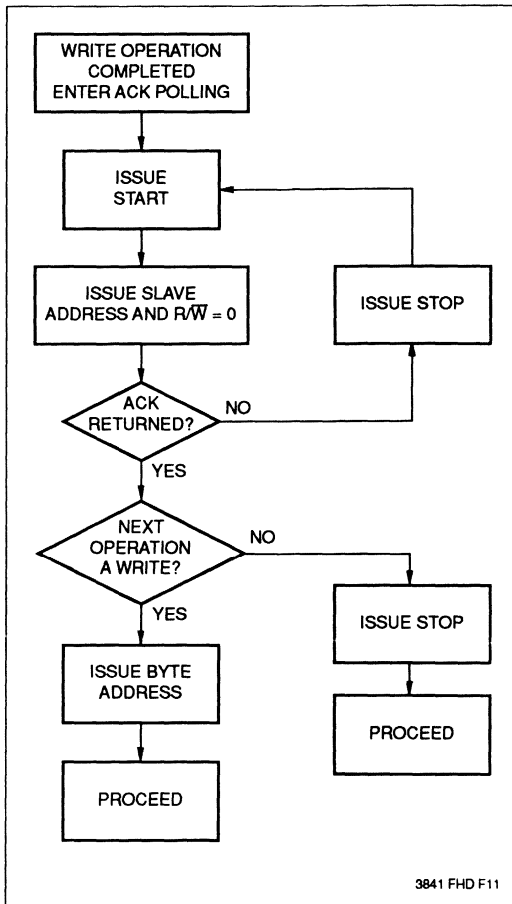
The disabling of the inputs, during the internal write operation, can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24C01A initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X24C01A is still busy with the write operation no ACK will be returned. If the X24C01A has completed the write operation an ACK will be returned and the master can then proceed with the next read or write operation (See Flow 1).

### READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/W bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Flow 1. ACK Polling Sequence



# X24C01A

## Current Address Read

Internally the X24C01A contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address  $n$ , the next read operation would access data from address  $n + 1$ . Upon receipt of the slave address with  $\overline{R/\overline{W}}$  set to one, the X24C01A issues an acknowledge and transmits the eight bit word during the next eight clock cycles. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

## Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the  $\overline{R/\overline{W}}$  bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the  $\overline{R/\overline{W}}$  bit set to one. This will be followed by an acknowledge from the X24C01A and then by the eight bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 7. Current Address Read

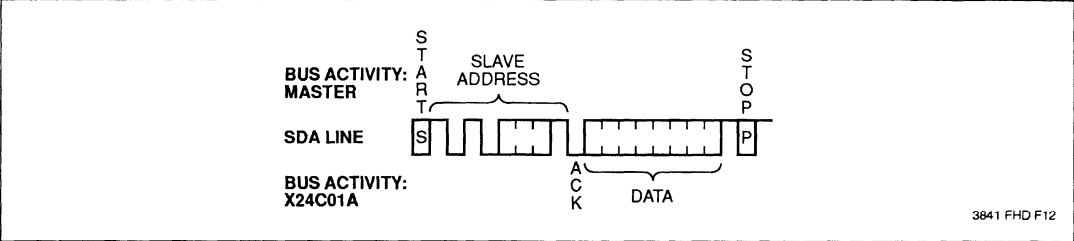
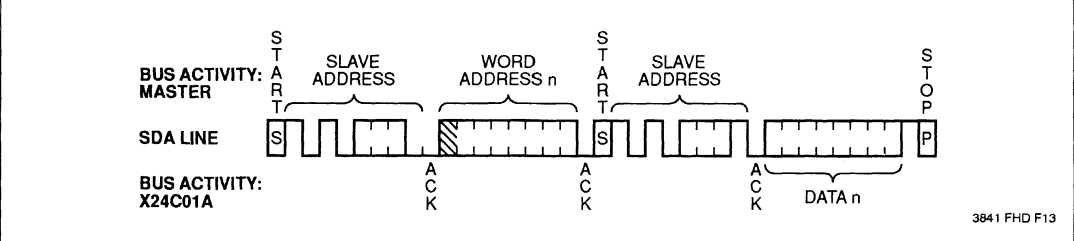


Figure 8. Random Read



# X24C01A

## Sequential Read

Sequential Read can be initiated as either a current address read or random access read. The first word is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24C01A continues to output data for each acknowledge received. The read operation is terminated by the master, by not responding with an acknowledge and by issuing a stop condition.

The data output is sequential, with the data from address  $n$  followed by the data from  $n + 1$ . The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 127), the counter "rolls over" to address 0 and the X24C01A continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

2

Figure 9. Sequential Read

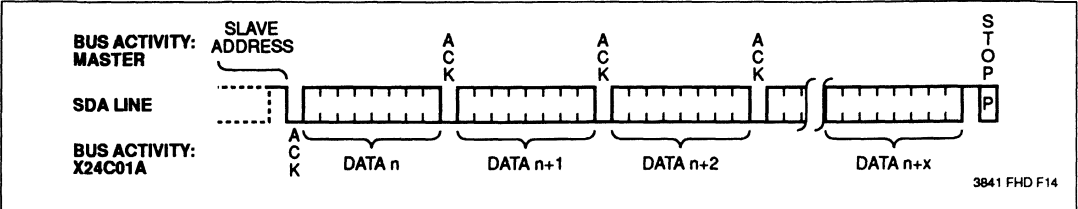
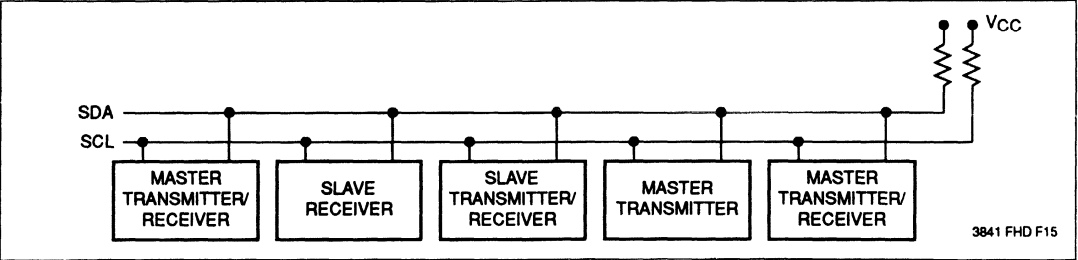


Figure 10. Typical System Configuration



# X24C01A

### ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	–65°C to +135°C
Storage Temperature .....	–65°C to +150°C
Voltage on any Pin with Respect to V <sub>SS</sub> .....	–1.0V to +7V
D.C. Output Current .....	5 mA
Lead Temperature (Soldering, 10 Seconds) .....	300°C

### \*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

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Supply Voltage	Limits
X24C01A	4.5V to 5.5V
X24C01A-3.5	3.5V to 5.5V
X24C01A-3	3V ± 5.5V
X24C01A-2.7	2.7V to 5.5V

3841 PGM T03

### D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC1</sub>	Power Supply Current (read)		1	mA	SCL = V <sub>CC</sub> x 0.1/V <sub>CC</sub> x 0.9 Levels @ 100 KHz, SDA = Open, All Other Inputs = GND or V <sub>CC</sub> – 0.3V
I <sub>CC2</sub>	Power Supply Current (write)		2	mA	SCL = V <sub>CC</sub> x 0.1/V <sub>CC</sub> x 0.9 Levels @ 100 KHz, SDA = Open, All Other Inputs = GND or V <sub>CC</sub> – 0.3V
I <sub>SB</sub> (1)	Standby Current		50	µA	SCL = SDA = V <sub>CC</sub> – 0.3V, All Other Inputs = GND or V <sub>CC</sub> , V <sub>CC</sub> = 5.5V
I <sub>SB</sub> (1)	Standby Current		30	µA	SCL = SDA = V <sub>CC</sub> – 0.3V, All Other Inputs = GND or V <sub>CC</sub> , V <sub>CC</sub> = 3.3V + 10%
I <sub>LI</sub>	Input Leakage Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> (2)	Input Low Voltage	–1.0	V <sub>CC</sub> x 0.3	V	
V <sub>IH</sub> (2)	Input High Voltage	V <sub>CC</sub> x 0.7	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 3 mA

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### CAPACITANCE T<sub>A</sub> = 25°C, f = 1.0MHZ, V<sub>CC</sub> = 5V

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (3)	Input/Output Capacitance (SDA)	8	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (3)	Input Capacitance (A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , SCL, WC)	6	pF	V <sub>IN</sub> = 0V

3841 PGM T06

- Notes:** (1) Must perform a stop command prior to measurement.  
(2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
(3) This parameter is periodically sampled and not 100% tested.

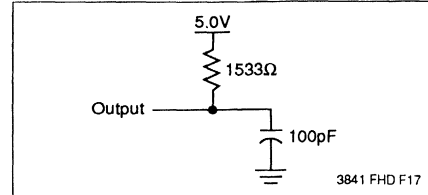
# X24C01A

## A.C. CONDITIONS OF TEST

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
Input and Output Timing Levels	$V_{CC} \times 0.5$

3841 PGM T07

## EQUIVALENT A.C. LOAD CIRCUIT



## A.C. CHARACTERISTICS LIMITS (Over recommended operating conditions unless otherwise specified)

### Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
$f_{SCL}$	SCL Clock Frequency	0	100	KHz
$T_I$	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
$t_{AA}$	SCL Low to SDA Data Out Valid	0.3	3.5	$\mu$ s
$t_{BUF}$	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		$\mu$ s
$t_{HD:STA}$	Start Condition Hold Time	4.0		$\mu$ s
$t_{LOW}$	Clock Low Period	4.7		$\mu$ s
$t_{HIGH}$	Clock High Period	4.0		$\mu$ s
$t_{SU:STA}$	Start Condition Setup Time	4.7		$\mu$ s
$t_{HD:DAT}$	Data In Hold Time	0		$\mu$ s
$t_{SU:DAT}$	Data In Setup Time	250		ns
$t_R$	SDA and SCL Rise Time		1	$\mu$ s
$t_F$	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		$\mu$ s
$t_{DH}$	Data Out Hold Time	300		ns

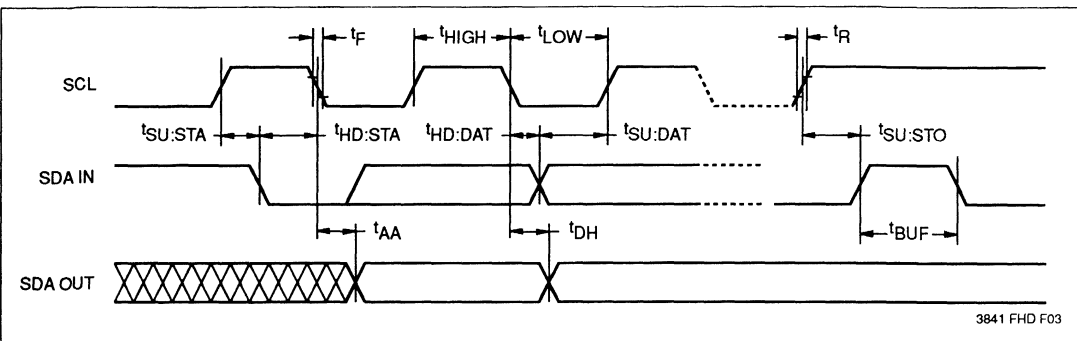
3841 PGM T08

## POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(4)}$	Power-Up to Read Operation	1	ms
$t_{PUW}^{(4)}$	Power-Up to Write Operation	5	ms

3841 PGM T09

## Bus Timing



**Note:** (4)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

X24C01A

WRITE CYCLE LIMITS

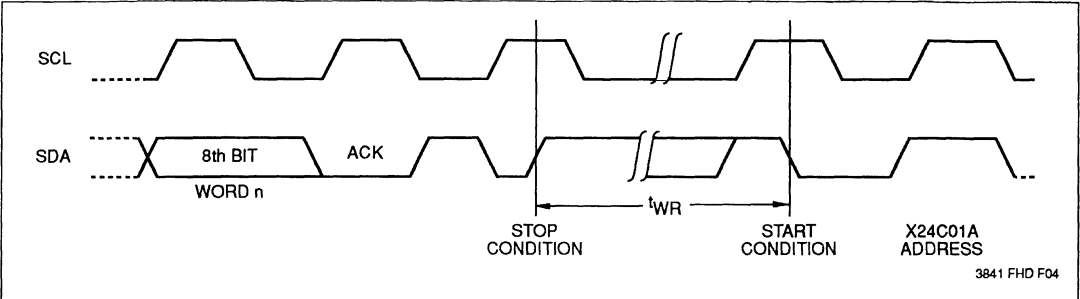
Symbol	Parameter	Min.	Typ. <sup>(5)</sup>	Max.	Units
t <sub>WR</sub> <sup>(6)</sup>	Write Cycle Time		5	10	ms

3841 PGM T10

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C01A

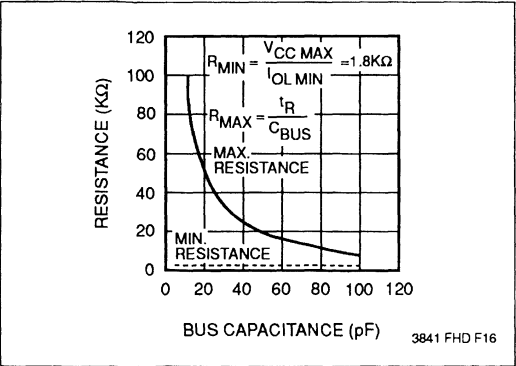
bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Write Cycle Timing



**Notes:** (5) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage (5V).  
(6) t<sub>WR</sub> is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

1K

**X24012**

128 x 8 Bit

**Serial E<sup>2</sup>PROM**

**FEATURES**

- 2.7 to 5.5V Power Supply
- Low Power CMOS
  - Active Current Less Than 1 mA
  - Standby Current Less Than 50  $\mu$ A
- Internally Organized 128 x 8
- Self Timed Write Cycle
  - Typical Write Cycle Time of 5 ms
- 2 Wire Serial Interface
  - Bidirectional Data Transfer Protocol
- Four Byte Page Write Operation
  - Minimizes Total Write Time Per Byte
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 100 Years

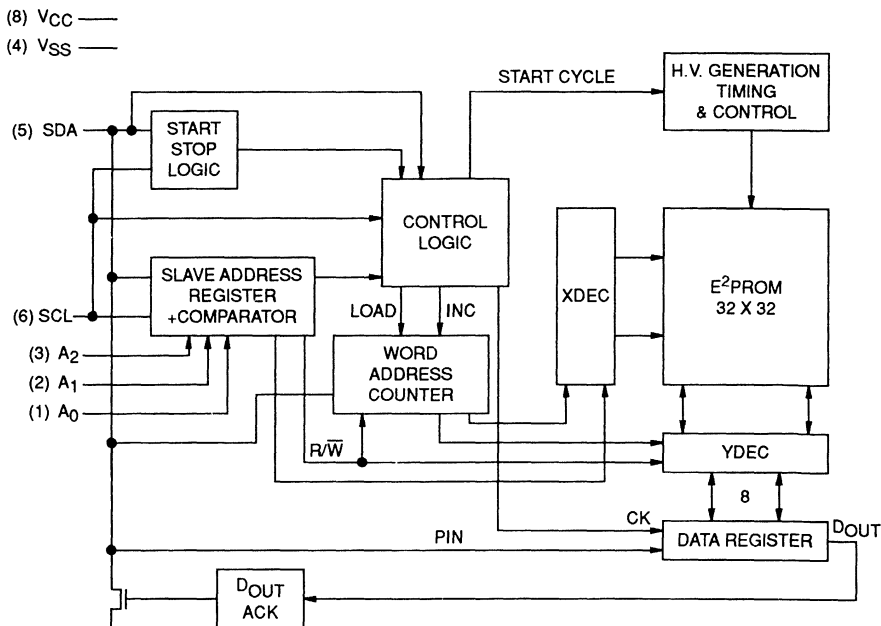
**DESCRIPTION**

The X24012 is a CMOS 1024 bit serial E<sup>2</sup>PROM, internally organized as one 128 x 8 bank. The X24012 features a serial interface and software protocol allowing operation on a simple two wire bus. Three address inputs allow up to eight devices to share a common two wire bus.

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years. The X24012 is available in eight pin DIP and SOIC packages.

2

**FUNCTIONAL DIAGRAM**



3847 FHD F01



# X24012

## PIN DESCRIPTIONS

### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

### Serial Data (SDA)

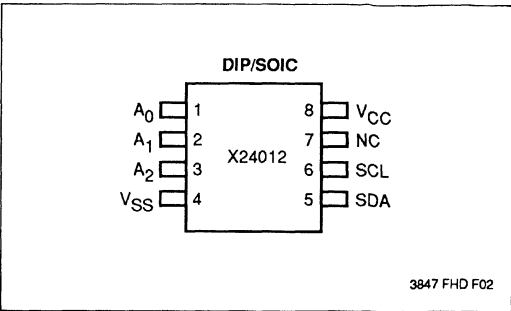
SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

### Address (A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub>)

The address inputs are used to set the least significant three bits of the seven bit slave address. These inputs can be static or actively driven. If used statically they must be tied to V<sub>SS</sub> or V<sub>CC</sub> as appropriate. If actively driven, they must be driven to V<sub>SS</sub> or to V<sub>CC</sub>.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
A <sub>0</sub> -A <sub>2</sub>	Address Inputs
SDA	Serial Data
SCL	Serial Clock
NC	No Connect
V <sub>SS</sub>	Ground
V <sub>CC</sub>	+5V

3847 PGM T01

# X24012

## DEVICE OPERATION

The X24012 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X24012 will be considered a slave in all applications.

## Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

## Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24012 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

2

Figure 1. Data Validity

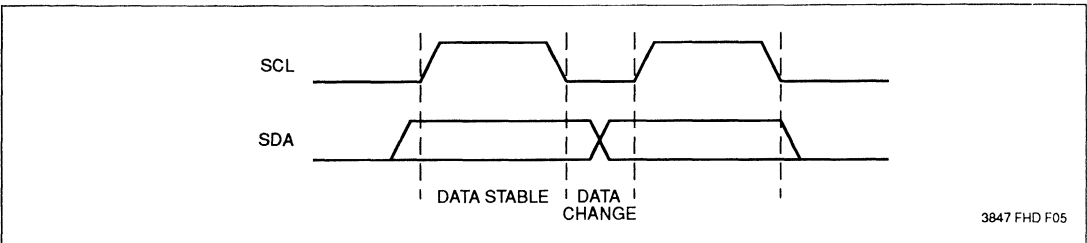
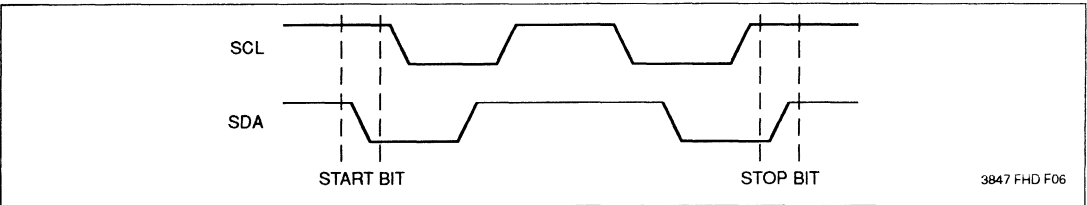


Figure 2. Definition of Start and Stop



# X24012

## Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24012 to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

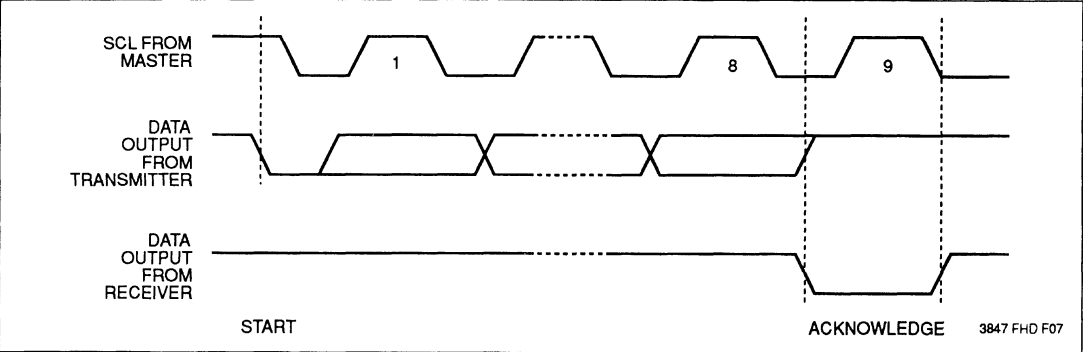
## Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24012 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24012 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24012 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24012 will continue to transmit data. If an acknowledge is not detected, the X24012 will terminate further data transmissions. The master must then issue a stop condition to return the X24012 to the standby power mode and place the device into a known state.

Figure 3. Acknowledge Response From Receiver

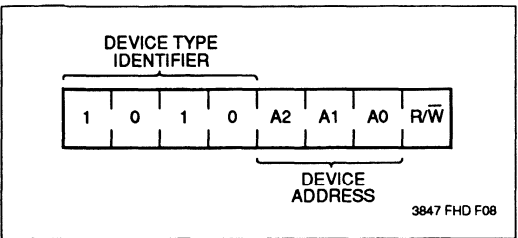


# X24012

## DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X24012 this is fixed as 1010[B].

Figure 4. Slave Address



The next three significant bits address a particular device. A system could have up to eight X24012 devices on the bus (see Figure 10). The eight addresses are defined by the state of the  $A_0$ ,  $A_1$  and  $A_2$  inputs.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

Figure 5. Byte Write

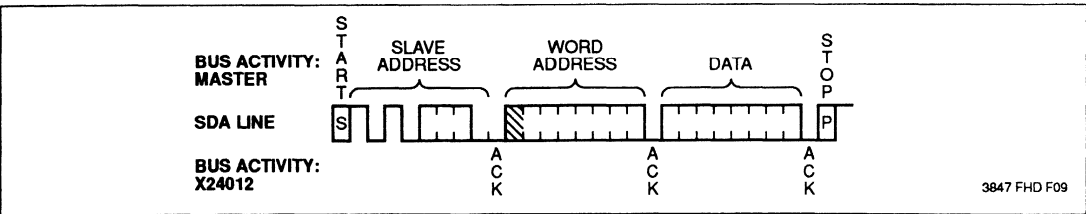
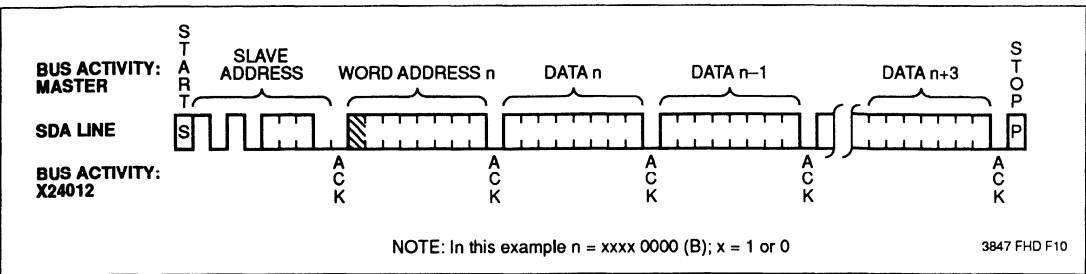


Figure 6. Page Write



Following the start condition, the X24012 monitors the SDA bus comparing the slave address being transmitted with its slave address (device type and state of  $A_0$ ,  $A_1$  and  $A_2$  inputs). Upon a correct compare the X24012 outputs an acknowledge on the SDA line. Depending on the state of the R/W bit, the X24012 will execute a read or write operation.

## WRITE OPERATIONS

### Byte Write

For a write operation, the X24012 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 128 words of memory. Note: the most significant bit is a don't care. Upon receipt of the word address the X24012 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24012 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24012 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

## X24012

### Page Write

The X24012 is capable of an four byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to three more words. After the receipt of each word, the X24012 will respond with an acknowledge.

After the receipt of each word, the two low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than four words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

### Acknowledge Polling

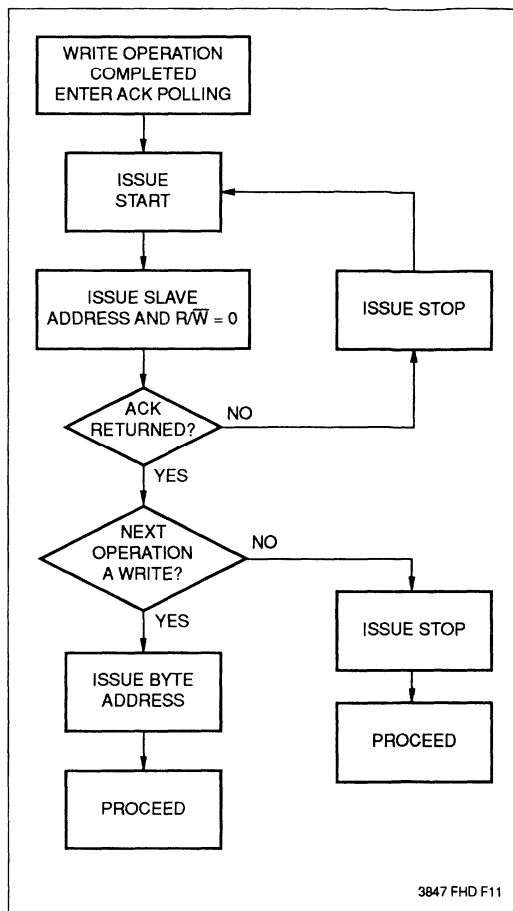
The disabling of the inputs, during the internal write operation, can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24012 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X24012 is still busy with the write operation no ACK will be returned. If the X24012 has completed the write operation an ACK will be returned and the master can then proceed with the next read or write operation (See Flow 1).

### READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/W bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Flow 1. ACK Polling Sequence



# X24012

## Current Address Read

Internally the X24012 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address  $n$ , the next read operation would access data from address  $n + 1$ . Upon receipt of the slave address with  $R/\bar{W}$  set to one, the X24012 issues an acknowledge and transmits the eight bit word during the next eight clock cycles. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

## Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the  $R/\bar{W}$  bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the  $R/\bar{W}$  bit set to one. This will be followed by an acknowledge from the X24012 and then by the eight bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

2

Figure 7. Current Address Read

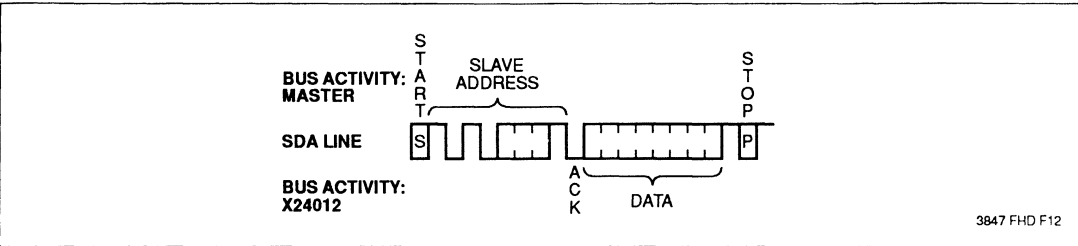
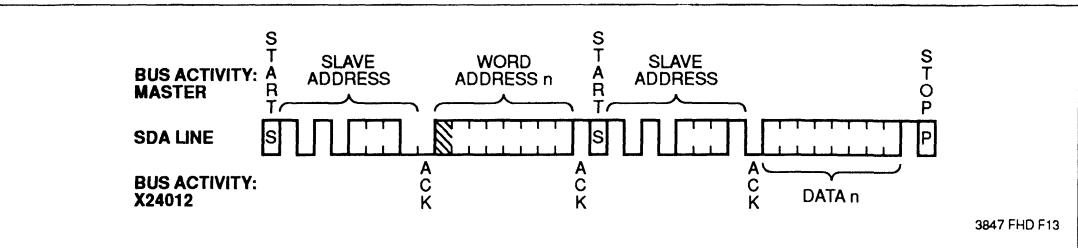


Figure 8. Random Read



# X24012

## Sequential Read

Sequential Read can be initiated as either a current address read or random access read. The first word is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24012 continues to output data for each acknowledge received. The read operation is terminated by the master, by not responding with an acknowledge and by issuing a stop condition.

The data output is sequential, with the data from address  $n$  followed by the data from  $n + 1$ . The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 127), the counter “rolls over” to address 0 and the X24012 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

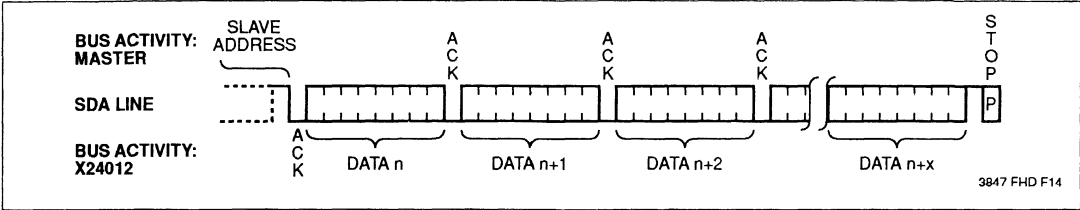
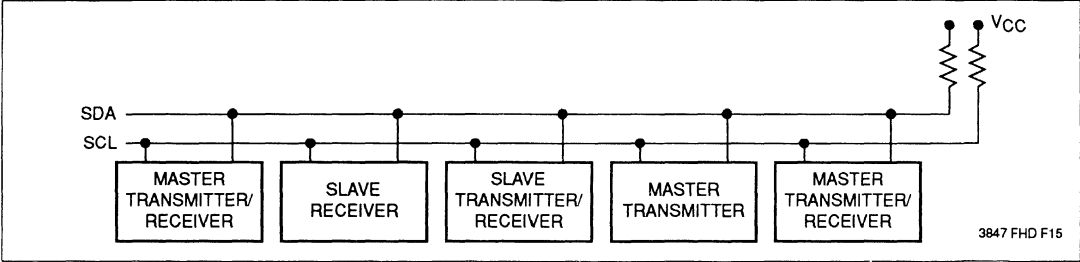


Figure 10. Typical System Configuration



X24012

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	–65°C to +135°C
Storage Temperature .....	–65°C to +150°C
Voltage on any Pin with Respect to V <sub>SS</sub> .....	–1.0V to +7V
D.C. Output Current .....	5 mA
Lead Temperature (Soldering, 10 Seconds) .....	300°C

\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3847 PGM T02

Supply Voltage	Limits
X24012	4.5V to 5.5V
X24012-3	3V to 5.5V
X24012-2.7	2.7V to 5.5V

3847 PGM T03

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC1</sub>	Power Supply Current (Read)		1	mA	SCL = V <sub>CC</sub> × 0.1/V <sub>CC</sub> × 0.9 Levels @ 100 KHz, SDA = Open, All Other Inputs = GND or V <sub>CC</sub> – 0.3V
I <sub>CC2</sub>	Power Supply Current (Write)		2		
I <sub>SB</sub> (1)	Standby Current		50	μA	SCL = SDA = V <sub>CC</sub> – 0.3V, All Other Inputs = GND or V <sub>CC</sub> , V <sub>CC</sub> = 5.5V
I <sub>SB</sub> (2)	Standby Current		30	μA	SCL = SDA = V <sub>CC</sub> – 0.3V, All Other Inputs = GND or V <sub>CC</sub> , V <sub>CC</sub> = 3V
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> (2)	Input Low Voltage	–1.0	V <sub>CC</sub> × 0.3	V	
V <sub>IH</sub> (2)	Input High Voltage	V <sub>CC</sub> × 0.7	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 3 mA

3847 PGM T04

CAPACITANCE T<sub>A</sub> = 25°C, F = 1.0MHZ, V<sub>CC</sub> = 5V

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (3)	Input/Output Capacitance (SDA)	8	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (3)	Input Capacitance (A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , SCL, WC)	6	pF	V <sub>IN</sub> = 0V

3847 PGM T06

- Notes: (1) Must perform a stop command prior to measurement.  
(2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
(3) This parameter is periodically sampled and not 100% tested.



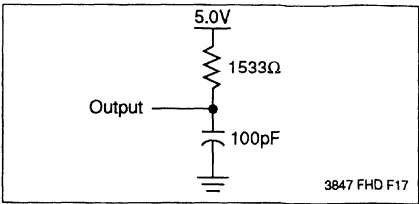
X24012

A.C. CONDITIONS OF TEST

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
Input and Output Timing Levels	$V_{CC} \times 0.5$

3847 PGM T07

EQUIVALENT A.C. LOAD CIRCUIT



3847 FHD F17

A.C. CHARACTERISTICS LIMITS (Over recommended operating conditions unless otherwise specified)

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
$f_{SCL}$	SCL Clock Frequency	0	100	KHz
$T_I$	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
$t_{AA}$	SCL Low to SDA Data Out Valid	0.3	3.5	$\mu$ s
$t_{BUF}$	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		$\mu$ s
$t_{HD:STA}$	Start Condition Hold Time	4.0		$\mu$ s
$t_{LOW}$	Clock Low Period	4.7		$\mu$ s
$t_{HIGH}$	Clock High Period	4.0		$\mu$ s
$t_{SU:STA}$	Start Condition Setup Time	4.7		$\mu$ s
$t_{HD:DAT}$	Data In Hold Time	0		$\mu$ s
$t_{SU:DAT}$	Data In Setup Time	250		ns
$t_R$	SDA and SCL Rise Time		1	$\mu$ s
$t_F$	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		$\mu$ s
$t_{DH}$	Data Out Hold Time	300		ns

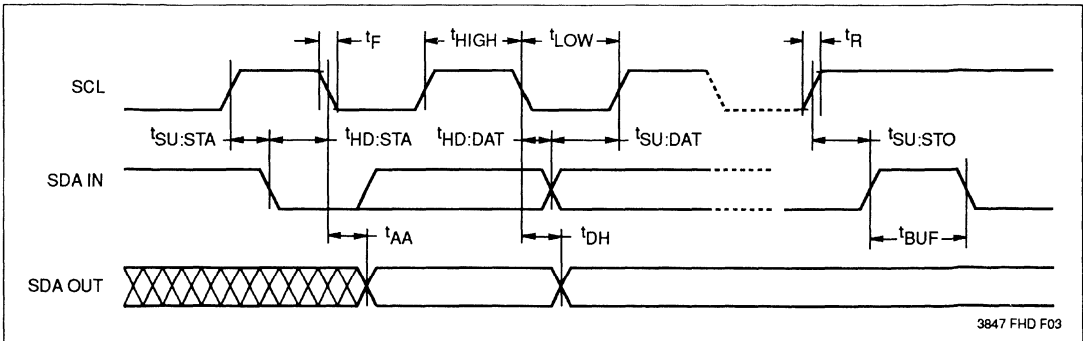
3847 PGM T08

POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(4)}$	Power-Up to Read Operation	1	ms
$t_{PUW}^{(4)}$	Power-Up to Write Operation	5	ms

3847 PGM T09

Bus Timing



3847 FHD F03

**Note:** (4)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

# X24012

## WRITE CYCLE LIMITS

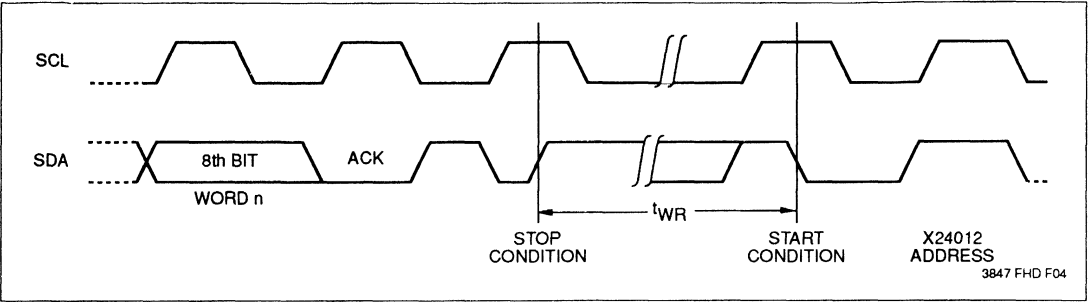
Symbol	Parameter	Min.	Typ. <sup>(5)</sup>	Max.	Units
$t_{WR}^{(6)}$	Write Cycle Time		5	10	ms

3847 PGM T10

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24012

bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

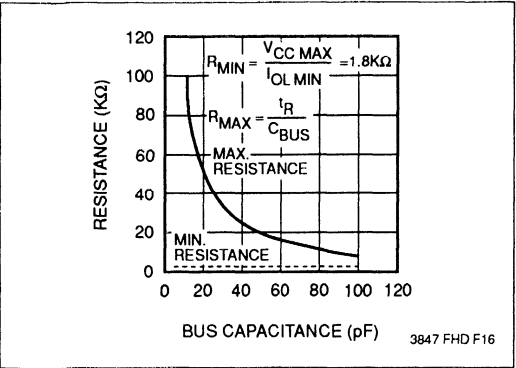
## Write Cycle Timing



**Notes:** (5) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage (5V).

(6)  $t_{WR}$  is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

## Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**X24012**

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**NOTES**



## Preliminary Information

2K

X24C02

256 x 8 Bit

## Serial E<sup>2</sup>PROM

### FEATURES

- 2.7V to 5.5V Power Supply
- Low Power CMOS
  - Active Current Less Than 1 mA
  - Standby Current Less Than 50  $\mu$ A
- Internally Organized 256 x 8
- Self Timed Write Cycle
  - Typical Write Cycle Time of 5 ms
- 2 Wire Serial Interface
  - Bidirectional Data Transfer Protocol
- Four Byte Page Write Operation
  - Minimizes Total Write Time Per Byte
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 100 Years
- New Hardwire—Write Control Function

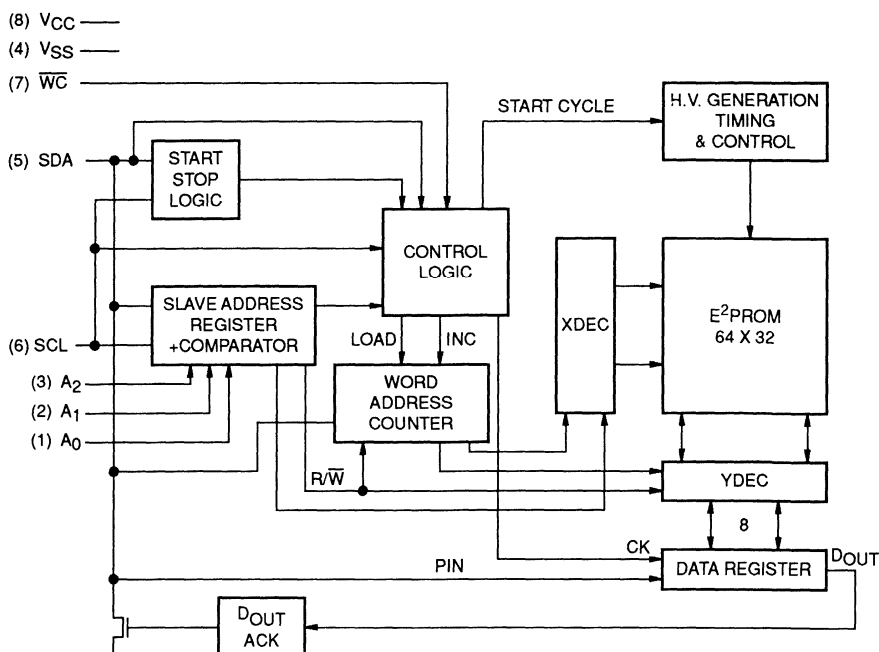
### DESCRIPTION

The X24C02 is CMOS a 2048 bit serial E<sup>2</sup>PROM, internally organized 256 x 8. The X24C02 features a serial interface and software protocol allowing operation on a simple two wire bus. Three address inputs allow up to eight devices to share a common two wire bus.

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years. Available in an eight pin DIP and SOIC package.

2

### FUNCTIONAL DIAGRAM



3838 FHD F01

# X24C02

## PIN DESCRIPTIONS

### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

### Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

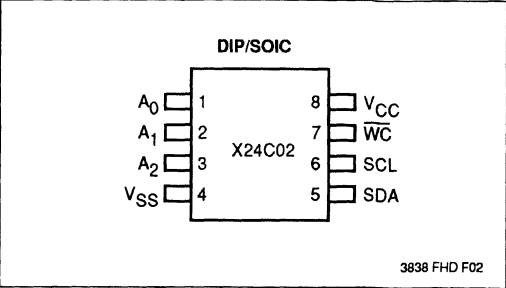
### Address (A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub>)

The address inputs are used to set the least significant three bits of the seven bit slave address. These inputs can be static or actively driven. If used statically they must be tied to V<sub>SS</sub> or V<sub>CC</sub> as appropriate. If actively driven, they must be driven to V<sub>SS</sub> or to V<sub>CC</sub>.

### Write Control ( $\overline{WC}$ )

The Write Control input controls the ability to write to the device. When  $\overline{WC}$  is LOW (tied to V<sub>SS</sub>) the X24C02 will be enabled to perform write operations. When  $\overline{WC}$  is HIGH (tied to V<sub>CC</sub>) the internal high voltage circuitry will be disabled and all writes will be disabled.

## PIN CONFIGURATION



## PIN DESCRIPTIONS

Symbol	Description
A <sub>0</sub> –A <sub>2</sub>	Address Inputs
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V <sub>SS</sub>	Ground
V <sub>CC</sub>	+5V

3838 PGM T01

# X24C02

## DEVICE OPERATION

The X24C02 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X24C02 will be considered a slave in all applications.

## Clock and Data Conventions

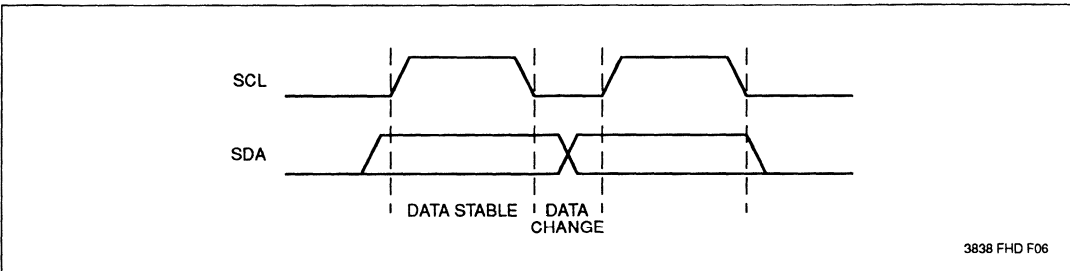
Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

## Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C02 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

2

Figure 1. Data Validity



# X24C02

## Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24C02 to place the device in the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

## Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C02 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24C02 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24C02 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24C02 will continue to transmit data. If an acknowledge is not detected, the X24C02 will terminate further data transmissions. The master must then issue a stop condition to return the X24C02 to the standby power mode and place the device into a known state.

Figure 2. Definition of Start and Stop

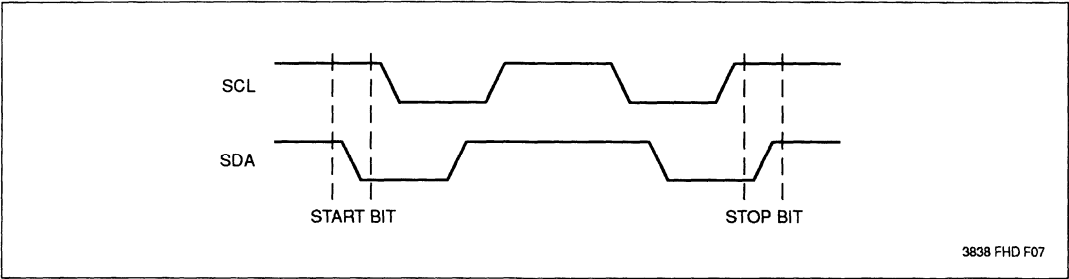
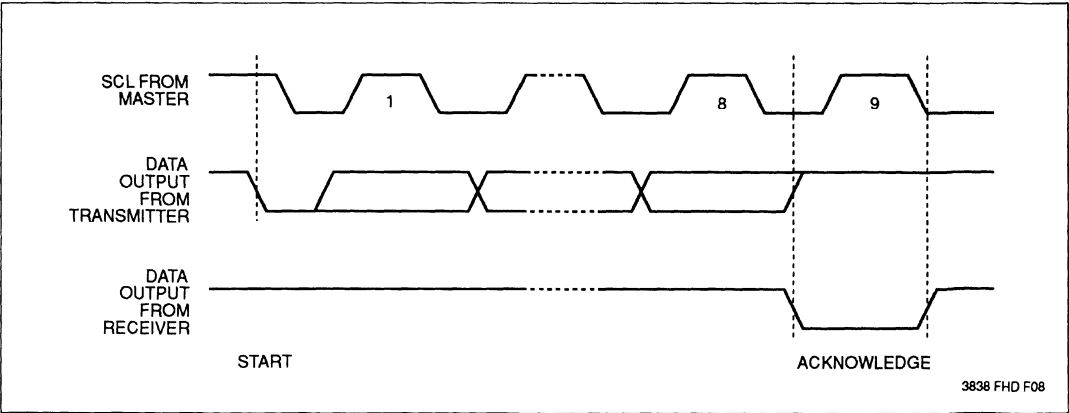


Figure 3. Acknowledge Response From Receiver

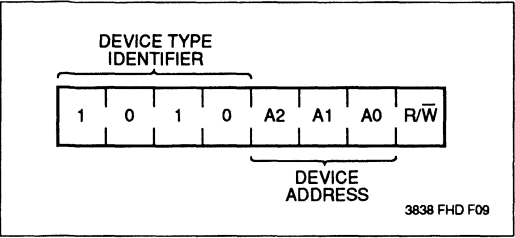


X24C02

DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave are the device type identifier (see Figure 4). For the X24C02 this is fixed as 1010[B].

Figure 4. Slave Address



The next three significant bits address a particular device. A system could have up to eight X24C02 devices on the bus (see Figure 10). The eight addresses are defined by the state of the A<sub>0</sub>, A<sub>1</sub> and A<sub>2</sub> inputs.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operations is selected.

Following the start condition, the X24C02 monitors the SDA bus comparing the slave address being transmitted with its slave address (device type and state of A<sub>0</sub>, A<sub>1</sub> and A<sub>2</sub> inputs). Upon a correct compare the X24C02 outputs an acknowledge on the SDA line. Depending on the state of the R/W bit, the X24C02 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24C02 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words of memory. Upon receipt of the word address the X24C02 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24C02 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24C02 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

2

Figure 5. Byte Write

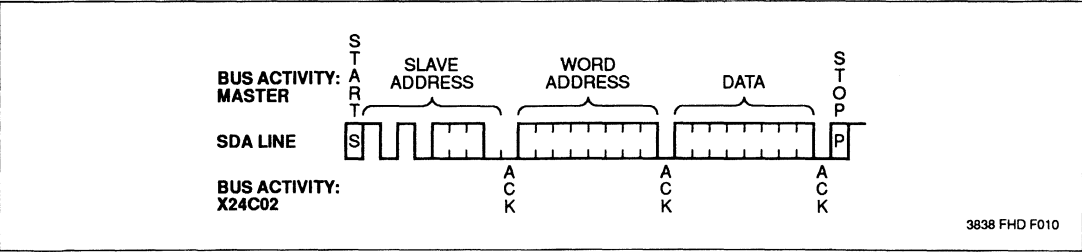
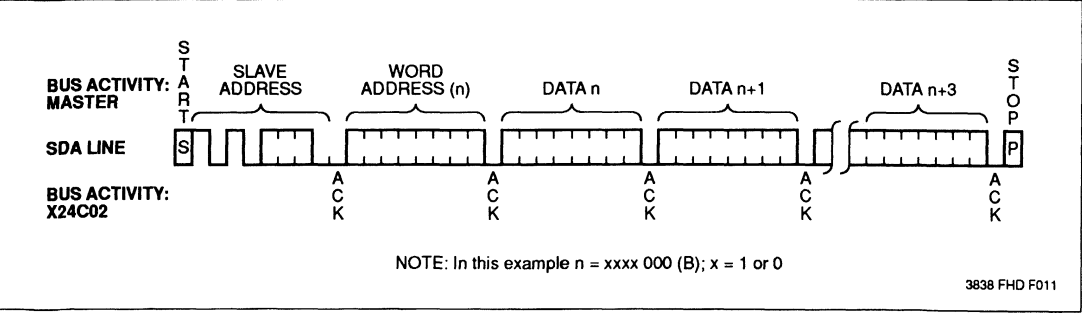


Figure 6. Page Write





## X24C02

### Page Write

The X24C02 is capable of a four byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to three more words. After the receipt of each word, the X24C02 will respond with an acknowledge.

After the receipt of each word, the two low order address bits are internally incremented by one. The high order six bits of the address remain constant. If the master should transmit more than four words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

### Acknowledge Polling

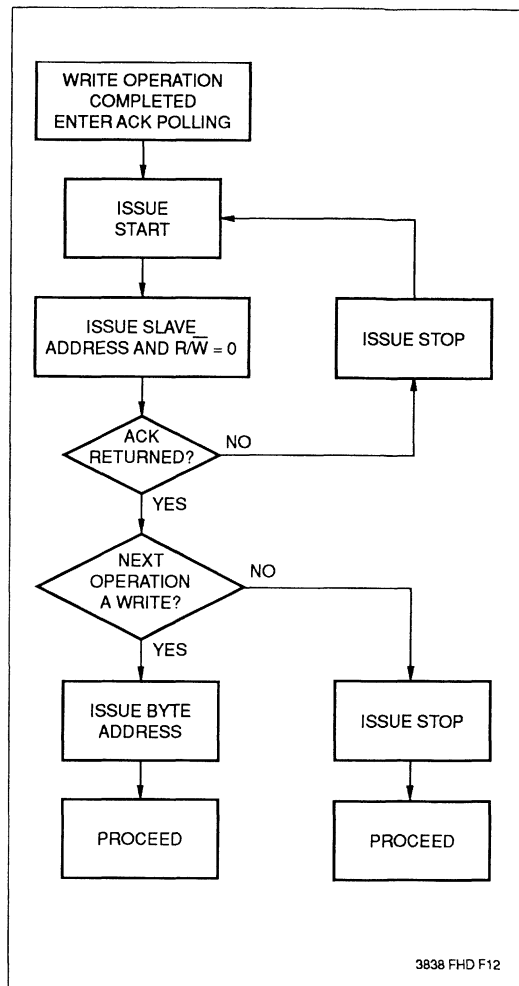
The disabling of the inputs, during the internal write operation, can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24C02 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X24C02 is still busy with the write operation no ACK will be returned. If the X24C02 has completed the write operation an ACK will be returned and the master can then proceed with the next read or write operation.

### READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the  $\overline{R}/\overline{W}$  bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Flow 1. ACK Polling Sequence



# X24C02

## Current Address Read

Internally the X24C02 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address  $n$ , the next read operation would access data from address  $n + 1$ . Upon receipt of the slave address with the R/W bit set to one, the X24C02 issues an acknowledge and transmits the eight bit word during the next eight clock cycles. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

## Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/W bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to one. This will be followed by an acknowledge from the X24C02 and then by the eight bit word. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

2

Figure 7. Current Address Read

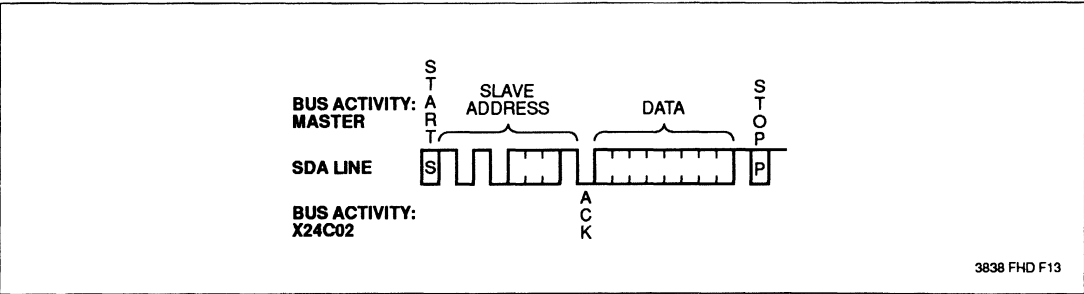
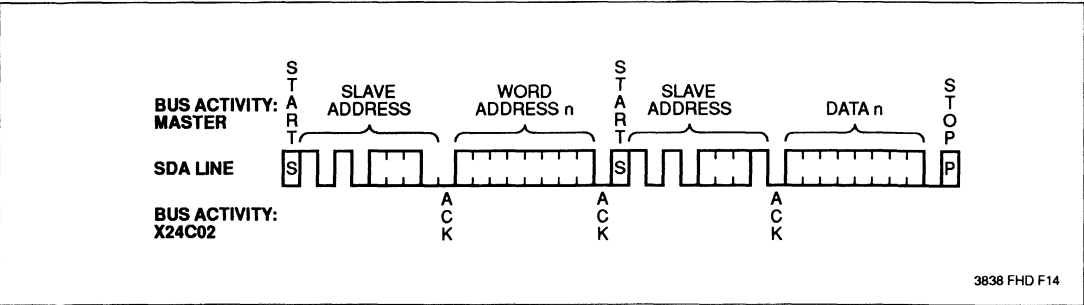


Figure 8. Random Read



# X24C02

## Sequential Read

Sequential Read can be initiated as either a current address read or random access read. The first word is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24C02 continues to output data for each acknowledge received. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge.

The data output is sequential, with the data from address  $n$  followed by the data from  $n + 1$ . The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 255), the counter "rolls over" to address 0 and the X24C02 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

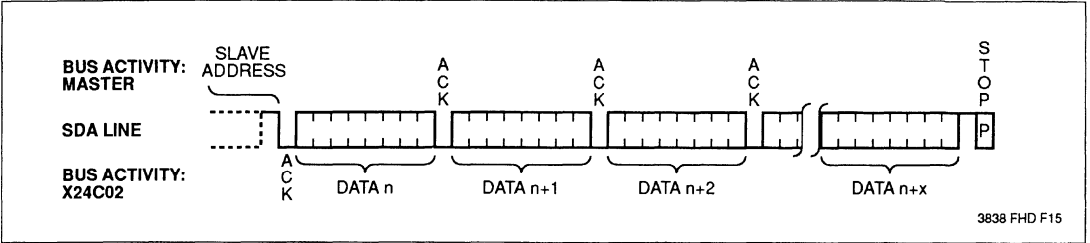
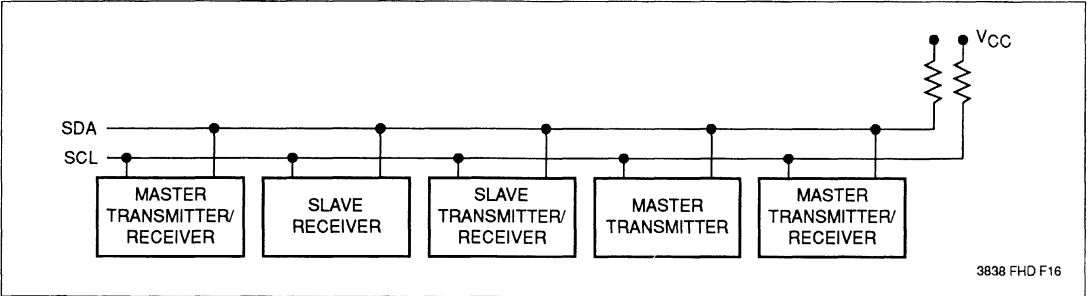


Figure 10. Typical System Configuration



# X24C02

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....-65°C to +135°C  
 Storage Temperature .....-65°C to +150°C  
 Voltage on any Pin with  
   Respect to  $V_{SS}$  .....-1.0V to +7.0V  
 D.C. Output Current .....5 mA  
 Lead Temperature (Soldering, 10 Seconds) .....300°C

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

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Supply Voltage	Limits
X24C02	4.5V to 5.5V
X24C02-3.5	3.5V to 5.5V
X24C02-3	3V to 5.5V
X24C02-2.7	2.7 to 5.5V

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## D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified).

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
$I_{CC1}$	Power Supply Current (read)		1	mA	SCL = $V_{CC} \times 0.1/V_{CC} \times 0.9$ Levels @ 100 KHz, SDA = Open, All Other Inputs = GND or $V_{CC} - 0.3V$
$I_{CC2}$	Power Supply Current (write)		2		
$I_{SB}^{(1)}$	Standby Current		50	$\mu A$	SCL = SDA = $V_{CC} - 0.3V$ , All other Inputs = GND or $V_{CC}$ , $V_{CC} = 5.5V$
$I_{SB}^{(2)}$	Standby Current		30	$\mu A$	SCL = SDA = $V_{CC} - 0.3V$ , All Other Inputs = GND or $V_{CC} = 3.3V + 10\%$
$I_{LI}$	Input Leakage Current		10	$\mu A$	$V_{IN} = GND$ to $V_{CC}$
$I_{LO}$	Output Leakage Current		10	$\mu A$	$V_{OUT} = GND$ to $V_{CC}$
$V_{IL}^{(2)}$	Input Low Voltage	-1.0	$V_{CC} \times 0.3$	V	
$V_{IH}^{(2)}$	Input High Voltage	$V_{CC} \times 0.7$	$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage		0.4	V	$I_{OL} = 3\text{ mA}$

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## CAPACITANCE $T_A = 25^\circ C$ , $f = 1\text{ MHz}$ , $V_{CC} = 5V$

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}^{(3)}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0V$
$C_{IN}^{(3)}$	Input Capacitance ( $A_0, A_1, A_2, SCL, WC$ )	6	pF	$V_{IN} = 0V$

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- Notes:** (1) Must perform a stop command prior to measurement.  
 (2)  $V_{IL}$  min. and  $V_{IH}$  max. are for reference only and are not tested.  
 (3) This parameter is periodically sampled and not 100% tested.

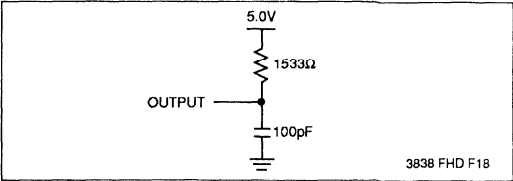
X24C02

A.C. CONDITIONS OF TEST

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$

3838 PGM T05

EQUIVALENT A.C. LOAD CIRCUIT



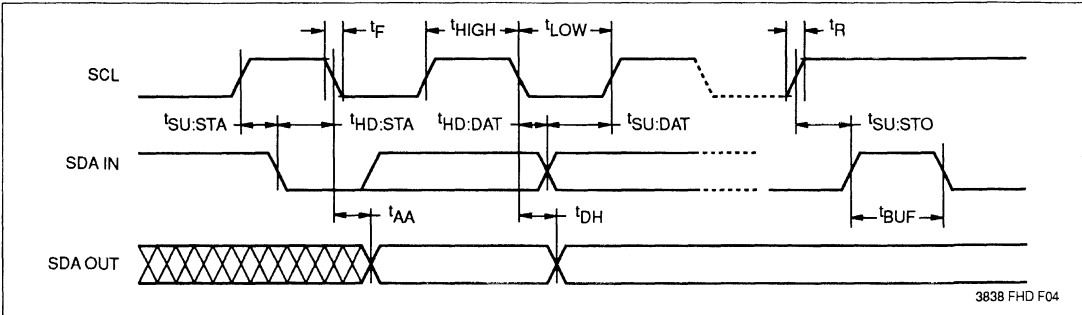
A.C. CHARACTERISTICS (Over recommended operating conditions)

DATA INPUT TIMING

Symbol	Parameter	Min.	Max.	Units
$f_{SCL}$	SCL Clock Frequency	0	100	KHz
$T_I$	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
$t_{AA}$	SCL Low to SDA Data Out Valid	0.3	3.5	μs
$t_{BUF}$	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
$t_{LOW}$	Clock Low Period	4.7		μs
$t_{HIGH}$	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time	4.7		μs
$t_{HD:DAT}$	Data In Hold Time	0		μs
$t_{SU:DAT}$	Data In Setup Time	250		ns
$t_R$	SDA and SCL Rise Time		1	μs
$t_F$	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
$t_{DH}$	Data Out Hold Time	300		ns

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Bus Timing



POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(4)}$	Power-up to Read Operation	1	ms
$t_{PUW}^{(4)}$	Power-up to Write Operation	5	ms

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Notes: (4)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

X24C02

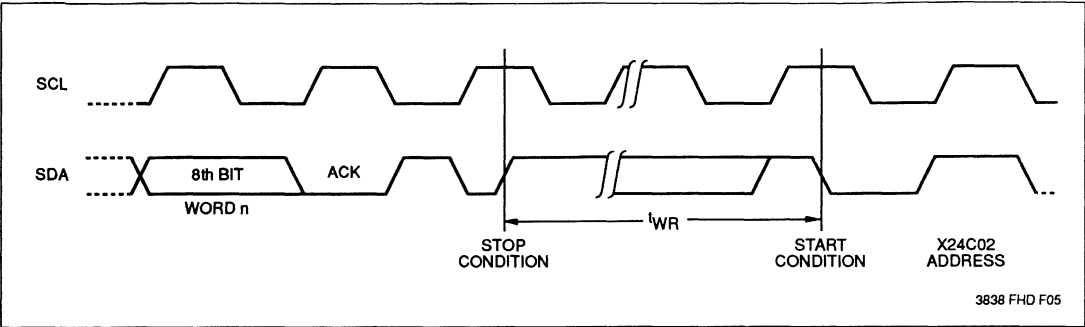
WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t <sub>WR</sub> (6)	Write Cycle Time		5	10	ms

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The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C02 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

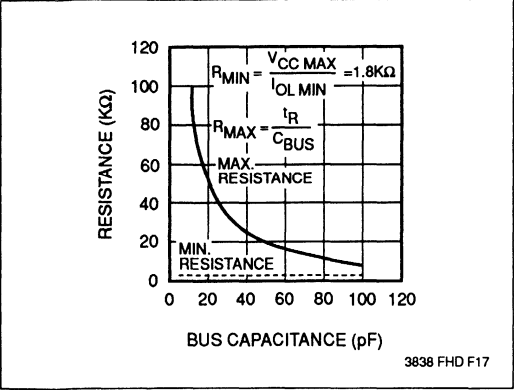
Write Cycle Timing



3838 FHD F05

- Notes: (5) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage (5V)  
(6) t<sub>WR</sub> is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



3838 FHD F17

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**X24C02**

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**NOTES**



Preliminary Information  
Pin 7 No Connect

2K

X24022

256 x 8 Bit

## Serial E<sup>2</sup>PROM

### FEATURES

- 2.7V to 5.5V Power Supply
- Low Power CMOS
  - Active Current Less Than 1 mA
  - Standby Current Less Than 50  $\mu$ A
- Internally Organized 256 x 8
- Self Timed Write Cycle
  - Typical Write Cycle Time of 5 ms
- 2 Wire Serial Interface
  - Bidirectional Data Transfer Protocol
- Four Byte Page Write Operation
  - Minimizes Total Write Time Per Byte
- High Reliability
  - Endurance: 100,000 Cycles Per Byte
  - Data Retention: 100 Years

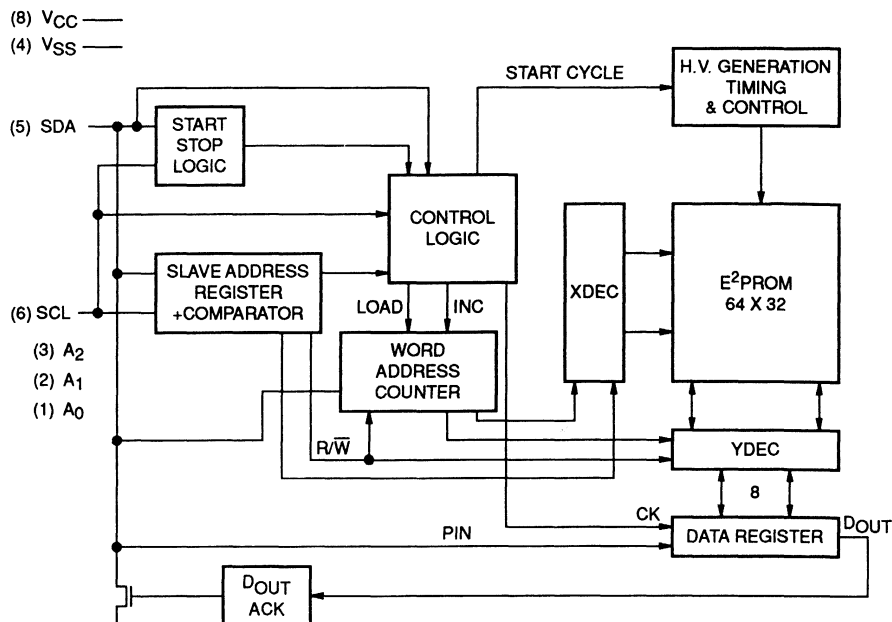
### DESCRIPTION

The X24022 is a CMOS 2048 bit serial E<sup>2</sup>PROM, internally organized 256 x 8. The X24022 features a serial interface and software protocol allowing operation on a simple two wire bus. Three address inputs allow up to eight devices to share a common two wire bus.

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years. The X24022 is available in eight pin DIP and SOIC packages.

2

### FUNCTIONAL DIAGRAM



3848 FHD F01



# X24022

## PIN DESCRIPTIONS

### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

### Serial Data (SDA)

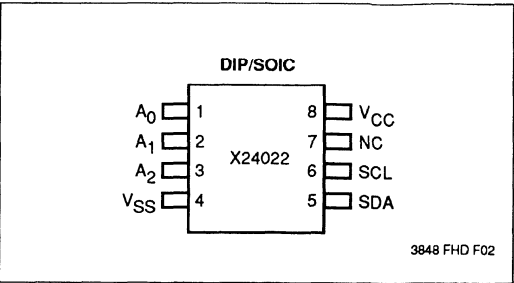
SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

### Address (A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub>)

The address inputs are used to set the least significant three bits of the seven bit slave address. These inputs can be static or actively driven. If used statically they must be tied to V<sub>SS</sub> or V<sub>CC</sub> as appropriate. If actively driven, they must be driven to V<sub>SS</sub> or to V<sub>CC</sub>.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>2</sub>	Address Inputs
SDA	Serial Data
SCL	Serial Clock
NC	No Connect
V <sub>SS</sub>	Ground
V <sub>CC</sub>	+5V

3848 PGM T01

# X24022

## DEVICE OPERATION

The X24022 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24022 will be considered a slave in all applications.

## Clock and Data Conventions

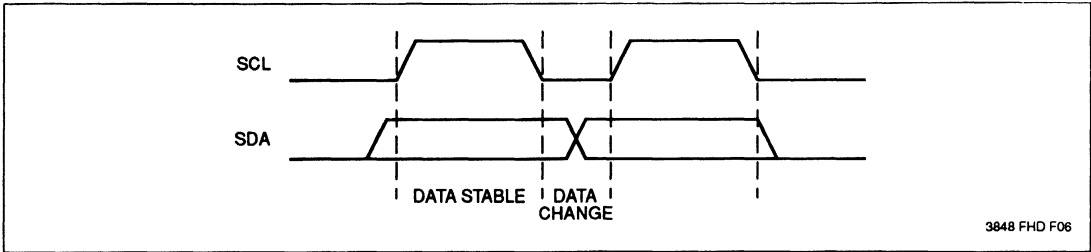
Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

## Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24022 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

2

Figure 1. Data Validity



# X24022

## Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24022 to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

## Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24022 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24022 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24022 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24022 will continue to transmit data. If an acknowledge is not detected, the X24022 will terminate further data transmissions. The master must then issue a stop condition to return the X24022 to the standby power mode and place the device into a known state.

Figure 2. Definition of Start and Stop

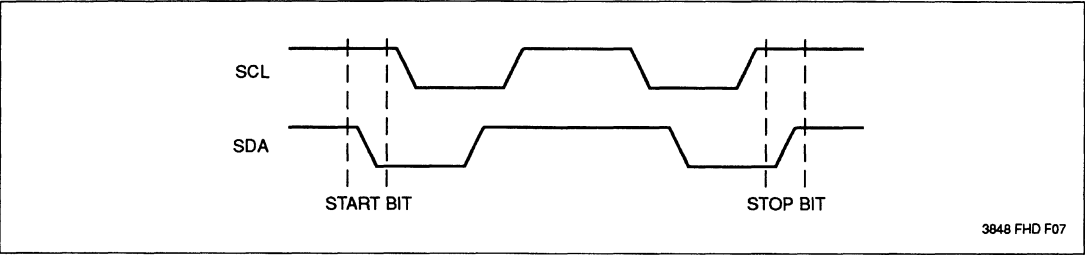
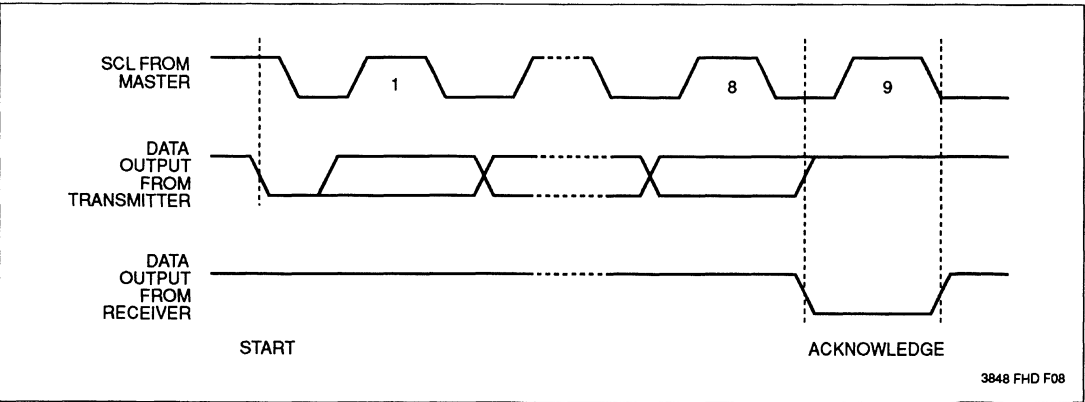


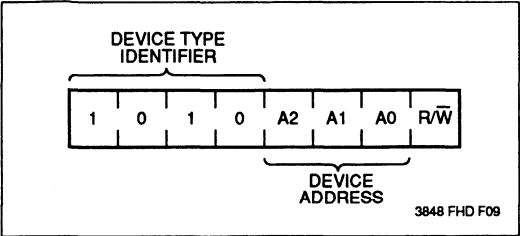
Figure 3. Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X24022 this is fixed as 1010[B].

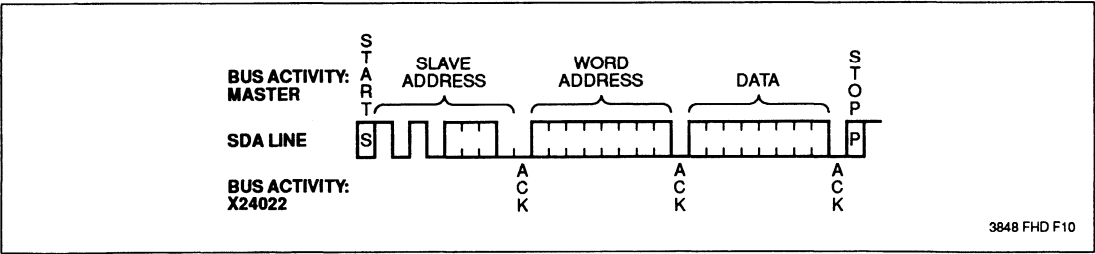
Figure 4. Slave Address



The next three significant bits address a particular device. A system could have up to eight X24022 devices on the bus (see Figure 10). The eight addresses are defined by the state of the A<sub>0</sub>, A<sub>1</sub> and A<sub>2</sub> inputs.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

Figure 5. Byte Write



Following the start condition, the X24022 monitors the SDA bus comparing the slave address being transmitted with its slave address (device type and state of A<sub>0</sub>, A<sub>1</sub> and A<sub>2</sub> inputs). Upon a correct compare the X24022 outputs an acknowledge on the SDA line. Depending on the state of the R/W bit, the X24022 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24022 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words of memory. Upon receipt of the word address the X24022 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24022 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24022 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

X24022

Page Write

The X24022 is capable of an four byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to three more words. After the receipt of each word, the X24022 will respond with an acknowledge.

After the receipt of each word, the two low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than four words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs, during the internal write operation, can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24022 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X24022 is still busy with the write operation no ACK will be returned. If the X24022 has completed the write operation an ACK will be returned and the master can then proceed with the next read or write operation (See Flow 1).

Flow 1. ACK Polling Sequence

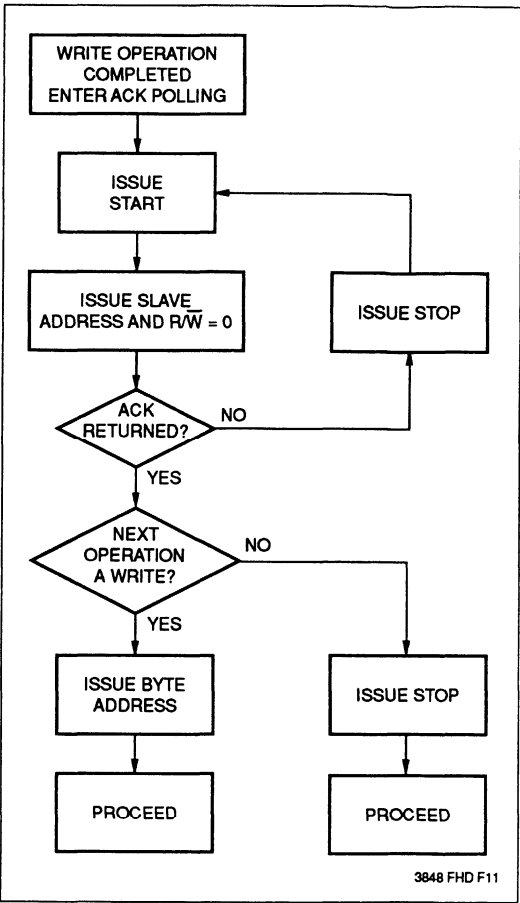
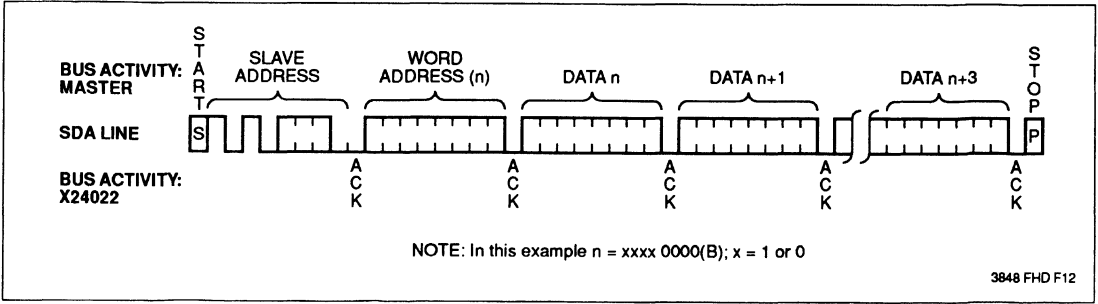


Figure 6. Page Write



READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/W bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Current Address Read

Internally the X24022 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/W set to one, the X24022 issues an acknowledge and transmits the eight bit word

during the next eight clock cycles. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/W bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to one. This will be followed by an acknowledge from the X24022 and then by the eight bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

2

Figure 7. Current Address Read

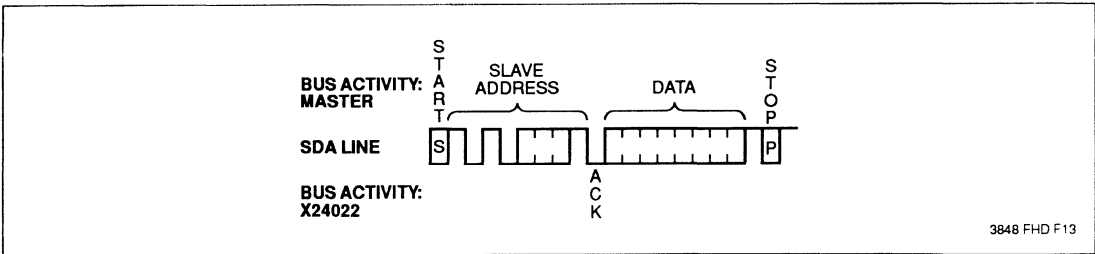
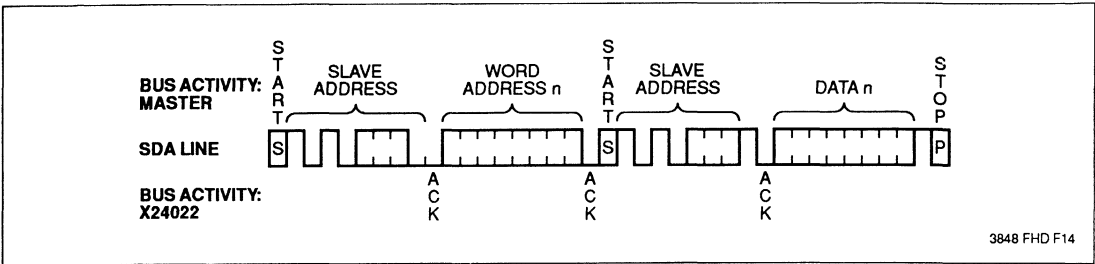


Figure 8. Random Read



# X24022

## Sequential Read

Sequential Read can be initiated as either a current address read or random access read. The first word is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24022 continues to output data for each acknowledge received. The read operation is terminated by the master, by not responding with an acknowledge and by issuing a stop condition.

The data output is sequential, with the data from address  $n$  followed by the data from  $n + 1$ . The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 255), the counter “rolls over” to address 0 and the X24022 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

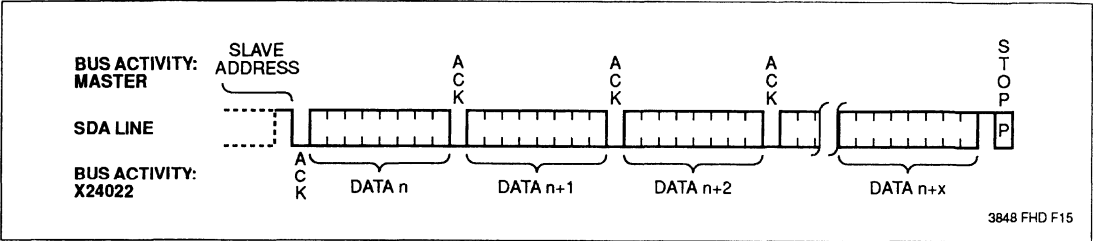
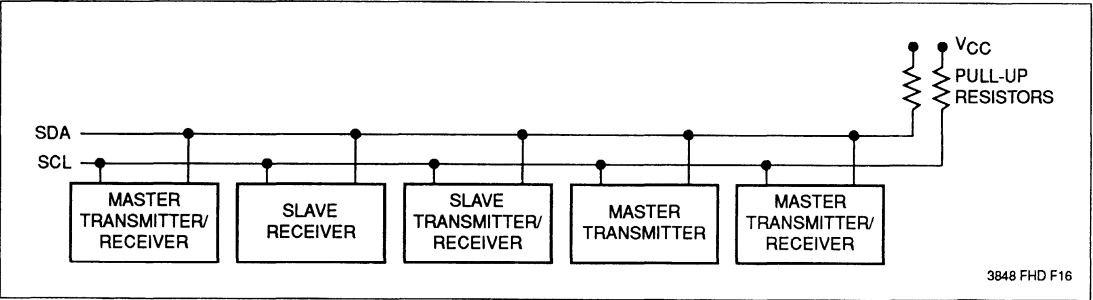


Figure 10. Typical System Configuration



X24022

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	–65°C to +135°C
Storage Temperature .....	–65°C to +150°C
Voltage on any Pin with	
Respect to V <sub>SS</sub> .....	–1.0V to +7V
D.C. Output Current .....	5 mA
Lead Temperature	
(Soldering, 10 Seconds) .....	300°C

\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3848 PGM T02

Supply Voltage	Limits
X24022	4.5V to 5.5V
X24022-3	3V to 5.5V
X24022-2.7	2.7V ± 5.5V

3848 PGM T03

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC1</sub>	Power Supply Current (read)		1	mA	SCL = V <sub>CC</sub> × 0.1/V <sub>CC</sub> × 0.9 Levels @ 100 KHz, SDA = Open, All Other Inputs = GND or V <sub>CC</sub> – 0.3V
I <sub>CC2</sub>	Power Supply Current (write)		2		
I <sub>SB</sub> (1)	Standby Current		50	µA	SCL = SDA = V <sub>CC</sub> – 0.3V, All Other Inputs = GND or V <sub>CC</sub> , V <sub>CC</sub> = 5.5V
I <sub>SB</sub> (2)	Standby Current		30	µA	SCL = SDA = V <sub>CC</sub> – 0.3V, All Other Inputs = GND or V <sub>CC</sub> , V <sub>CC</sub> = 3V
I <sub>LI</sub>	Input Leakage Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> (2)	Input Low Voltage	–1.0	V <sub>CC</sub> × 0.3	V	
V <sub>IH</sub> (2)	Input High Voltage	V <sub>CC</sub> × 0.7	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 3 mA

3848 PGM T04

CAPACITANCE T<sub>A</sub> = 25°C, f = 1.0 MHz, V<sub>CC</sub> = 5V

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (3)	Input/Output Capacitance (SDA)	8	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (3)	Input Capacitance (A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , SCL)	6	pF	V <sub>IN</sub> = 0V

3848 PGM T06

- Notes: (1) Must perform a stop command prior to measurement.  
(2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
(3) This parameter is periodically sampled and not 100% tested.



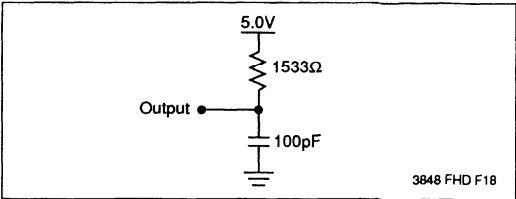
X24022

A.C. CONDITIONS OF TEST

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$

3848 PGM T02

EQUIVALENT A.C. LOAD CIRCUIT



3848 FHD F18

A.C. CHARACTERISTICS LIMITS (Over recommended operating conditions unless otherwise specified)

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
$f_{SCL}$	SCL Clock Frequency	0	100	KHz
$T_I$	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
$t_{AA}$	SCL Low to SDA Data Out Valid	0.3	3.5	μs
$t_{BUF}$	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
$t_{LOW}$	Clock Low Period	4.7		μs
$t_{HIGH}$	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time	4.7		μs
$t_{HD:DAT}$	Data In Hold Time	0		μs
$t_{SU:DAT}$	Data In Setup Time	250		ns
$t_R$	SDA and SCL Rise Time		1	μs
$t_F$	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
$t_{DH}$	Data Out Hold Time	300		ns

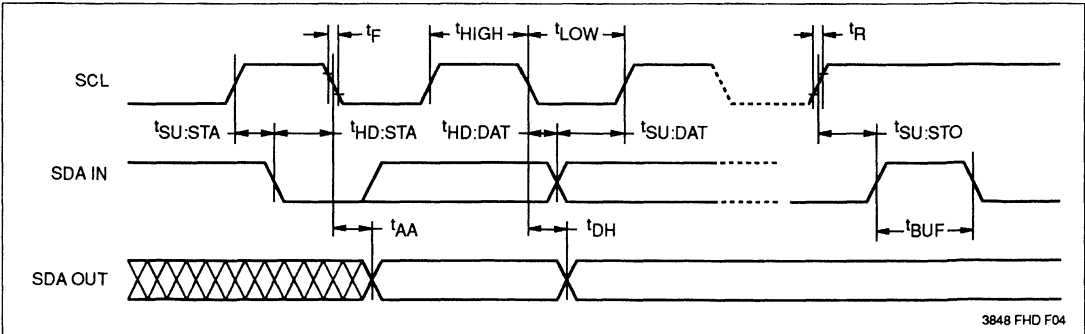
3848 PGM T08

POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(4)}$	Power-Up to Read Operation	1	ms
$t_{PUW}^{(4)}$	Power-Up to Write Operation	5	ms

3848 PGM T09

Bus Timing



3848 FHD F04

Notes: (4)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

X24022

WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t <sub>WR</sub> (6)	Write Cycle Time		5	10	ms

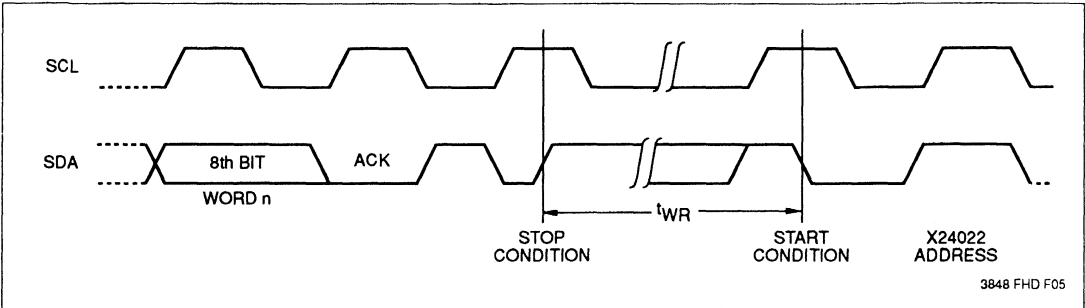
3848 PGM T08

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24022

bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

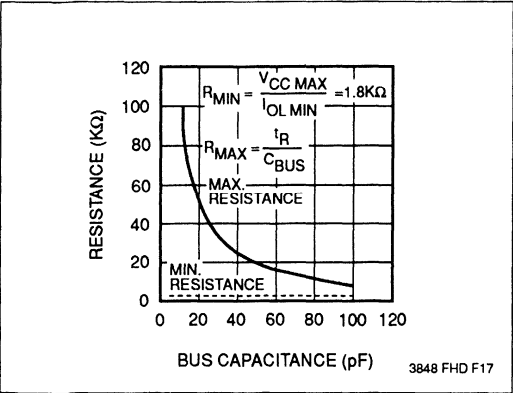
2

Write Cycle Timing



- Notes: (5) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage (5V)  
(6) t<sub>WR</sub> is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**X24022**

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**NOTES**

**4K****X24C04****512 x 8 Bit****Serial E<sup>2</sup>PROM****FEATURES**

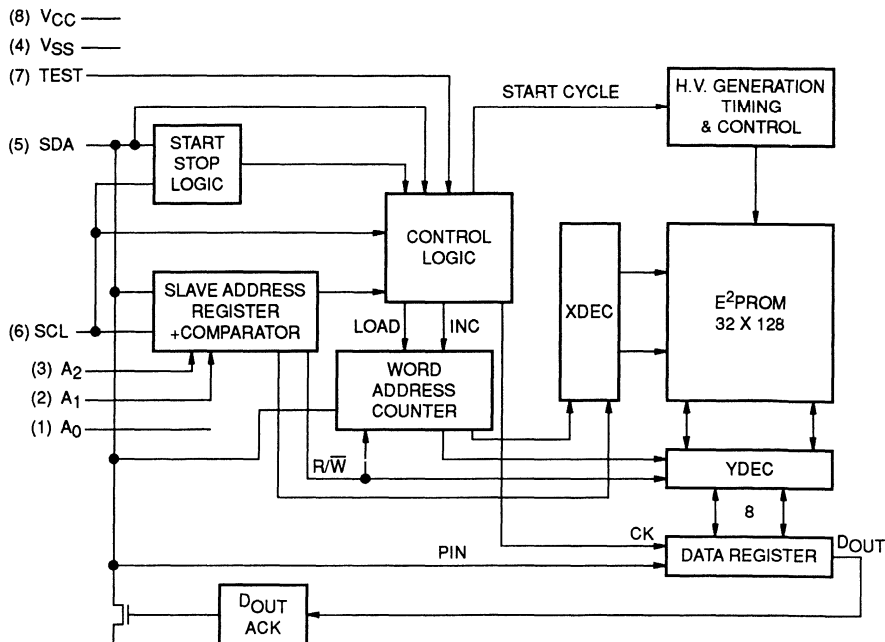
- 2.7V to 5.5V Power Supply
- Low Power CMOS
  - Active Read Current Less Than 1 mA
  - Active Write Current Less Than 3 mA
  - Standby Current Less Than 50  $\mu$ A
- Internally Organized 512 x 8
- 2 Wire Serial Interface
  - Bidirectional Data Transfer Protocol
- Sixteen Byte Page Write Mode
  - Minimizes Total Write Time Per Byte
- Self Timed Write Cycle
  - Typical Write Cycle Time of 5 ms
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 100 Years
- 8 Pin Mini-DIP, 8 Pin SOIC and 14 Pin SOIC Packages

**DESCRIPTION**

The X24C04 is a CMOS 4096 bit serial E<sup>2</sup>PROM, internally organized 512 x 8. The X24C04 features a serial interface and software protocol allowing operation on a simple two wire bus.

The X24C04 is fabricated with Xicor's advanced CMOS Textured Poly Floating Gate Technology.

The X24C04 utilizes Xicor's proprietary DirectWrite™ cell providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

**2****FUNCTIONAL DIAGRAM**

3839 FHD F01

DirectWrite™ is a trademark of Xicor, Inc.

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2-95

Characteristics subject to change without notice

3839-1

# X24C04

## PIN DESCRIPTIONS

### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

### Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-Up Resistor selection graph at the end of this data sheet.

### Address (A<sub>0</sub>)

A<sub>0</sub> is unused by the X24C04, however, it must be tied to V<sub>SS</sub> to insure proper device operation.

### Address (A<sub>1</sub>, A<sub>2</sub>)

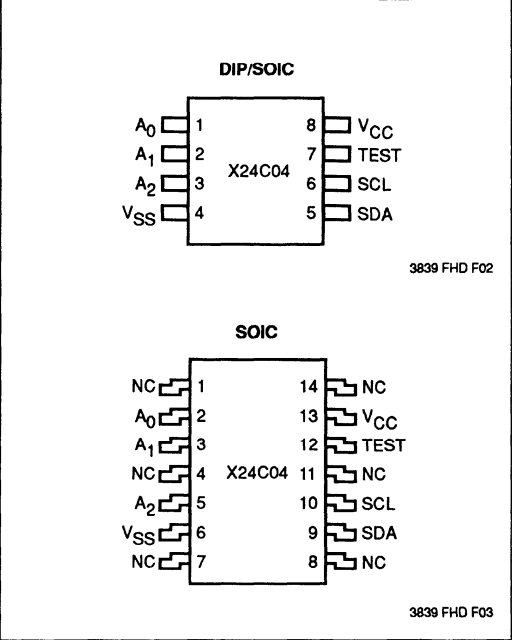
The Address inputs are used to set the appropriate bits of the seven bit slave address. These inputs can be used static or actively driven. If used statically they must be tied to V<sub>SS</sub> or V<sub>CC</sub> as appropriate. If driven they must be driven to V<sub>SS</sub> or to V<sub>CC</sub>.

## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>2</sub>	Address Inputs
SDA	Serial Data
SCL	Serial Clock
TEST	Hold at V <sub>SS</sub>
V <sub>SS</sub>	Ground
V <sub>CC</sub>	Supply Voltage
NC	No Connect

3839 PGM T01

## PIN CONFIGURATION



# X24C04

## DEVICE OPERATION

The X24C04 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24C04 will be considered a slave in all applications.

## Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

## Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C04 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

2

Figure 1. Data Validity

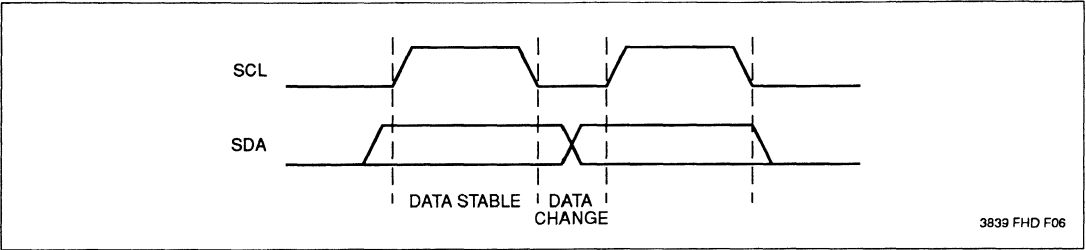
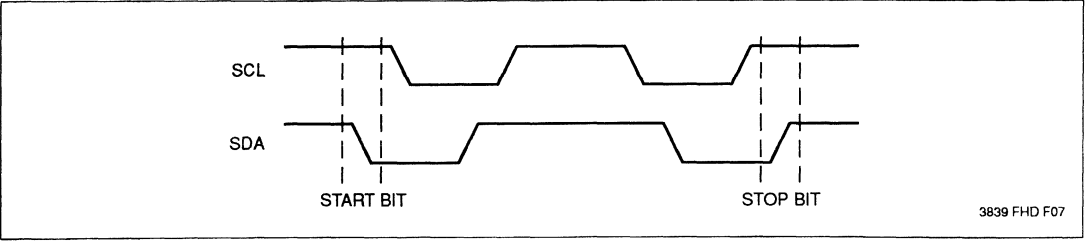


Figure 2. Definition of Start and Stop



## X24C04

### Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24C04 to place the device in the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

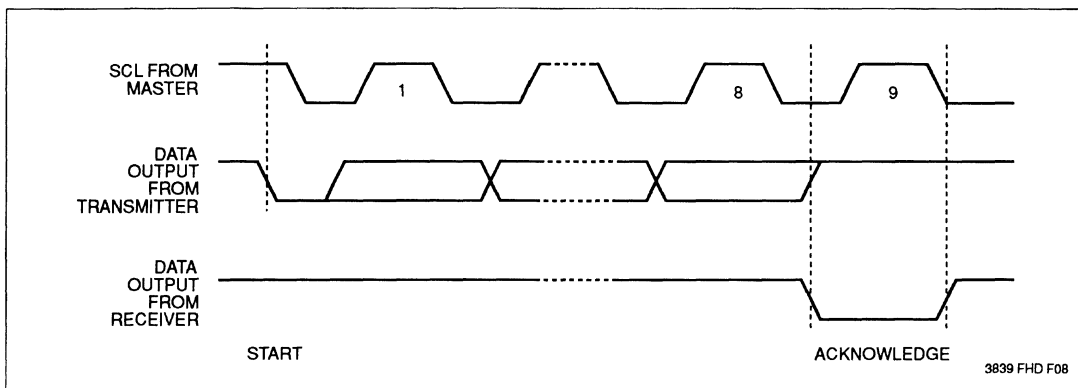
### Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C04 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24C04 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24C04 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24C04 will continue to transmit data. If an acknowledge is not detected, the X24C04 will terminate further data transmissions. The master must then issue a stop condition to return the X24C04 to the standby power mode and place the device into a known state.

Figure 3. Acknowledge Response From Receiver

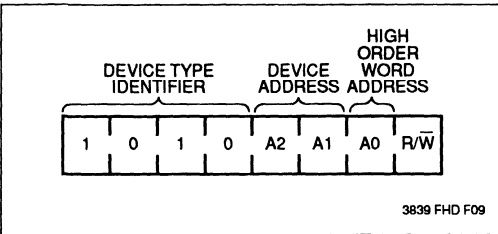


# X24C04

## DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave are the device type identifier (see Figure 4). For the X24C04 this is fixed as 1010[B].

Figure 4. Slave Address



The next two significant bits address a particular device. A system could have up to four X24C04 devices on the bus (see Figure 10). The four addresses are defined by the state of the A<sub>1</sub> and A<sub>2</sub> inputs.

The next bit of the slave address is an extension of the array's address and is concatenated with the eight bits of address in the word address field, providing direct access to the whole 512 x 8 array.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

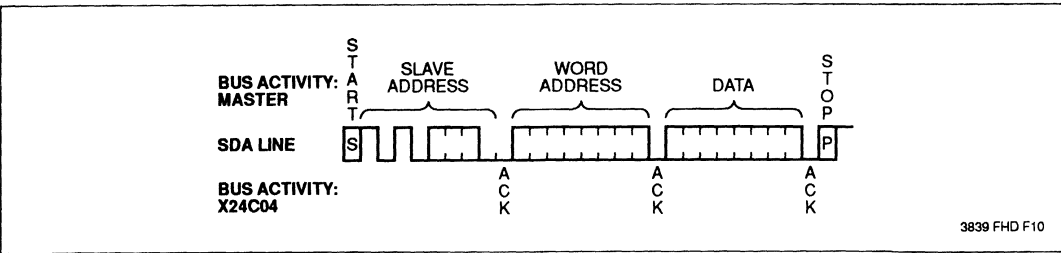
Following the start condition, the X24C04 monitors the SDA bus comparing the slave address being transmitted with its slave address (device type and state of A<sub>1</sub> and A<sub>2</sub> inputs). Upon a correct compare the X24C04 outputs an acknowledge on the SDA line. Depending on the state of the R/W bit, the X24C04 will execute a read or write operation.

## WRITE OPERATIONS

### Byte Write

For a write operation, the X24C04 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 512 words of memory. Upon receipt of the word address the X24C04 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24C04 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24C04 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5. Byte Write





# X24C04

## Page Write

The X24C04 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24C04 will respond with an acknowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

## Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24C04 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X24C04 is still busy with the write operation no ACK will be returned. If the X24C04 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation. Refer to Flow 1.

## READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/W bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Flow 1. ACK Polling Sequence

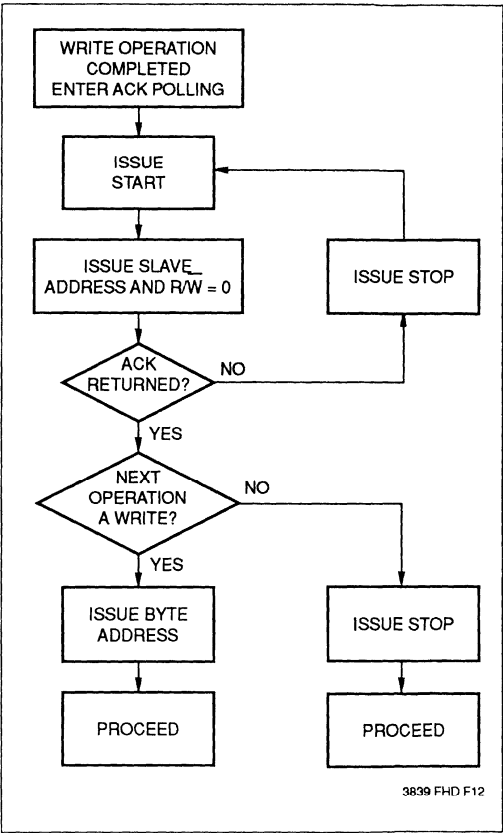
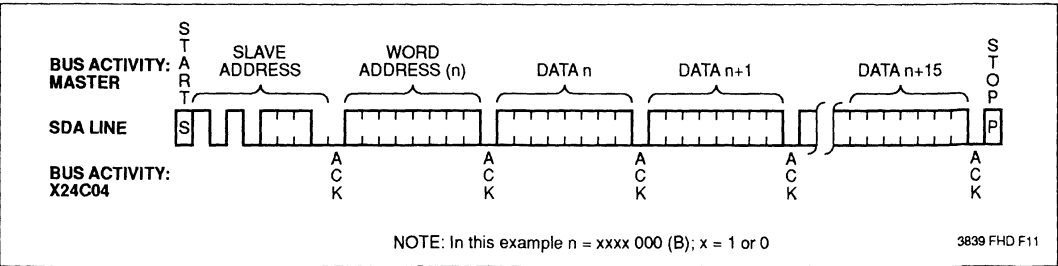


Figure 6. Page Write



# X24C04

## Current Address Read

Internally the X24C04 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address  $n$ , the next read operation would access data from address  $n + 1$ . Upon receipt of the slave address with the R/W bit set to one, the X24C04 issues an acknowledge and transmits the eight bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

## Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/W bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to one. This will be followed by an acknowledge from the X24C04 and then by the eight bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

2

Figure 7. Current Address Read

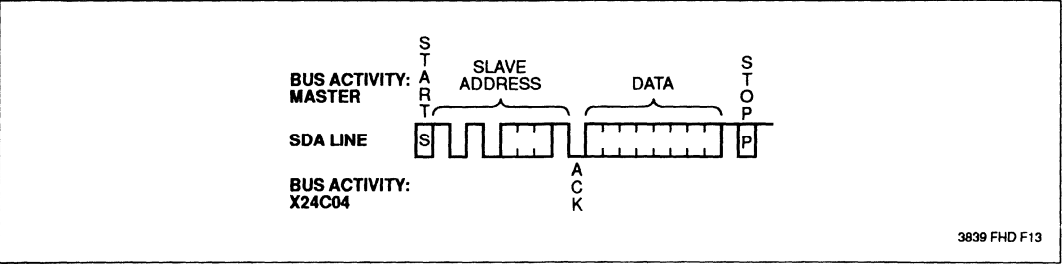
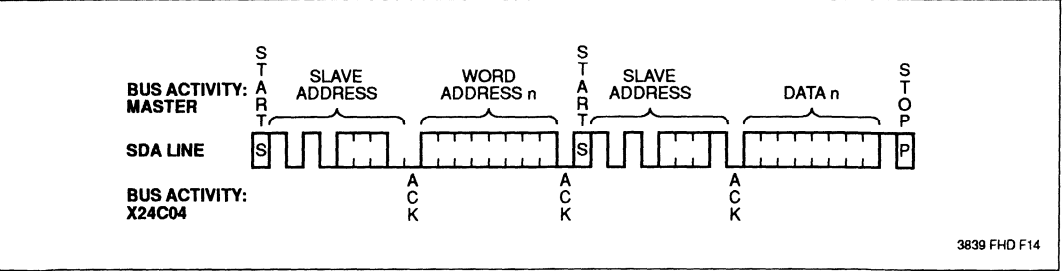


Figure 8. Random Read



## X24C04

### Sequential Read

Sequential Read can be initiated as either a current address read or random access read. The first word is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24C04 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition.

The data output is sequential, with the data from address  $n$  followed by the data from  $n + 1$ . The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 511), the counter "rolls over" to address 0 and the X24C04 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

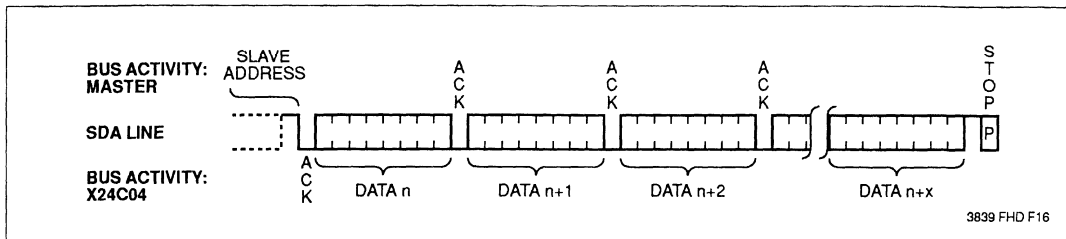
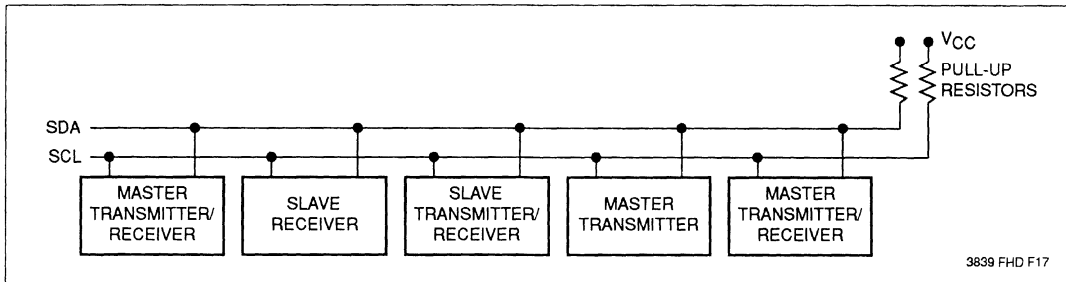


Figure 10. Typical System Configuration



# X24C04

2

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....-65°C to +135°C  
Storage Temperature .....-65°C to +150°C  
Voltage on any Pin with  
    Respect to V<sub>SS</sub> .....-1.0V to +7.0V  
D.C. Output Current .....5 mA  
Lead Temperature  
    (Soldering, 10 Seconds) .....300°C

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

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Supply Voltage	Limits
X24C04	4.5V to 5.5V
X24C04-3.5	3.5V to 5.5V
X24C04-3	3V to 5.5V
X24C04-2.7	2.7V to 5.5V

3836 PGM T03

## D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC1</sub>	V <sub>CC</sub> Supply Current (Read)		1	mA	SCL = V <sub>CC</sub> x 0.1/V <sub>CC</sub> x 0.9 Levels @ 100 KHz, SDA = Open, All Other Inputs = GND or V <sub>CC</sub> - 0.3V
I <sub>CC2</sub>	V <sub>CC</sub> Supply Current (Write)		3		
I <sub>SB1</sub> (1)	V <sub>CC</sub> Standby Current		150	μA	SCL = SDA = V <sub>CC</sub> - 0.3V, All Other Inputs = GND or V <sub>CC</sub> , V <sub>CC</sub> = 5.5V
I <sub>SB2</sub> (1)	V <sub>CC</sub> Standby Current		50	μA	SCL = SDA = V <sub>CC</sub> - 0.3V, All Other Inputs = GND or V <sub>CC</sub> , V <sub>CC</sub> = 3V
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> (2)	Input Low Voltage	-1.0	V <sub>CC</sub> x 0.3	V	
V <sub>IH</sub> (2)	Input High Voltage	V <sub>CC</sub> x 0.7	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 3 mA

3839 PGM T03

## CAPACITANCE T<sub>A</sub> = 25°C, f = 1.0MHz, V<sub>CC</sub> = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C <sub>I/O</sub> (3)	Input/Output Capacitance (SDA)	8	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (3)	Input Capacitance (A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , SCL)	6	pF	V <sub>IN</sub> = 0V

3839 PGM T05

- Notes: (1) Must perform a stop command prior to measurement.  
(2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
(3) This parameter is periodically sampled and not 100% tested.

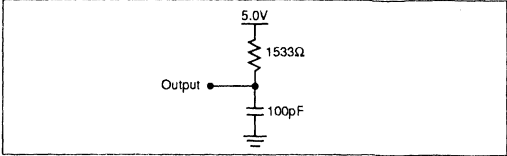
X24C04

A.C. CONDITIONS OF TEST

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$

3839 PGM T02

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)  
Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
$f_{SCL}$	SCL Clock Frequency	0	100	KHz
$T_I$	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
$t_{AA}$	SCL Low to SDA Data Out Valid	0.3	3.5	$\mu$ s
$t_{BUF}$	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		$\mu$ s
$t_{HD:STA}$	Start Condition Hold Time	4.0		$\mu$ s
$t_{LOW}$	Clock Low Period	4.7		$\mu$ s
$t_{HIGH}$	Clock High Period	4.0		$\mu$ s
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		$\mu$ s
$t_{HD:DAT}$	Data In Hold Time	0		$\mu$ s
$t_{SU:DAT}$	Data In Setup Time	250		ns
$t_R$	SDA and SCL Rise Time		1	$\mu$ s
$t_F$	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		$\mu$ s
$t_{DH}$	Data Out Hold Time	300		ns

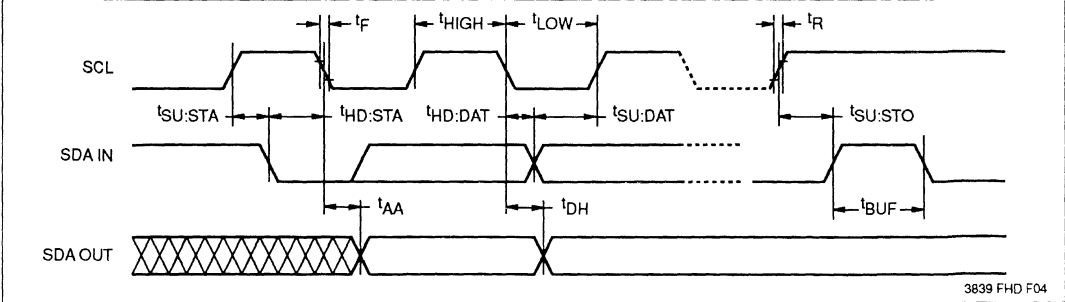
3839 PGM T06

POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(4)}$	Power-up to Read Operation	1	ms
$t_{PUW}^{(4)}$	Power-up to Write Operation	5	ms

3839 PGM T07

Bus Timing



3839 FHD F04

Notes: (4)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

# X24C04

## Write Cycle Limits

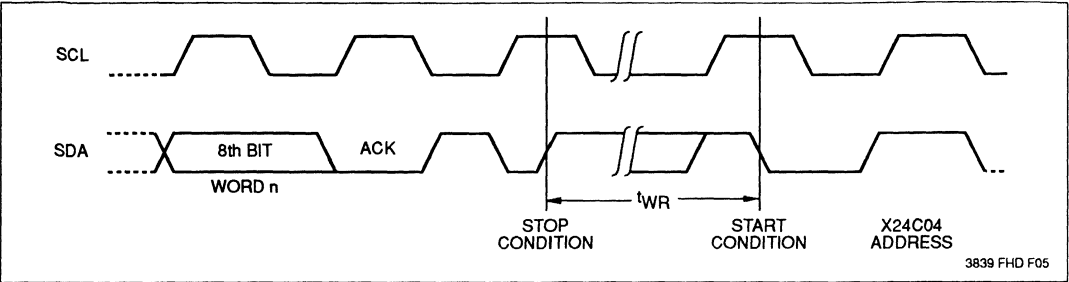
Symbol	Parameter	Min.	Typ.(5)	Max.	Units
$t_{WR}^{(6)}$	Write Cycle Time		5	10	ms

3839 PGM T08

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C04

bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

## Write Cycle Timing

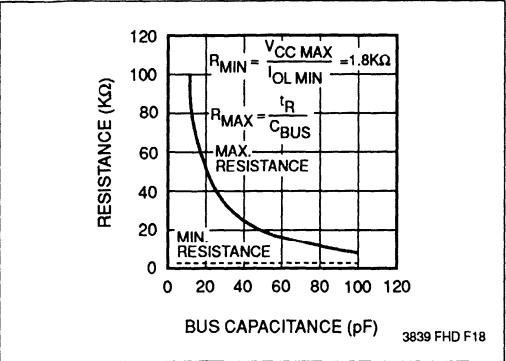


**Notes:** (5) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage (5V).

(6)  $t_{WR}$  is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

2

## Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**X24C04**

---

**NOTES**

4K

**X24042**

512 x 8 Bit

## Serial E<sup>2</sup>PROM

### TYPICAL FEATURES

- 2.7V to 5.5V Power Supply
- Low Power CMOS
  - Active Read Current Less Than 1 mA
  - Active Write Current Less Than 3 mA
  - Standby Current Less Than 50  $\mu$ A
- Internally Organized 512 x 8
- 2 Wire Serial Interface
  - Bidirectional Data Transfer Protocol
- Sixteen Byte Page Write Mode
  - Minimizes Total Write Time Per Byte
- Self Timed Write Cycle
  - Typical Write Cycle Time of 5 ms
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 100 Years
- 8 Pin Mini-DIP and 8 Pin SOIC Packages

### DESCRIPTION

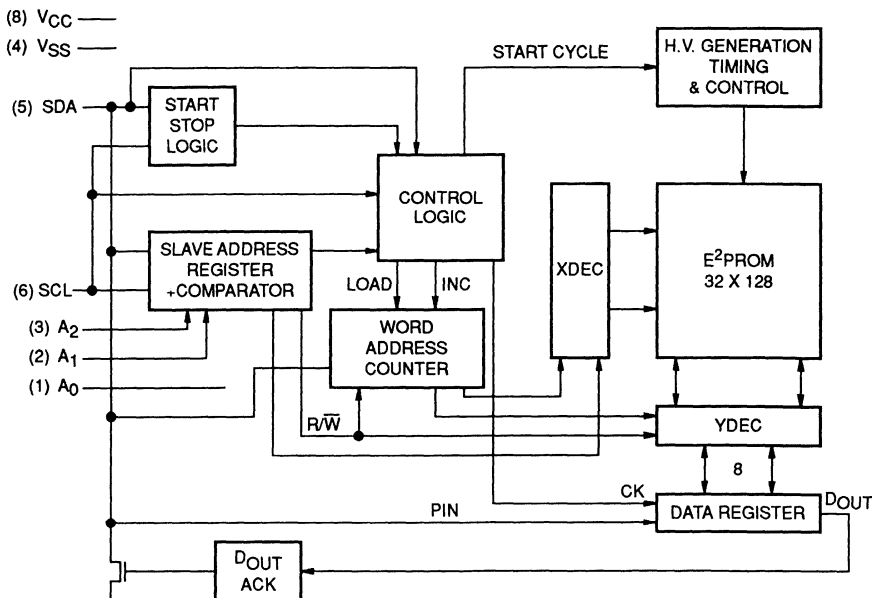
The X24042 is a CMOS 4,096 bit serial E<sup>2</sup>PROM, internally organized 512 x 8. The X24042 features a serial interface and software protocol allowing operation on a simple two wire bus.

The X24042 is fabricated with Xicor's advanced CMOS Textured Poly Floating Gate Technology.

The X24042 utilizes Xicor's proprietary Direct Write<sup>™</sup> cell providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

2

### FUNCTIONAL DIAGRAM



3849 FHD F01



# X24042

## PIN DESCRIPTIONS

### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

### Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-Up Resistor selection graph at the end of this data sheet.

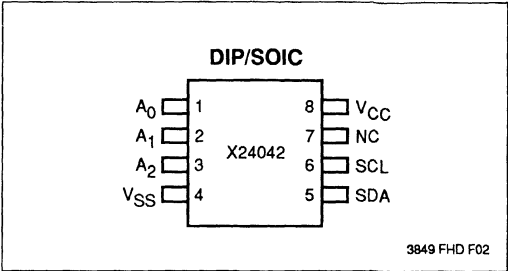
### Address (A<sub>0</sub>)

A<sub>0</sub> is unused by the X24042, however, it must be tied to V<sub>SS</sub> to insure proper device operation.

### Address (A<sub>1</sub>, A<sub>2</sub>)

The Address inputs are used to set the appropriate bits of the seven bit slave address. These inputs can be used static or actively driven. If used statically they must be tied to V<sub>SS</sub> or V<sub>CC</sub> as appropriate. If driven they must be driven to V<sub>SS</sub> or to V<sub>CC</sub>.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>2</sub>	Address Inputs
SDA	Serial Data
SCL	Serial Clock
NC	No Connect
V <sub>SS</sub>	Ground
V <sub>CC</sub>	Supply Voltage

3849 PGM T01

# X24042

## DEVICE OPERATION

The X24042 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24042 will be considered a slave in all applications.

## Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

## Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24042 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

## Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24042 to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

2

Figure 1. Data Validity

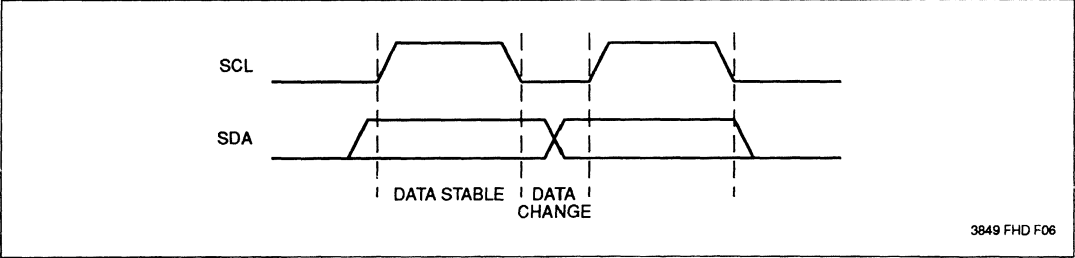
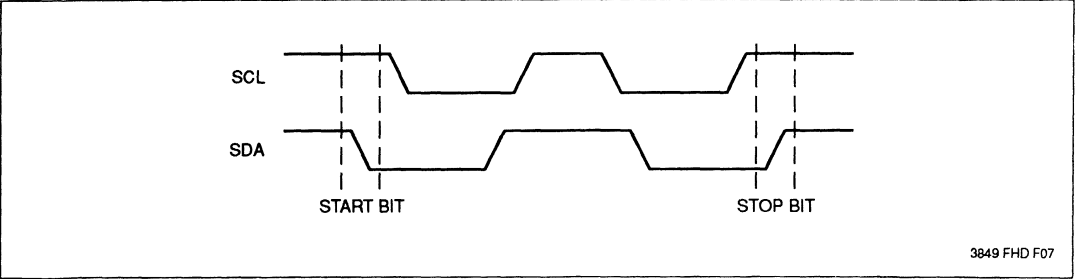


Figure 2. Definition of Start and Stop



## X24042

### Acknowledge

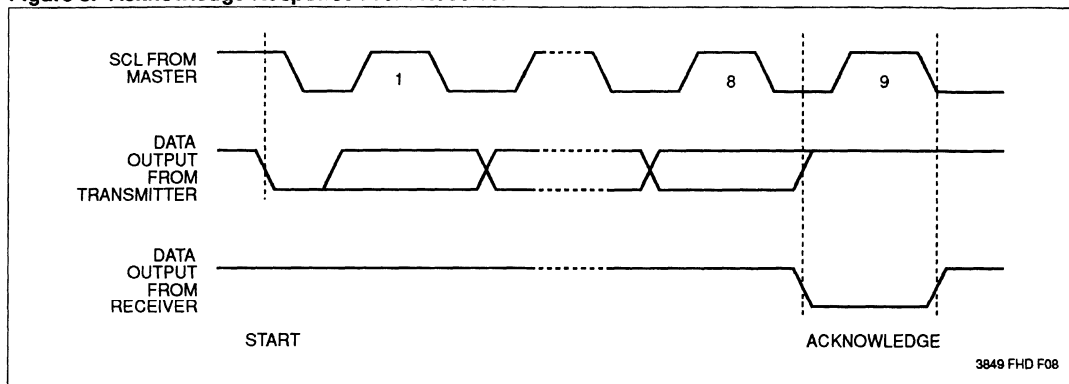
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24042 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24042 will respond with an acknowledge

after the receipt of each subsequent eight bit word.

In the read mode the X24042 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24042 will continue to transmit data. If an acknowledge is not detected, the X24042 will terminate further data transmissions. The master must then issue a stop condition to return the X24042 to the standby power mode and place the device into a known state.

**Figure 3. Acknowledge Response From Receiver**

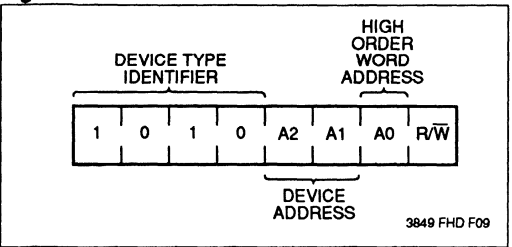


# X24042

## DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X24042 this is fixed as 1010[B].

Figure 4. Slave Address



The next two significant bits addresses a particular device. A system could have up to four X24042 devices on the bus (see Figure 10). The four addresses are defined by the state of the A1 and A2 input.

The next bit of the slave address is an extension of the array's address and is concatenated with the eight bits of address in the word address field, providing direct access to the whole 512 x 8 array.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

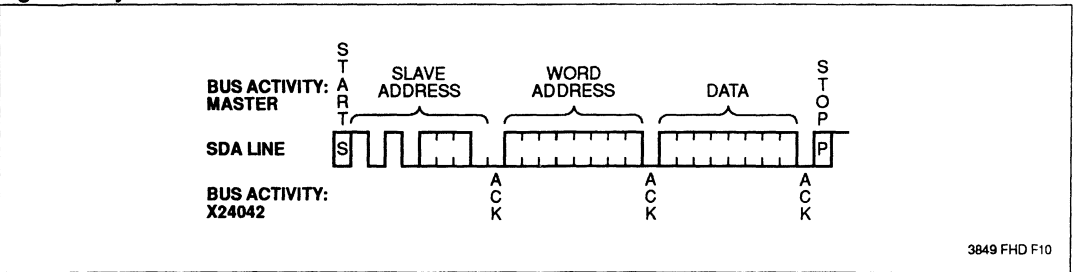
Following the start condition, the X24042 monitors the SDA bus comparing the slave address being transmitted with its slave address (device type and state of the A2 and A1 inputs). Upon a correct compare the X24042 outputs an acknowledge on the SDA line. Depending on the state of the R/W bit, the X24042 will execute a read or write operation.

## WRITE OPERATIONS

### Byte Write

For a write operation, the X24042 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 512 words in the selected page of memory. Upon receipt of the word address the X24042 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24042 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24042 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5. Byte Write



## X24042

### Page Write

The X24042 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to seven more words. After the receipt of each word, the X24042 will respond with an acknowledge.

After the receipt of each word, the three low order address bits are internally incremented by one. The high order eight bits of the word address remain constant. The master should not transmit more than eight words prior to generating the stop condition. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

### Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24042 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X24042 is still busy with the write operation no ACK will be returned. If the X24042 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation. Refer to Flow 1.

### Flow 1. ACK Polling Sequence

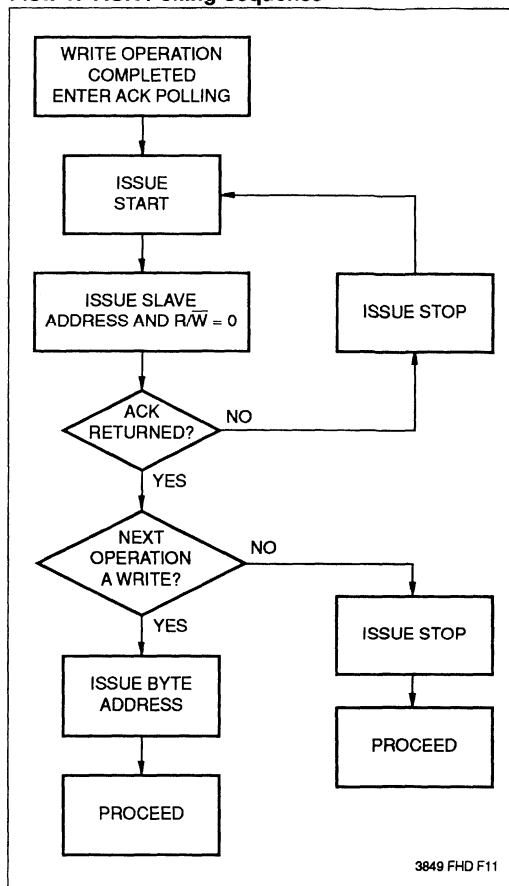
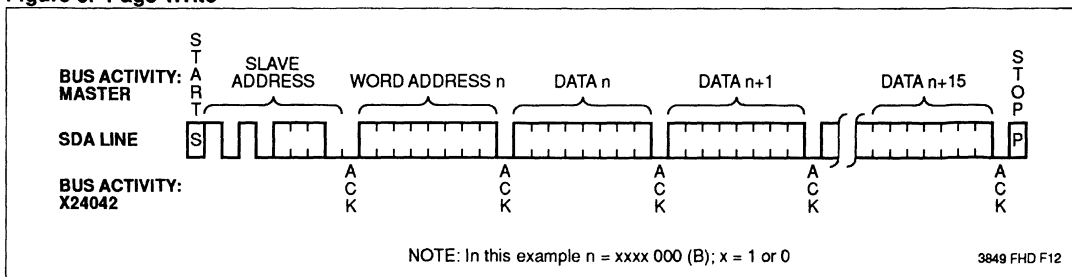


Figure 6. Page Write



# X24042

## READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/W bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

### Current Address Read

Internally the X24042 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address  $n$ , the next read operation would access data from address  $n + 1$ . Upon receipt of the slave address with R/W set to one, the X24042 issues an acknowledge and transmits the eight bit word.

The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

### Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/W bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to one. This will be followed by an acknowledge from the X24042 and then by the eight bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

2

Figure 7. Current Address Read

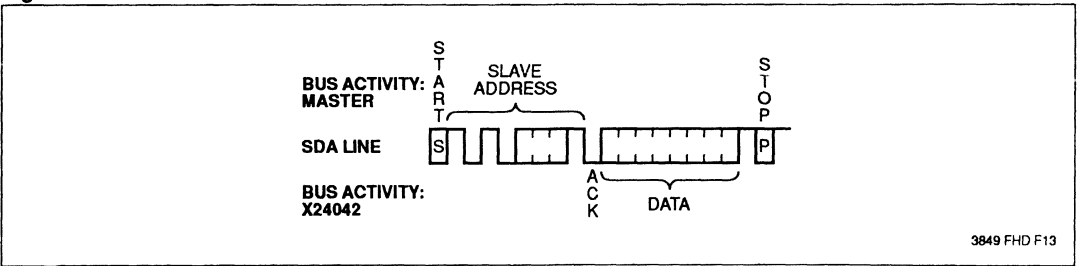
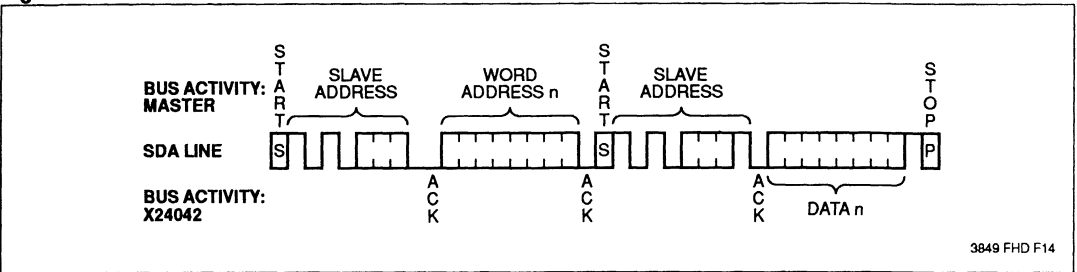


Figure 8. Random Read



## X24042

### Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The X24042 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition.

The data output is sequential, with the data from address  $n$  followed by the data from  $n + 1$ . The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 511) the counter "rolls over" to address 0 and the X24042 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

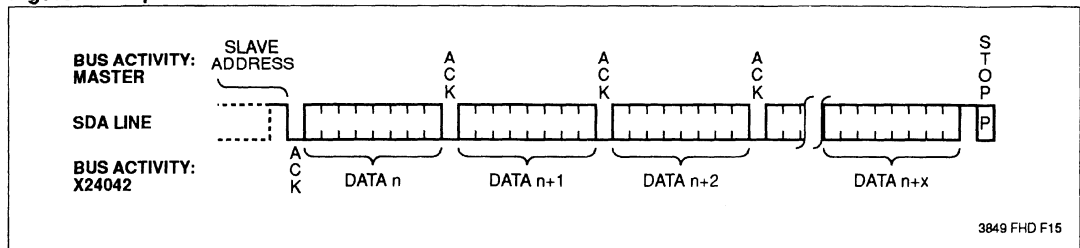
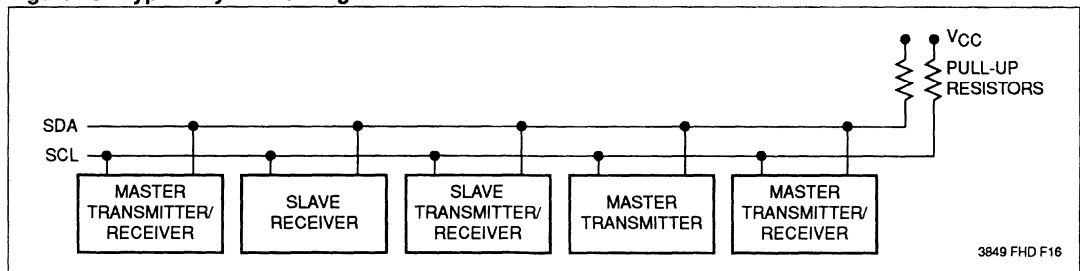


Figure 10. Typical System Configuration



# X24042

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	-65°C to +135°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin with Respect to V <sub>SS</sub> .....	-1.0V to +7V
D.C. Output Current .....	5 mA
Lead Temperature (Soldering, 10 Seconds) .....	300°C

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

3849 PGM T02

Supply Voltage	Limits
X24042	4.5V to 5.5V
X24042-3	3.0V to 5.5V
X24042-2.7	2.7V to 5.5V

3849 PGM T03

## D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC1</sub>	V <sub>CC</sub> Supply Current (Read)		1	mA	SCL = V <sub>CC</sub> x 0.1/V <sub>CC</sub> x 0.9 Levels @ 100 KHz, SDA = Open, All Other Inputs = GND or V <sub>CC</sub> - 0.3V
I <sub>CC2</sub>	V <sub>CC</sub> Supply Current (Write)		3		
I <sub>SB1</sub> (1)	V <sub>CC</sub> Standby Current		150	µA	SCL = SDA = V <sub>CC</sub> - 0.3V, All Other Inputs = GND or V <sub>CC</sub> , V <sub>CC</sub> = 5.5V
I <sub>SB2</sub> (1)	V <sub>CC</sub> Standby Current		50	µA	SCL = SDA = V <sub>CC</sub> - 0.3V, All Other Inputs = GND or V <sub>CC</sub> , V <sub>CC</sub> = 3V
I <sub>LI</sub>	Input Leakage Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> (2)	Input Low Voltage	-1.0	V <sub>CC</sub> x 0.3	V	
V <sub>IH</sub> (2)	Input High Voltage	V <sub>CC</sub> x 0.7	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 3 mA

3849 PGM T04

## CAPACITANCE T<sub>A</sub> = 25°C, F = 1.0MHZ, V<sub>CC</sub> = 5V

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (3)	Input/Output Capacitance (SDA)	8	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (3)	Input Capacitance (A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , SCL)	6	pF	V <sub>IN</sub> = 0V

3849 PGM T05

- Notes:** (1) Must perform a stop command prior to measurement.  
(2) V<sub>IL</sub> min and V<sub>IH</sub> max. are for reference only and are not 100% tested.  
(3) This parameter is periodically sampled and not 100% tested.



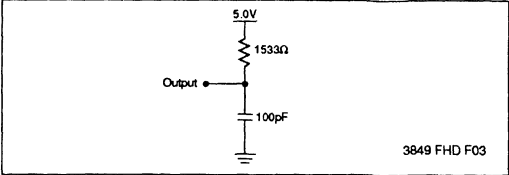
X24042

A.C. CONDITIONS OF TEST

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
I/O Timing Levels	$V_{CC} \times 0.5$

3849 PGM T06

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CHARACTERISTICS LIMITS (Over recommended operating conditions, unless otherwise specified).

READ & WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Max.	Units
$t_{SCL}$	SCL Clock Frequency	0	100	KHz
$t_I$	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
$t_{AA}$	SCL Low to SDA Data Out Valid	0.3	3.5	$\mu$ s
$t_{BUF}$	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		$\mu$ s
$t_{HD:STA}$	Start Condition Hold Time	4.0		$\mu$ s
$t_{LOW}$	Clock Low Period	4.7		$\mu$ s
$t_{HIGH}$	Clock High Period	4.0		$\mu$ s
$t_{SU:STA}$	Start Condition Setup Time	4.7		$\mu$ s
$t_{HD:DAT}$	Data In Hold Time	0		$\mu$ s
$t_{SU:DAT}$	Data In Setup Time	250		ns
$t_R$	SDA and SCL Rise Time		1	$\mu$ s
$t_F$	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		$\mu$ s
$t_{DH}$	Data Out Hold Time	300		ns

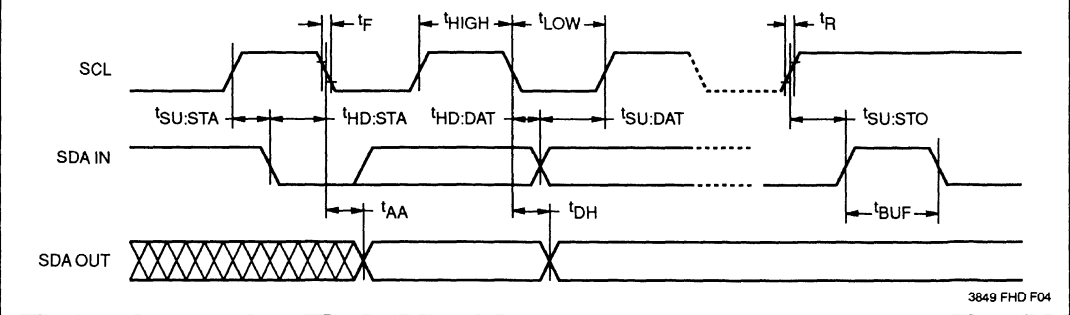
3849 PGM T07

POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(4)}$	Power-Up to Read Operation	1	ms
$t_{PUW}^{(4)}$	Power-Up to Write Operation	5	ms

3849 PGM T08

Bus Timing



Note: (4)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

X24042

WRITE CYCLE LIMITS

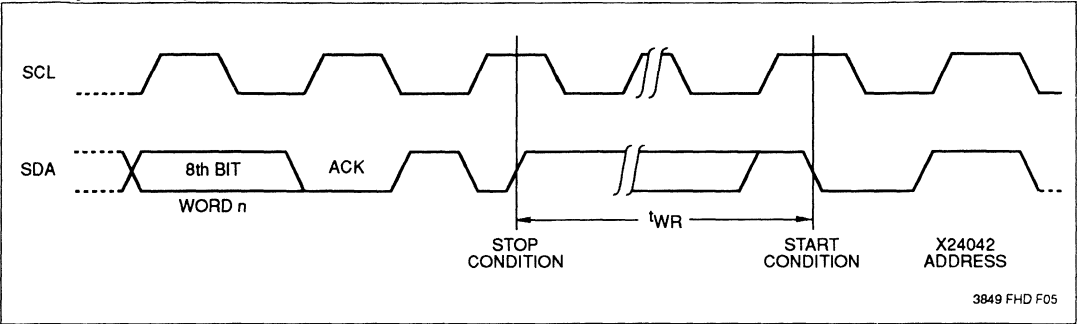
Symbol	Parameter	Min.	Typ.(5)	Max.	Units
$t_{WR}^{(6)}$	Write Cycle Time		5	10	ms

3849 PGM T09

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24042

bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Write Cycle Timing

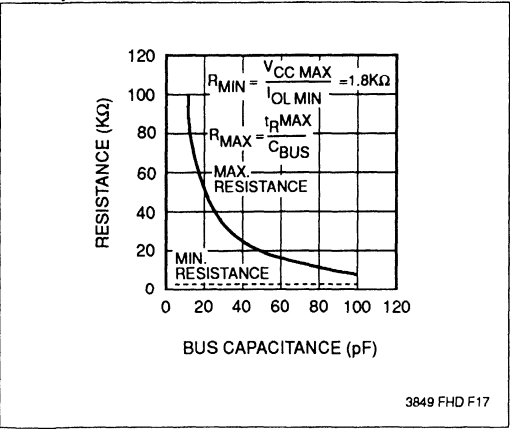


3849 FHD F05

Notes: (5) Typical values are for  $T_A = 25^{\circ}\text{C}$  and nominal supply voltage (5V).

(6)  $t_{WR}$  is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



3849 FHD F17

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**X24042**

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**NOTES**



## Preliminary Information

8K

X24C08

1024 x 8 Bit

## Serial E<sup>2</sup>PROM

### TYPICAL FEATURES

- 2.7V to 5.5V Power Supply
- Low Power CMOS
  - Active Read Current Less Than 1 mA
  - Active Write Current Less Than 3 mA
  - Standby Current Less Than 50  $\mu$ A
- Internally Organized 1024 x 8
- 2 Wire Serial Interface
  - Bidirectional Data Transfer Protocol
- Sixteen Byte Page Write Mode
  - Minimizes Total Write Time Per Byte
- Self Timed Write Cycle
  - Typical Write Cycle Time of 5 ms
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 100 Years
- 8 Pin Mini-DIP, 8 Pin SOIC and 14 Pin SOIC Packages

### DESCRIPTION

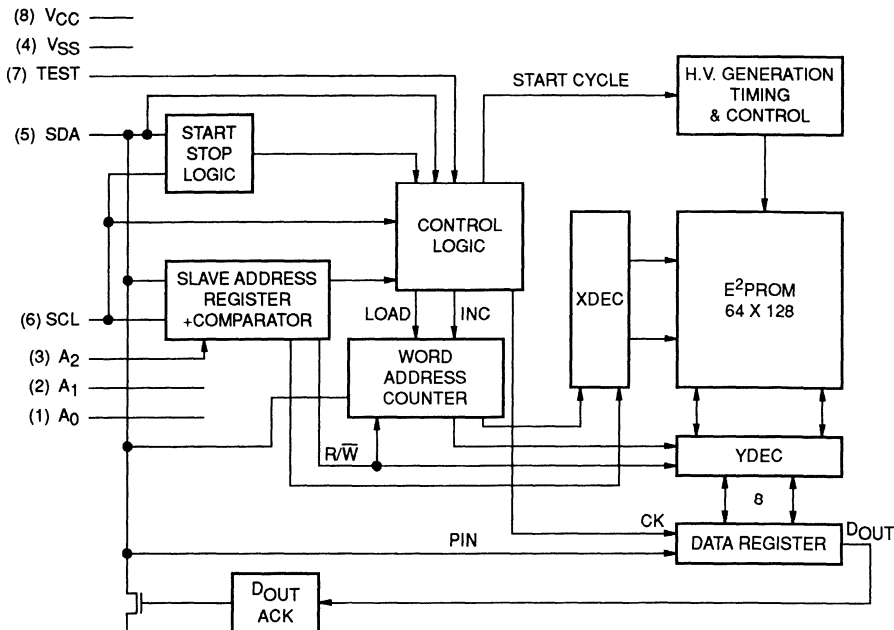
The X24C08 is a CMOS 8,192 bit serial E<sup>2</sup>PROM, internally organized 1024 x 8. The X24C08 features a serial interface and software protocol allowing operation on a simple two wire bus.

The X24C08 is fabricated with Xicor's advanced CMOS Textured Poly Floating Gate Technology.

The X24C08 utilizes Xicor's proprietary Direct Write™ cell providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

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### FUNCTIONAL DIAGRAM



3842 FHD F01

# X24C08

## PIN DESCRIPTIONS

### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

### Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-Up Resistor selection graph at the end of this data sheet.

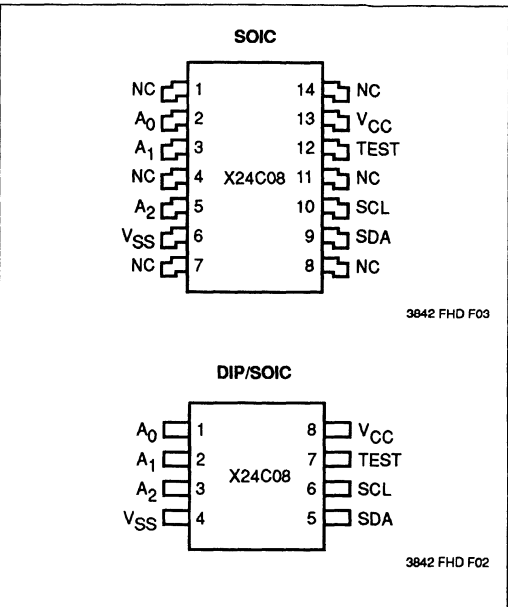
### Address (A<sub>0</sub>, A<sub>1</sub>)

A<sub>0</sub> and A<sub>1</sub> are unused by the X24C08; however, they must be tied to V<sub>SS</sub> to insure proper device operation.

### Address (A<sub>2</sub>)

The A<sub>2</sub> input is used to set the appropriate bit of the seven bit slave address. This input can be used static or actively driven. If used statically, it must be tied to V<sub>SS</sub> or V<sub>CC</sub> as appropriate. If actively driven, it must be driven to V<sub>SS</sub> or to V<sub>CC</sub>.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
A <sub>0</sub> -A <sub>2</sub>	Address Inputs
SDA	Serial Data
SCL	Serial Clock
TEST	Hold at V <sub>SS</sub>
V <sub>SS</sub>	Ground
V <sub>CC</sub>	Supply Voltage
NC	No Connect

3842 PGM T01

# X24C08

## DEVICE OPERATION

The X24C08 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24C08 will be considered a slave in all applications.

## Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

## Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C08 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

## Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24C08 to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

2

Figure 1. Data Validity

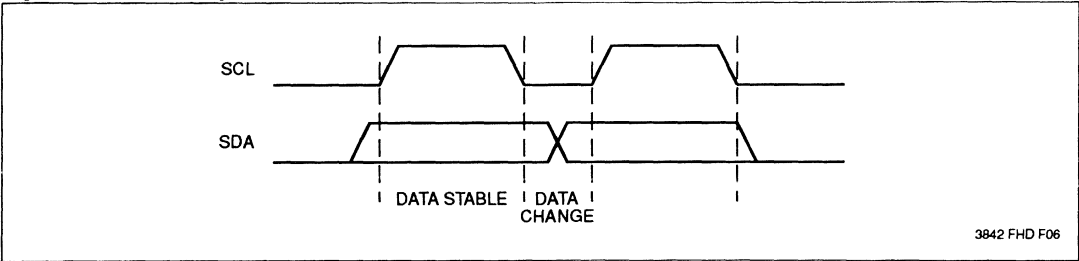
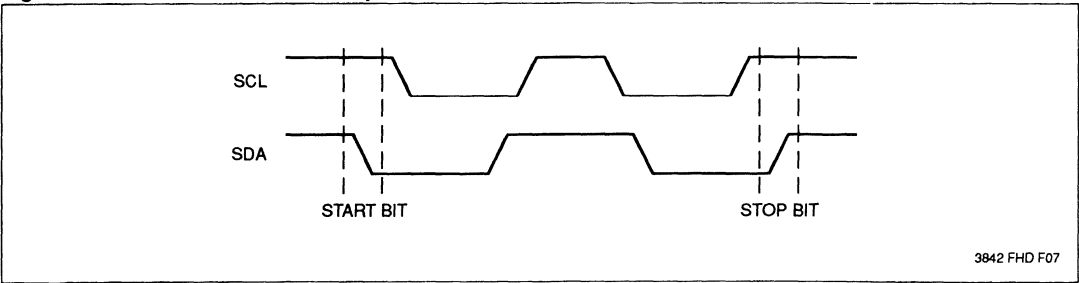


Figure 2. Definition of Start and Stop



## X24C08

### Acknowledge

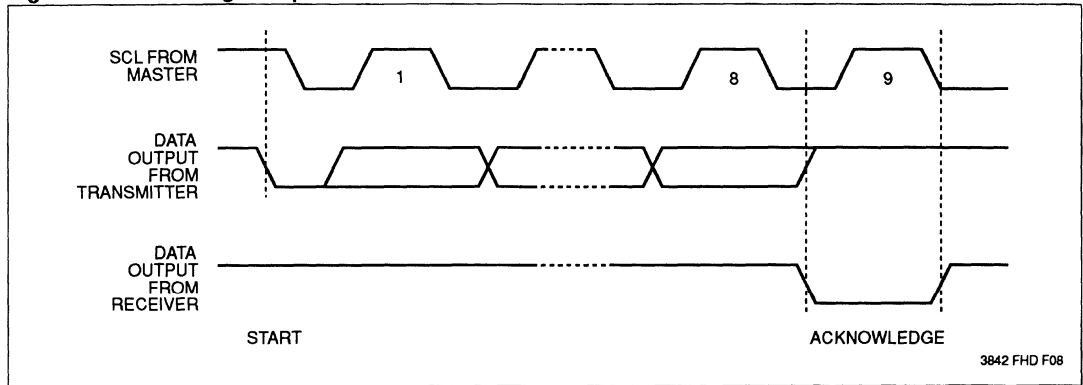
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C08 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been se-

lected, the X24C08 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24C08 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24C08 will continue to transmit data. If an acknowledge is not detected, the X24C08 will terminate further data transmissions. The master must then issue a stop condition to return the X24C08 to the standby power mode and place the device into a known state.

**Figure 3. Acknowledge Response From Receiver**

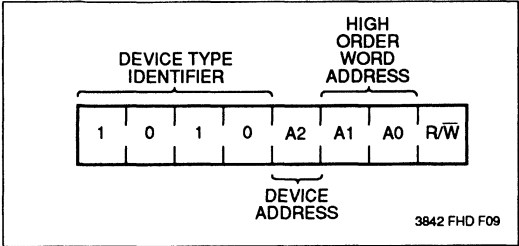


# X24C08

## DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X24C08 this is fixed as 1010[B].

Figure 4. Slave Address



The next bit addresses a particular device. A system could have up to two X24C08 devices on the bus (see Figure 10). The two addresses are defined by the state of the A2 input.

The next two bits of the slave address field are an extension of the array's address and are concatenated with the eight bits of address in the word address field, providing direct access to the whole 1024 x 8 array.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

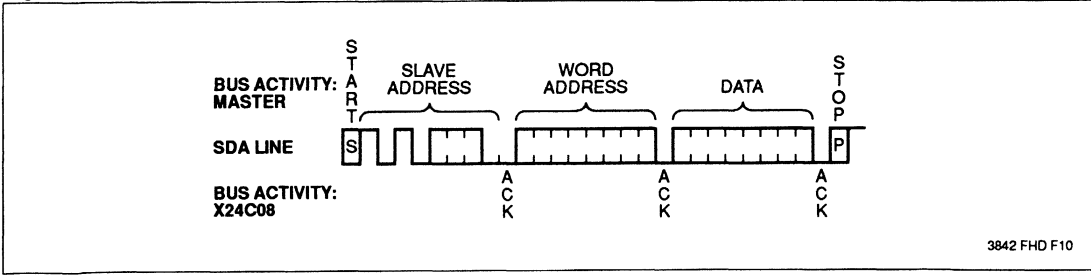
Following the start condition, the X24C08 monitors the SDA bus comparing the slave address being transmitted with its slave address (device type and state of A<sub>2</sub> input.) Upon a correct compare the X24C08 outputs an acknowledge on the SDA line. Depending on the state of the R/W bit, the X24C08 will execute a read or write operation.

## WRITE OPERATIONS

### Byte Write

For a write operation, the X24C08 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of 1024 words in the array. Upon receipt of the word address the X24C08 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24C08 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24C08 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5. Byte Write





# X24C08

## Page Write

The X24C08 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24C08 will respond with an acknowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order six bits of the word address remain constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

## Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24C08 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X24C08 is still busy with the write operation no ACK will be returned. If the X24C08 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation. Refer to Flow 1.

Flow 1. ACK Polling Sequence

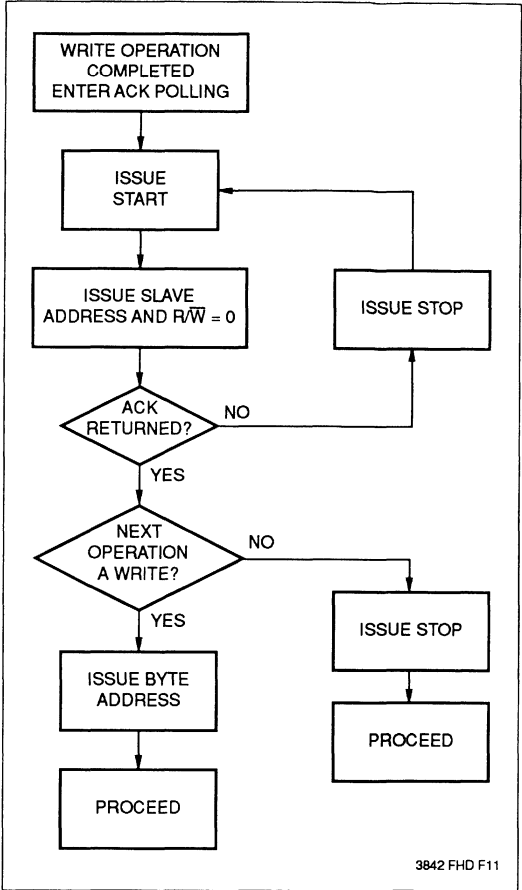
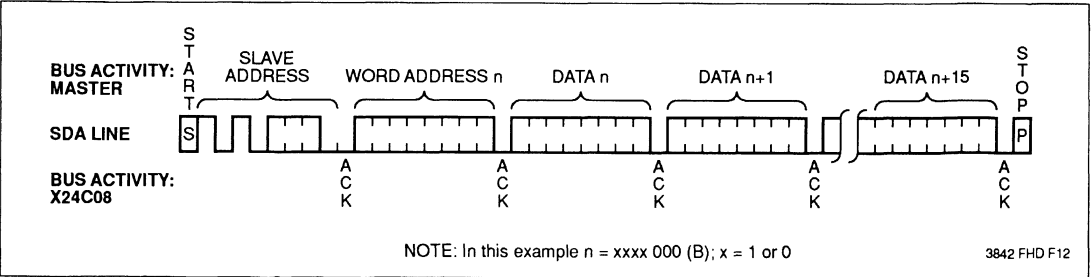


Figure 6. Page Write



X24C08

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/W bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Current Address Read

Internally the X24C08 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/W set to one, the X24C08 issues an acknowledge and transmits the eight bit word.

The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/W bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to one. This will be followed by an acknowledge from the X24C08 and then by the eight bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

2

Figure 7. Current Address Read

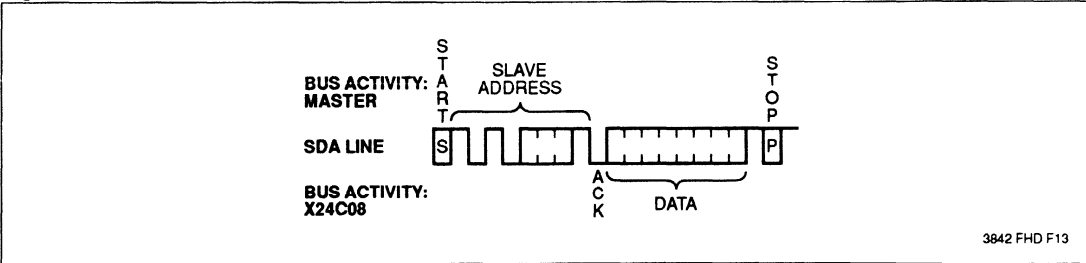
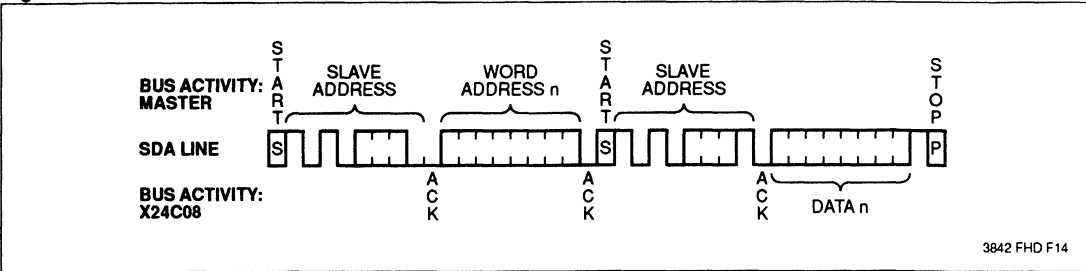


Figure 8. Random Read



# X24C08

## Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The X24C08 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition.

The data output is sequential, with the data from address  $n$  followed by the data from  $n + 1$ . The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 1023) the counter "rolls over" to address 0 and the X24C08 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

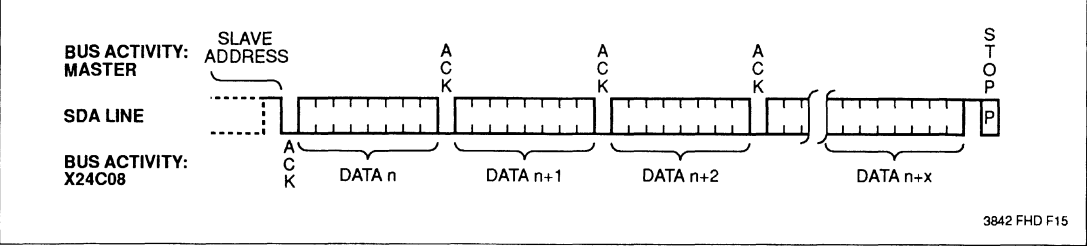
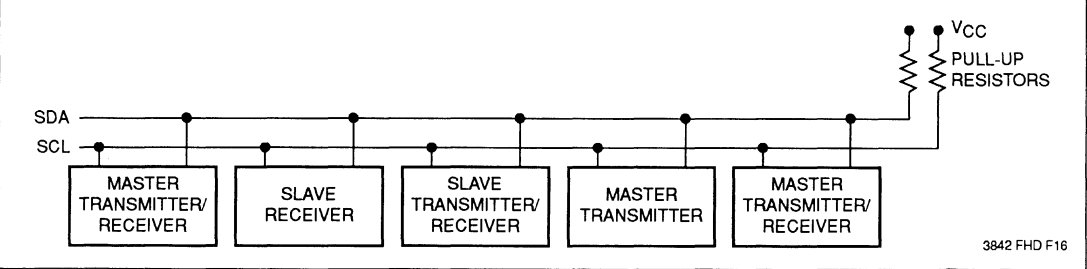


Figure 10. Typical System Configuration



X24C08

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	–65°C to +135°C
Storage Temperature .....	–65°C to +150°C
Voltage on any Pin with Respect to V <sub>SS</sub> .....	–1.0V to +7V
D.C. Output Current .....	5 mA
Lead Temperature (Soldering, 10 Seconds) .....	300°C

\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

Supply Voltage	Limits
X24C08	4.5V to 5.5V
X24C08-3.5	3.5V to 5.5V
X24C08-3	3V to 5.5V
X24C08-2.7	2.7V to 5.5V

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC1</sub>	V <sub>CC</sub> Supply Current (Read)		1	mA	SCL = V <sub>CC</sub> x 0.1/V <sub>CC</sub> x 0.9 Levels @ 100 KHz, SDA = Open, All Other Inputs = GND or V <sub>CC</sub> – 0.3V
I <sub>CC2</sub>	V <sub>CC</sub> Supply Current (Write)		3		
I <sub>SB1</sub> (1)	V <sub>CC</sub> Standby Current		150	μA	
I <sub>SB2</sub> (1)	V <sub>CC</sub> Standby Current		50	μA	SCL = SDA = V <sub>CC</sub> – 0.3V, All Other Inputs = GND or V <sub>CC</sub> , V <sub>CC</sub> = 5.5V
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> (2)	Input Low Voltage	–1.0	V <sub>CC</sub> x 0.3	V	
V <sub>IH</sub> (2)	Input High Voltage	V <sub>CC</sub> x 0.7	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 3 mA

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CAPACITANCE T<sub>A</sub> = 25°C, F = 1.0MHZ, V<sub>CC</sub> = 5V

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (3)	Input/Output Capacitance (SDA)	8	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (3)	Input Capacitance (A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , SCL)	6	pF	V <sub>IN</sub> = 0V

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- Notes: (1) Must perform a stop command prior to measurement.  
(2) V<sub>IL</sub> min and V<sub>IH</sub> max. are for reference only and are not 100% tested.  
(3) This parameter is periodically sampled and not 100% tested.

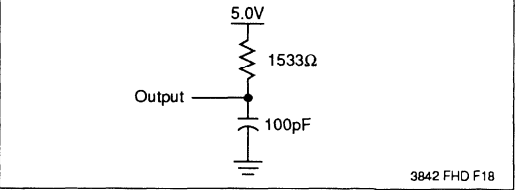
# X24C08

## A.C. CONDITIONS OF TEST

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
I/O Timing Levels	$V_{CC} \times 0.5$

3842 PGM T05

## EQUIVALENT A.C. LOAD CIRCUIT



3842 FHD F18

## A.C. CHARACTERISTICS LIMITS (Over recommended operating conditions, unless otherwise specified.)

### Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
$t_{SCL}$	SCL Clock Frequency	0	100	KHz
$t_I$	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
$t_{AA}$	SCL Low to SDA Data Out Valid	0.3	3.5	μs
$t_{BUF}$	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
$t_{LOW}$	Clock Low Period	4.7		μs
$t_{HIGH}$	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time	4.7		μs
$t_{HD:DAT}$	Data In Hold Time	0		μs
$t_{SU:DAT}$	Data In Setup Time	250		ns
$t_R$	SDA and SCL Rise Time		1	μs
$t_F$	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
$t_{DH}$	Data Out Hold Time	300		ns

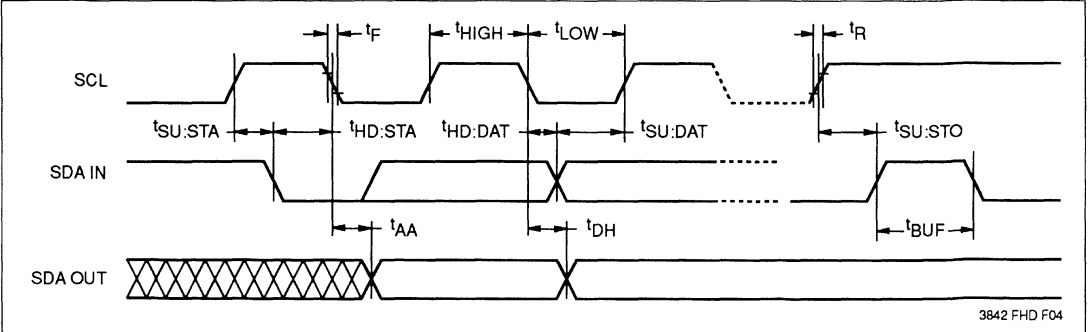
3842 PGM T06

## POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(4)}$	Power-Up to Read Operation	1	ms
$t_{PUW}^{(4)}$	Power-Up to Write Operation	5	ms

3842 PGM T07

## Bus Timing



3842 FHD F04

**Note:** (4)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

# X24C08

## WRITE CYCLE LIMITS

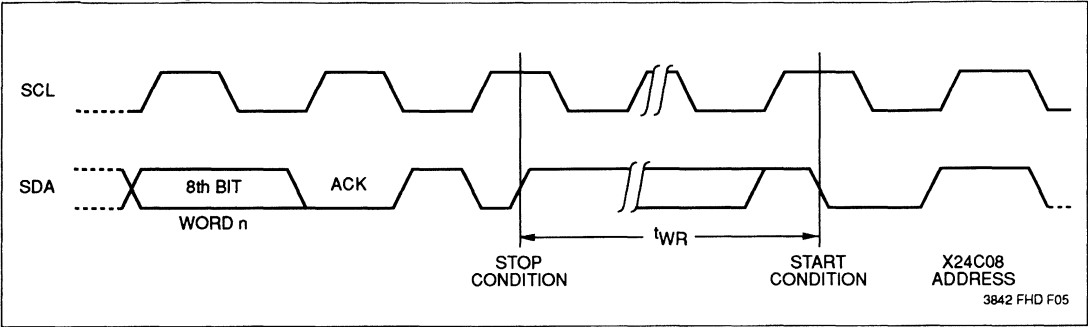
Symbol	Parameter	Min.	Typ.(5)	Max.	Units
$t_{WR}^{(6)}$	Write Cycle Time		5	10	ms

3842 PGM T08

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C08

bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

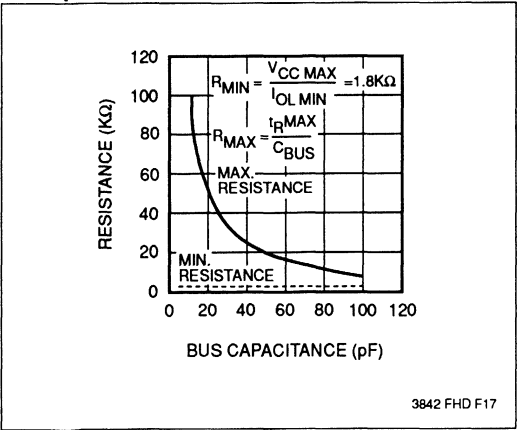
## Write Cycle Timing



Notes: (5) Typical values are for  $T_A = 25^{\circ}\text{C}$  and nominal supply voltage (5V).

(6)  $t_{WR}$  is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

## Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**X24C08**

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**NOTES**



## Preliminary Information

16K

X24C16

2048 x 8 Bit

## Serial E<sup>2</sup>PROM

### FEATURES

- 2.7V to 5.5V Power Supply
- Low Power CMOS
  - Active Read Current Less Than 1 mA
  - Active Write Current Less Than 3 mA
  - Standby Current Less Than 50  $\mu$ A
- Internally Organized 2048 x 8
- 2 Wire Serial Interface
  - Bidirectional Data Transfer Protocol
- Sixteen Byte Page Write Mode
  - Minimizes Total Write Time Per Byte
- Self Timed Write Cycle
  - Typical Write Cycle Time of 5 ms
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 100 Years
- 8 Pin Mini-DIP, 8 Pin SOIC and 14 Pin SOIC Packages

### DESCRIPTION

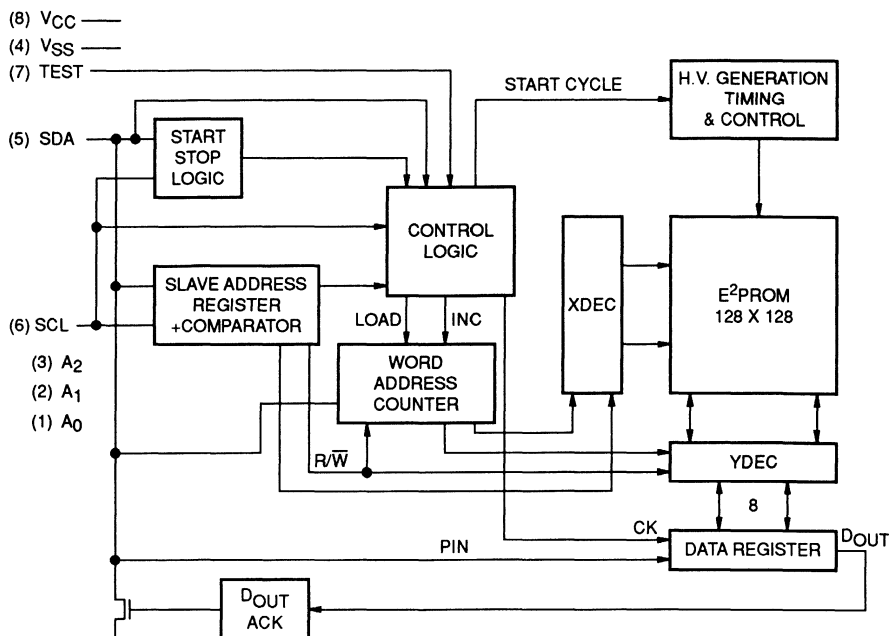
The X24C16 is a CMOS 16,384 bit serial E<sup>2</sup>PROM, internally organized 2048 X 8. The X24C16 features a serial interface and software protocol allowing operation on a simple two wire bus.

The X24C16 is fabricated with Xicor's advanced CMOS Textured Poly Floating Gate Technology.

The X24C16 utilizes Xicor's proprietary Direct Write™ cell providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

2

### FUNCTIONAL DIAGRAM



3840 FHD F01



# X24C16

## PIN DESCRIPTIONS

### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

### Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-Up Resistor selection graph at the end of this data sheet.

### Address ( $A_0$ , $A_1$ , $A_2$ )

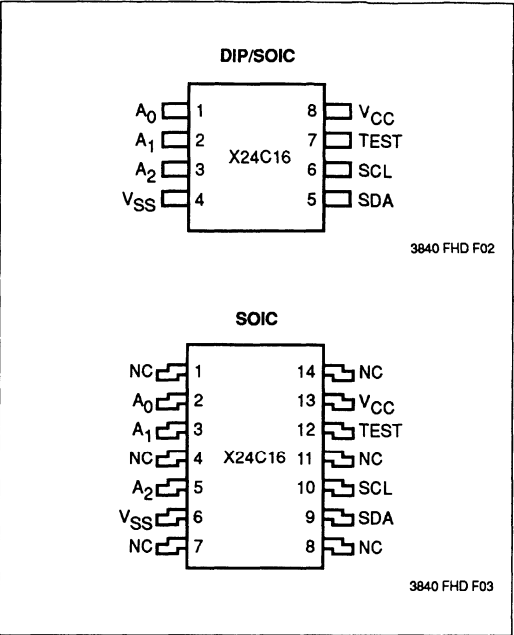
The  $A_0$ ,  $A_1$  and  $A_2$  inputs are unused by the X24C16, however, they must be tied to  $V_{SS}$  to insure proper device operation.

## PIN NAMES

Symbol	Description
$A_0$ – $A_2$	Address Inputs
SDA	Serial Data
SCL	Serial Clock
TEST	Hold at $V_{SS}$
$V_{SS}$	Ground
$V_{CC}$	Supply Voltage
NC	No Connect

3840 PGM T01

## PIN CONFIGURATION



# X24C16

## DEVICE OPERATION

The X24C16 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24C16 will be considered a slave in all applications.

## Clock and Data Conventions

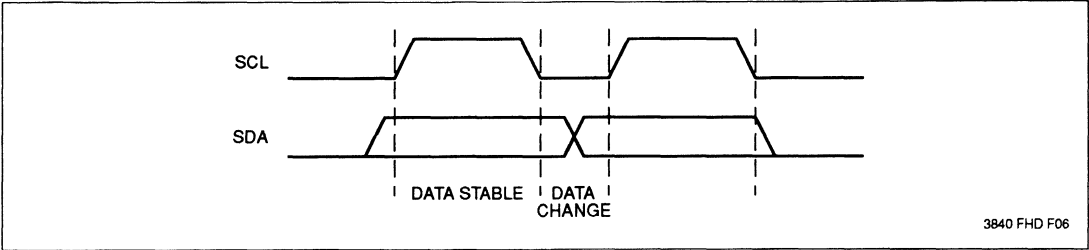
Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

## Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C16 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

2

Figure 1. Data Validity



## X24C16

### Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24C16 to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

### Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C16 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24C16 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24C16 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24C16 will continue to transmit data. If an acknowledge is not detected, the X24C16 will terminate further data transmissions. The master must then issue a stop condition to return the X24C16 to the standby power mode and place the device into a known state.

Figure 2. Definition of Start and Stop

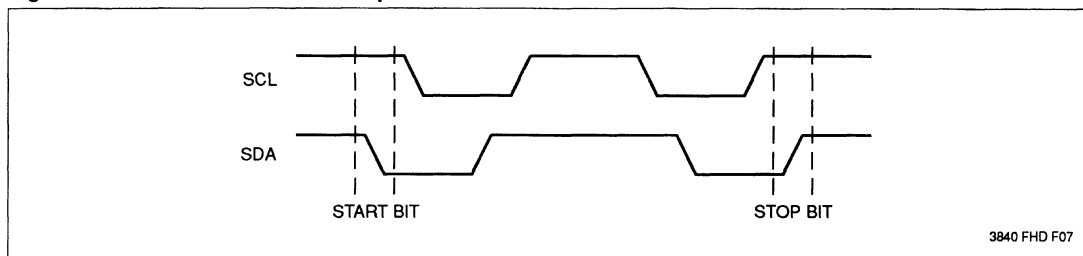
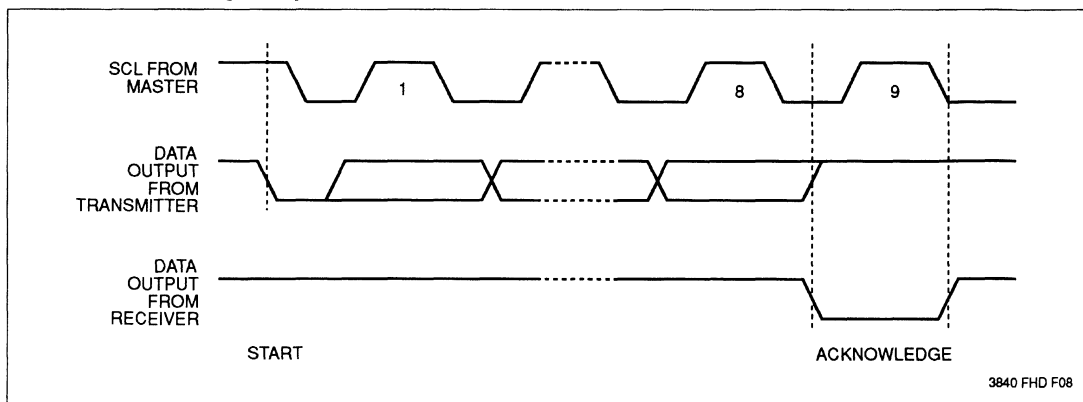


Figure 3. Acknowledge Response From Receiver

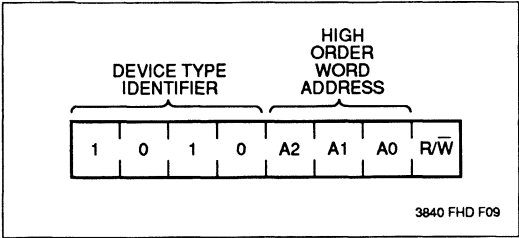


# X24C16

## DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X24C16 this is fixed as 1010[B].

Figure 4. Slave Address



The next three bits of the slave address field are the bank select bits. They are used by the host to toggle between the eight 256 x 8 banks of memory. These are, in effect, the most significant bits for the word address.

The next three bits of the slave address are an extension of the array's address and are concatenated with the

eight bits of address in the word address field, providing direct access to the whole 2048 x 8 array.

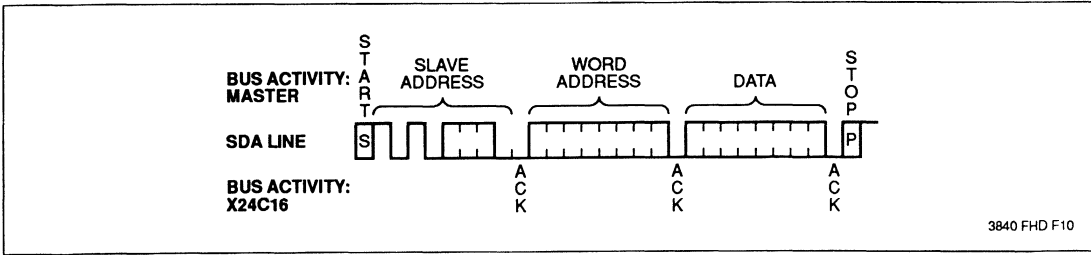
Following the start condition, the X24C16 monitors the SDA bus comparing the slave address being transmitted with its slave address (device type). Upon a correct compare the X24C16 outputs an acknowledge on the SDA line. Depending on the state of the R/W bit, the X24C16 will execute a read or write operation.

## WRITE OPERATIONS

### Byte Write

For a write operation, the X24C16 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 2048 words in the array. Upon receipt of the word address the X24C16 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24C16 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24C16 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5. Byte Write



# X24C16

## Page Write

The X24C16 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24C16 will respond with an acknowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order seven bits of the address remain constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

## Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24C16 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X24C16 is still busy with the write operation no ACK will be returned. If the X24C16 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation. Refer to Flow 1.

## Flow 1. ACK Polling Sequence

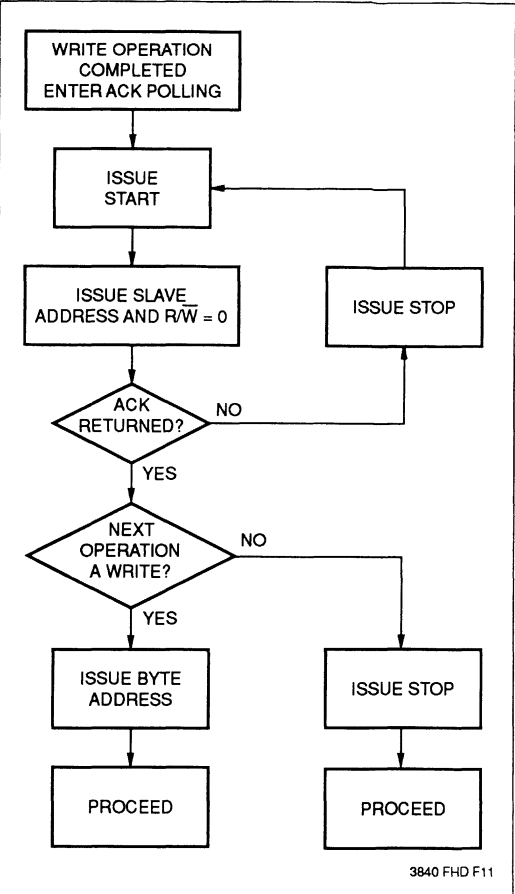
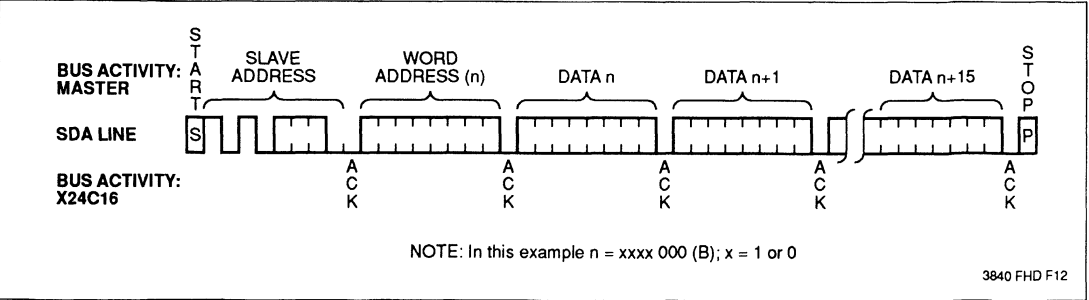


Figure 6. Page Write



X24C16

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/W bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Current Address Read

Internally the X24C16 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with the R/W bit set to one, the X24C16 issues an acknowledge and transmits the eight

bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/W bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to one. This will be followed by an acknowledge from the X24C16 and then by the eight bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

2

Figure 7. Current Address Read

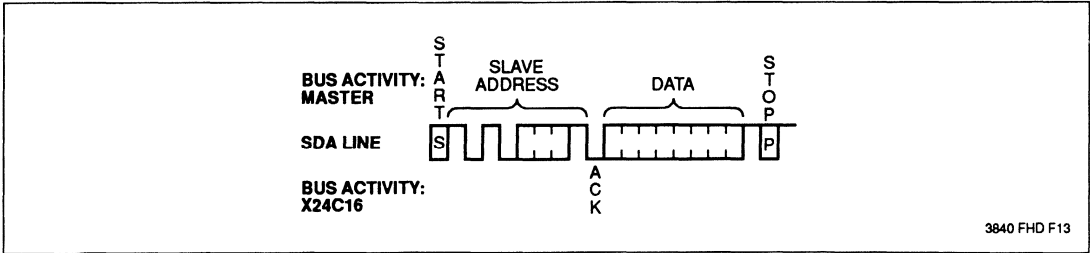
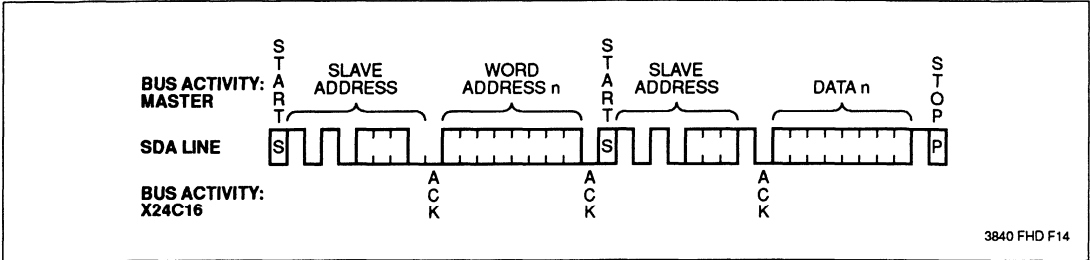


Figure 8. Random Read



# X24C16

## Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other read modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24C16 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition.

The data output is sequential, with the data from address  $n$  followed by the data from  $n + 1$ . The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 2047), the counter “rolls over” to 0 and the X24C16 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

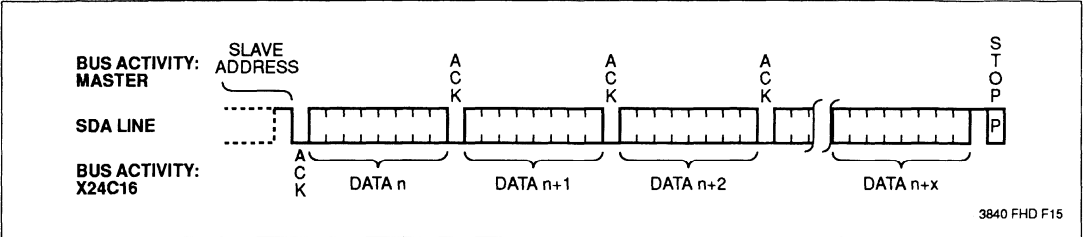
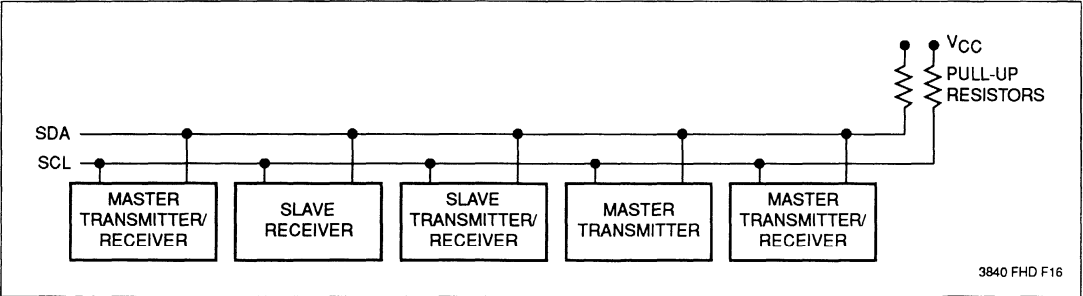


Figure 10. Typical System Configuration



X24C16

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	–65°C to +135°C
Storage Temperature .....	–65°C to +150°C
Voltage on any Pin with Respect to V <sub>SS</sub> .....	–1.0V to +7.0V
D.C. Output Current .....	5 mA
Lead Temperature (Soldering, 10 Seconds) .....	300°C

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

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\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Supply Voltage	Limits
X24C16	4.5V to 5.5V
X24C16–3.5	3.5V to 5.5V
X24C16–3	3V to 5.5V
X24C16–2.7	2.7V to 5.5V

3840 PGM T10

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC1</sub>	V <sub>CC</sub> Supply Current (read)		1	mA	SCL = V <sub>CC</sub> × 0.1/V <sub>CC</sub> × 0.9 Levels @ 100 KHz, SDA = Open, All Other Inputs = GND or V <sub>CC</sub> – 0.3V
I <sub>CC2</sub>	V <sub>CC</sub> Supply Current (write)		3		
I <sub>SB1</sub> (1)	V <sub>CC</sub> Standby Current		150	μA	SCL = SDA = V <sub>CC</sub> – 0.3V, All Other Inputs = GND or V <sub>CC</sub> , V <sub>CC</sub> = 5.5V
I <sub>SB2</sub> (1)	V <sub>CC</sub> Standby Current		50	μA	SCL = SDA = V <sub>CC</sub> – 0.3V, All Other Inputs = GND or V <sub>CC</sub> , V <sub>CC</sub> = 3.3V +10%
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> (2)	Input Low Voltage	–1.0	V <sub>CC</sub> × 0.3	V	
V <sub>IH</sub> (2)	Input High Voltage	V <sub>CC</sub> × 0.7	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 3 mA

3840 PGM T03

CAPACITANCE T<sub>A</sub> = 25°C, f = 1.0 MHz, V<sub>CC</sub> = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C <sub>I/O</sub> (3)	Input/Output Capacitance (SDA)	8	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (3)	Input Capacitance (A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , SCL)	6	pF	V <sub>IN</sub> = 0V

3840 PGM T05

- Notes: (1) Must perform a stop command prior to measurement.  
(2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
(3) This parameter is periodically sampled and not 100% tested.



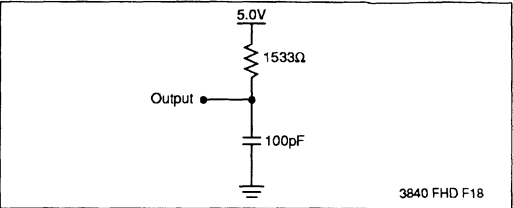
# X24C16

## A.C. CONDITIONS OF TEST

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$

3840 PGM T02

## EQUIVALENT A.C. LOAD CIRCUIT



3840 FHD F18

## A.C. CHARACTERISTICS LIMITS (Over the recommended operating conditions unless otherwise specified.) Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
$f_{SCL}$	SCL Clock Frequency	0	100	KHz
$T_I$	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
$t_{AA}$	SCL Low to SDA Data Out Valid	0.3	3.5	$\mu$ s
$t_{BUF}$	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		$\mu$ s
$t_{HD:STA}$	Start Condition Hold Time	4.0		$\mu$ s
$t_{LOW}$	Clock Low Period	4.7		$\mu$ s
$t_{HIGH}$	Clock High Period	4.0		$\mu$ s
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		$\mu$ s
$t_{HD:DAT}$	Data In Hold Time	0		$\mu$ s
$t_{SU:DAT}$	Data In Setup Time	250		ns
$t_R$	SDA and SCL Rise Time		1	$\mu$ s
$t_F$	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		$\mu$ s
$t_{DH}$	Data Out Hold Time	300		ns

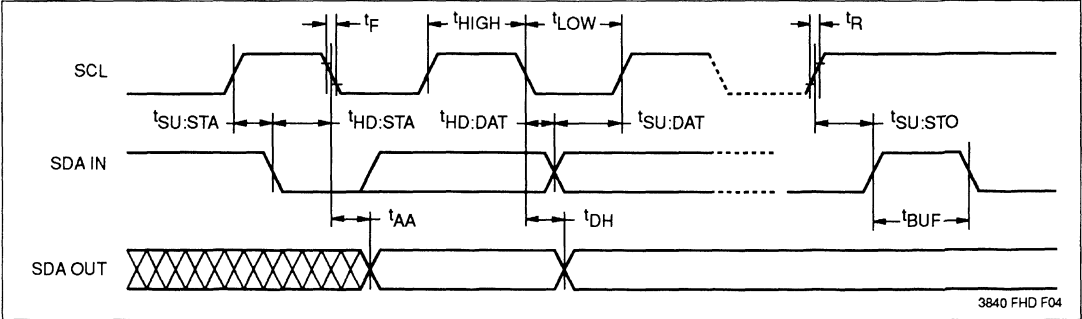
3840 PGM T06

## POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(4)}$	Power-up to Read Operation	1	ms
$t_{PUW}^{(4)}$	Power-up to Write Operation	5	ms

3840 PGM T07

## Bus Timing



3840 FHD F04

**Notes:** (4)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

X24C16

WRITE CYCLE LIMITS

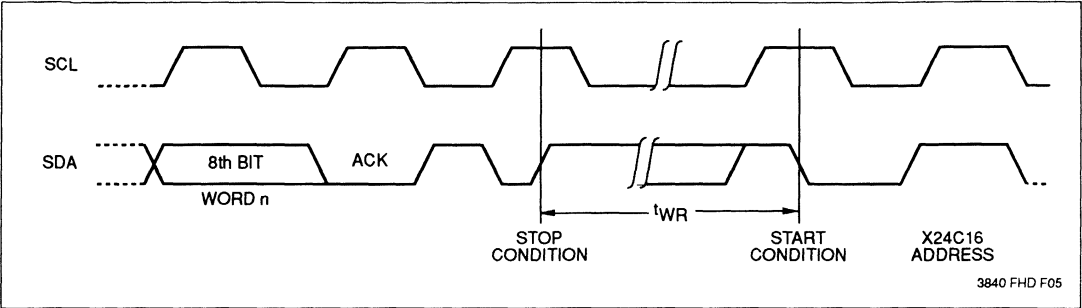
Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t <sub>WR</sub> (6)	Write Cycle Time		5	10	ms

3840 PGM T08

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C16

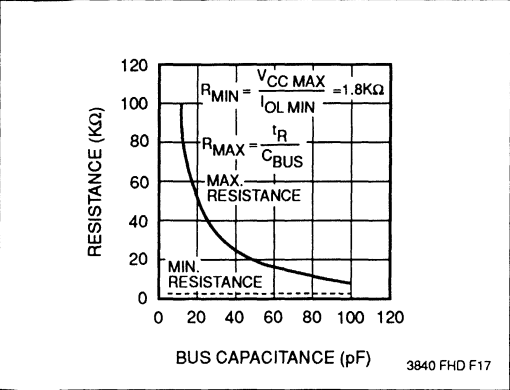
bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Write Cycle Timing



- Notes: (5) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage (5V)  
(6) t<sub>WR</sub> is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**X24C16**

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**NOTES**



## Preliminary Information

16K

X24164

2048 x 8 Bit

## Serial E<sup>2</sup>PROM

### FEATURES

- 2.7V to 5.5V Power Supply
- Low Power CMOS
  - Active Read Current Less Than 1 mA
  - Active Write Current Less Than 3 mA
  - Standby Current Less Than 50  $\mu$ A
- Internally Organized 2048 x 8
- 2 Wire Serial Interface
  - Bidirectional Data Transfer Protocol
- Sixteen Byte Page Write Mode
  - Minimizes Total Write Time Per Byte
- Self Timed Write Cycle
  - Typical Write Cycle Time of 5 ms
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 100 Years
- Pin and Function Compatible with X24C16
- 8-Pin Plastic DIP and 8-Lead SOIC Packages

### DESCRIPTION

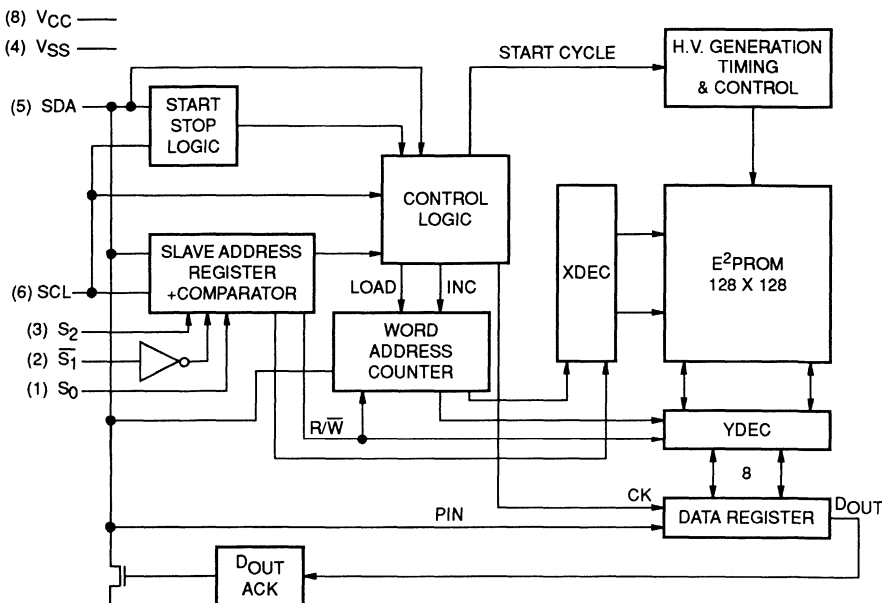
The X24164 is a CMOS 16,384 bit serial E<sup>2</sup>PROM, internally organized 2048 x 8. The X24164 features a serial interface and software protocol allowing operation on a simple two wire bus.

Three device select inputs ( $S_0$ – $S_2$ ) allow up to eight devices to share a common two wire bus.

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

2

### FUNCTIONAL DIAGRAM



3846 FHD F01

# X24164

## PIN DESCRIPTIONS

### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

### Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-Up Resistor selection graph at the end of this data sheet.

### Device Select ( $S_0$ , $\overline{S_1}$ , $S_2$ )

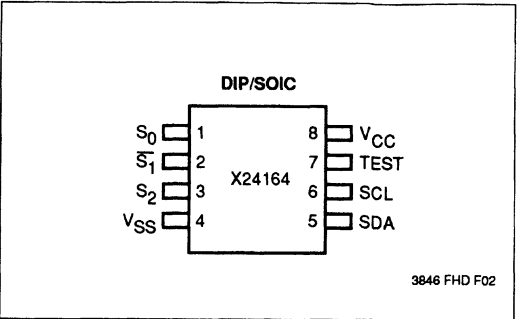
The device select inputs ( $S_0$ ,  $\overline{S_1}$ ,  $S_2$ ) are used to set the second, third and fourth bits of the 8 bit slave address. This allows up to eight X24164's to share a common bus. These inputs can be static or actively driven. If used statically they must be tied to  $V_{SS}$  or  $V_{CC}$  as appropriate. If actively driven, they must be driven to  $V_{SS}$  or  $V_{CC}$ . To be compatible with the X24C16 these pins must all be tied to  $V_{SS}$ .

### Pin Names

Symbol	Description
$S_0$ - $S_2$	Device Select Inputs
SDA	Serial Data
SCL	Serial Clock
TEST	Hold at $V_{SS}$
$V_{SS}$	Ground
$V_{CC}$	Supply Voltage

3846 PGM T01

## PIN CONFIGURATION



# X24164

## DEVICE OPERATION

The X24164 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24164 will be considered a slave in all applications.

## Clock and Data Conventions

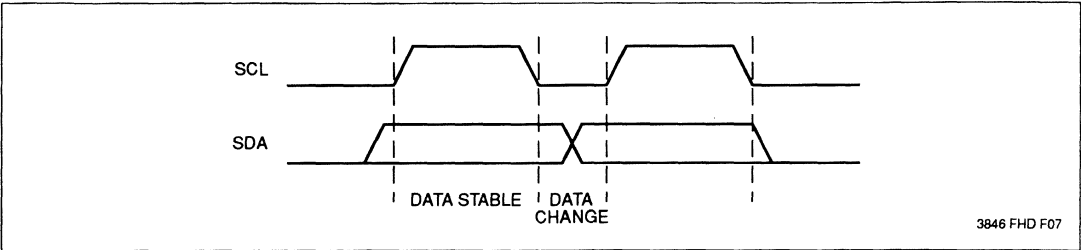
Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

### Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24164 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

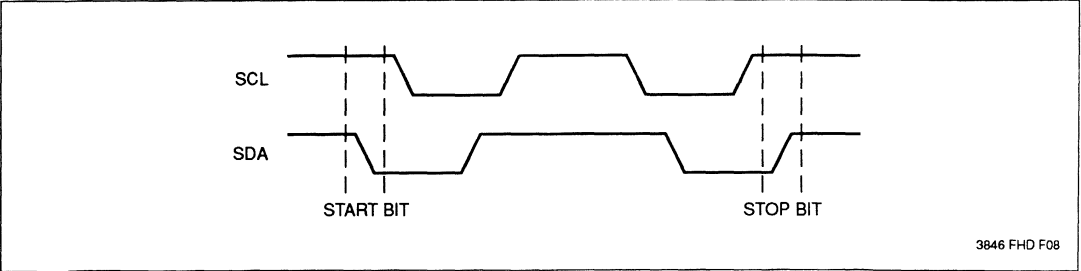
2

Figure 1. Data Validity



- Notes: (5) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage (5V)  
(6)  $t_{WR}$  is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

Figure 2. Definition of Start and Stop



## X24164

### Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

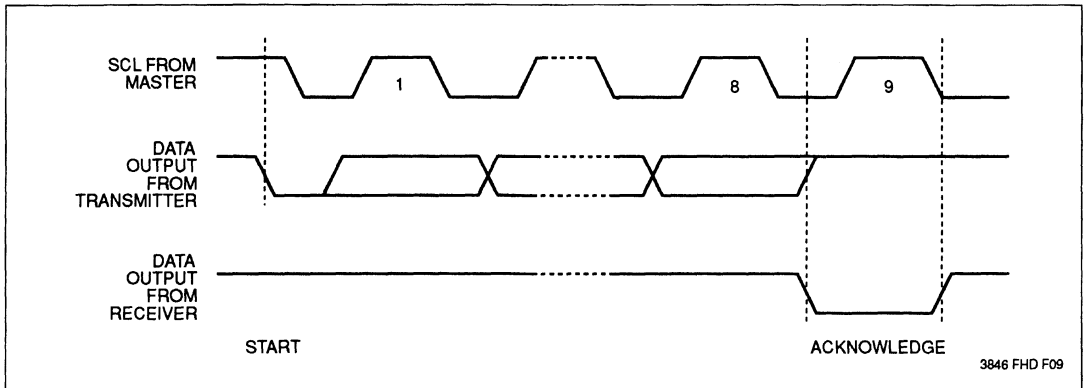
### Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24164 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24164 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24164 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24164 will continue to transmit data. If an acknowledge is not detected, the X24164 will terminate further data transmissions. The master must then issue a stop condition to return the X24164 to the standby power mode and place the device into a known state.

**Figure 3. Acknowledge Response From Receiver**

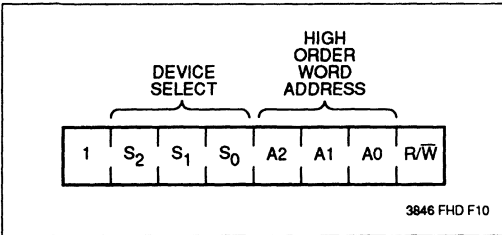


# X24164

## DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant bit of the slave address is a one (see Figure 4). The next three bits are the device select bits. A system could have up to eight X24164's on the bus. The eight addresses are defined by the state of the  $S_0$ ,  $\bar{S}_1$ , and  $S_2$  inputs.  $S_1$  of the slave address must be the inverse of the  $\bar{S}_1$  input pin.

Figure 4. Slave Address



The next three bits of the slave address are an extension of the array's address and are concatenated with the eight bits of address in the word address field, providing direct access to the whole 2048 x 8 array.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

Following the start condition, the X24164 monitors the SDA bus comparing the slave address being transmitted with its slave address device type identifier. Upon a correct compare the X24164 outputs an acknowledge on the SDA line. Depending on the state of the R/W bit, the X24164 will execute a read or write operation.

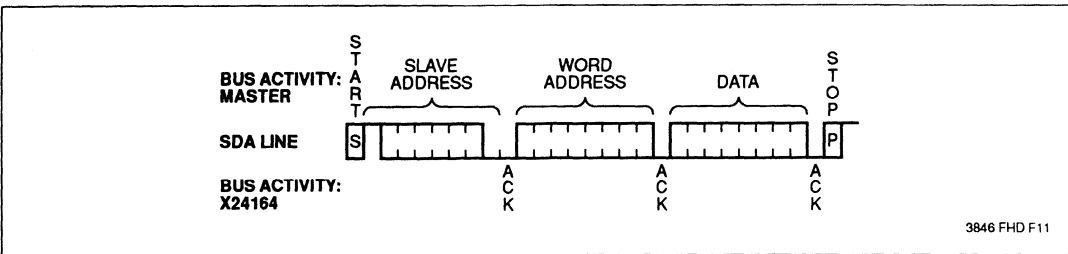
2

## WRITE OPERATIONS

### Byte Write

For a write operation, the X24164 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of 2048 words in the array. Upon receipt of the word address the X24164 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24164 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24164 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5. Byte Write





## X24164

### Page Write

The X24164 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24164 will respond with an acknowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order seven bits of the word address remain constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

### Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24164 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a **write operation**. If the X24164 is still busy with the write operation no ACK will be returned. If the X24164 has completed the **write operation** an ACK will be returned and the host can then proceed with the next read or write operation. Refer to Flow 1.

### Flow 1. ACK Polling Sequence

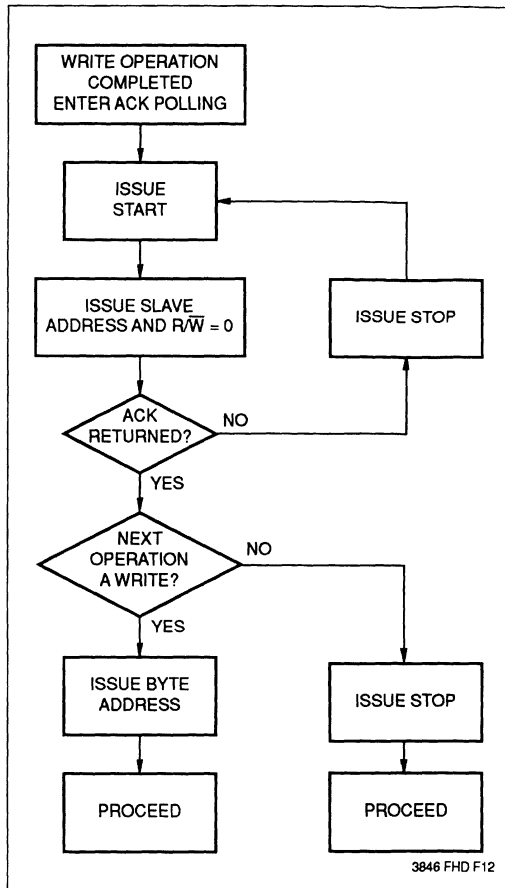
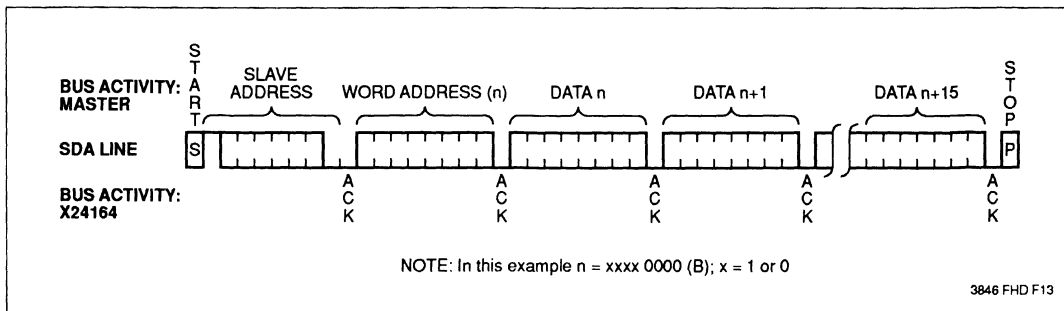


Figure 6. Page Write



# X24164

## READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the  $R/\overline{W}$  bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

### Current Address Read

Internally the X24164 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address  $n$ , the next read operation would access data from address  $n + 1$ . Upon receipt of the slave address with the  $R/\overline{W}$  set to one, the X24164 issues an acknowledge and transmits the eight bit word.

The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

### Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the  $R/\overline{W}$  bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the  $R/\overline{W}$  bit set to one. This will be followed by an acknowledge from the X24164 and then by the eight bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 7. Current Address Read

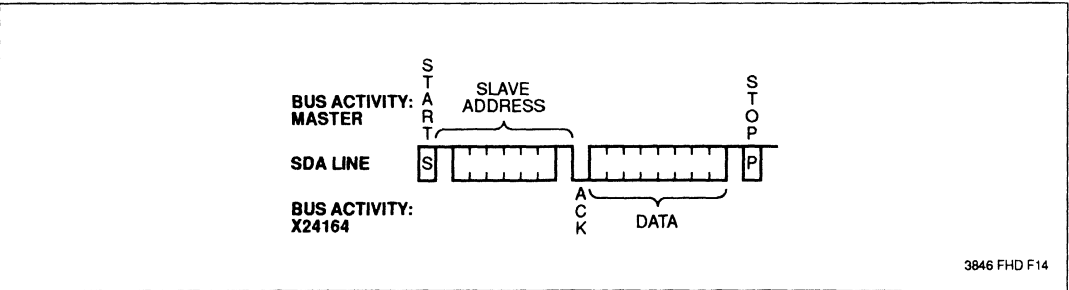
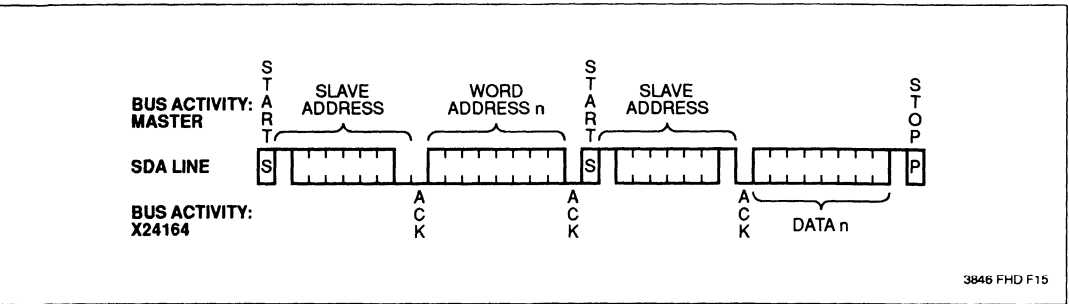


Figure 8. Random Read



# X24164

## Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24164 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition.

The data output is sequential, with the data from address  $n$  followed by the data from  $n + 1$ . The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 2047), the counter "rolls over" to 0 and the X24164 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

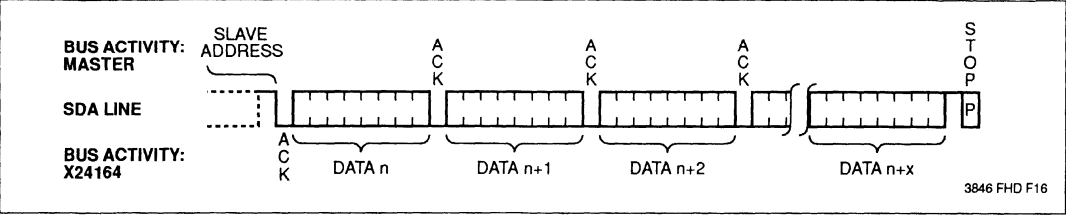
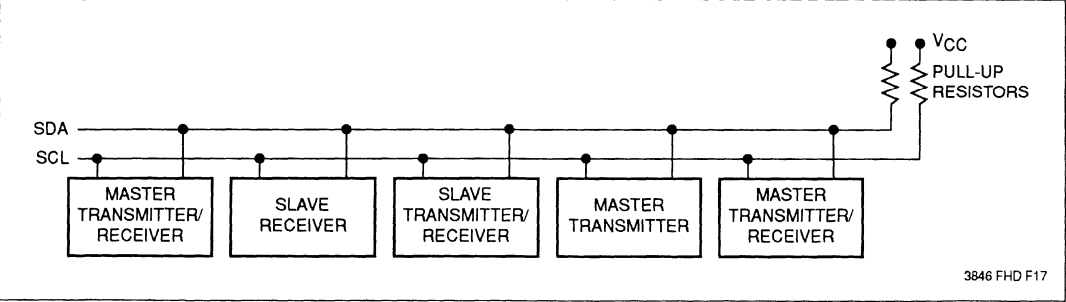


Figure 10. Typical System Configuration



# X24164

2

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X24164 .....	–65°C to +135°C
Storage Temperature .....	–65°C to +150°C
Voltage on any Pin with	
Respect to V <sub>SS</sub> .....	–1.0V to +7.0V
D.C. Output Current .....	5 mA
Lead Temperature (Soldering, 10 Seconds) .....	300°C

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3846 PGM T02

Supply Voltage	Limits
X24164	4.5V to 5.5V
X24164-3	3V to 5.5V
X24164-2.7	2.7V to 5.5V

3846 PGM T03

## D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC1</sub>	V <sub>CC</sub> Supply Current (Read)		1	mA	SCL = V <sub>CC</sub> X 0.1/V <sub>CC</sub> X 0.9 Levels @ 100 KHz, SDA = Open, All Other Inputs = GND or V <sub>CC</sub> – 0.3V
I <sub>CC2</sub>	V <sub>CC</sub> Supply Current (Write)		3	mA	
I <sub>SB1</sub> <sup>(1)</sup>	V <sub>CC</sub> Standby Current		150	μA	SCL = SDA = V <sub>CC</sub> , All Other Inputs = GND or V <sub>CC</sub> – 0.3V, V <sub>CC</sub> = 5V ± 10%
I <sub>SB2</sub> <sup>(1)</sup>	V <sub>CC</sub> Standby Current		50	μA	SCL = SDA = V <sub>CC</sub> , All Other Inputs = GND or V <sub>CC</sub> – 0.3V, V <sub>CC</sub> = 3V
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> <sup>(2)</sup>	Input Low Voltage	–1.0	V <sub>CC</sub> x 0.3	V	
V <sub>IH</sub> <sup>(2)</sup>	Input High Voltage	V <sub>CC</sub> x 0.7	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 3 mA

3846 PGM T04

## CAPACITANCE T<sub>A</sub> = 25°C, f = 1.0 MHz, V<sub>CC</sub> = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C <sub>IO</sub> <sup>(3)</sup>	Input/Output Capacitance (SDA)	8	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> <sup>(3)</sup>	Input Capacitance (S <sub>0</sub> , S <sub>1</sub> , S <sub>2</sub> , SCL)	6	pF	V <sub>IN</sub> = 0V

3846 PGM T05

- Notes: (1) Must perform a stop command prior to measurement.  
(2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not 100% tested.  
(3) This parameter is periodically sampled and not 100% tested.

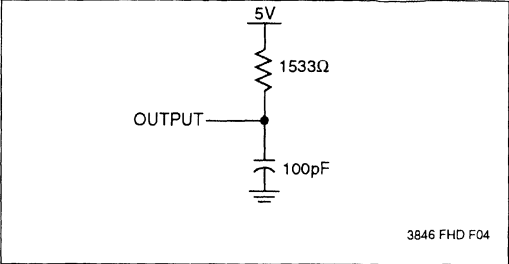
X24164

A.C. CONDITIONS OF TEST

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$

3846 PGM T06

EQUIVALENT A.C. LOAD CIRCUIT



3846 FHD F04

A.C. CHARACTERISTICS (Over recommended operating range unless otherwise specified)

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f <sub>SCL</sub>	SCL Clock Frequency	0	100	KHz
T <sub>I</sub>	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t <sub>AA</sub>	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t <sub>BUF</sub>	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		μs
t <sub>HD:STA</sub>	Start Condition Hold Time	4.0		μs
t <sub>LOW</sub>	Clock Low Period	4.7		μs
t <sub>HIGH</sub>	Clock High Period	4.0		μs
t <sub>SU:STA</sub>	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
t <sub>HD:DAT</sub>	Data In Hold Time	0		μs
t <sub>SU:DAT</sub>	Data In Setup Time	250		ns
t <sub>R</sub>	SDA and SCL Rise Time		1	μs
t <sub>F</sub>	SDA and SCL Fall Time		300	ns
t <sub>SU:STO</sub>	Stop Condition Setup Time	4.7		μs
t <sub>DH</sub>	Data Out Hold Time	300		ns

3846 PGM T07

POWER-UP TIMING<sup>(4)</sup>

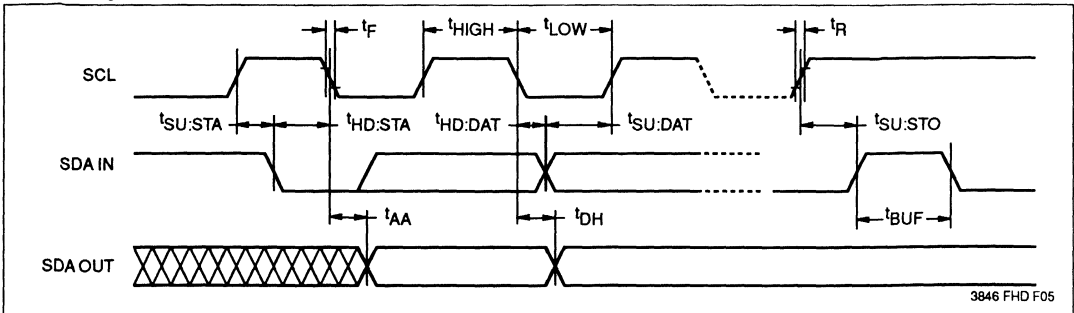
Symbol	Parameter	Max.	Units
t <sub>PUR</sub>	Power-up to Read Operation	1	ms
t <sub>PUW</sub>	Power-up to Write Operation	5	ms

3846 PGM T08

**Notes:** (4) t<sub>PUR</sub> and t<sub>PUW</sub> are the delays required from the time V<sub>CC</sub> is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

X24164

Bus Timing



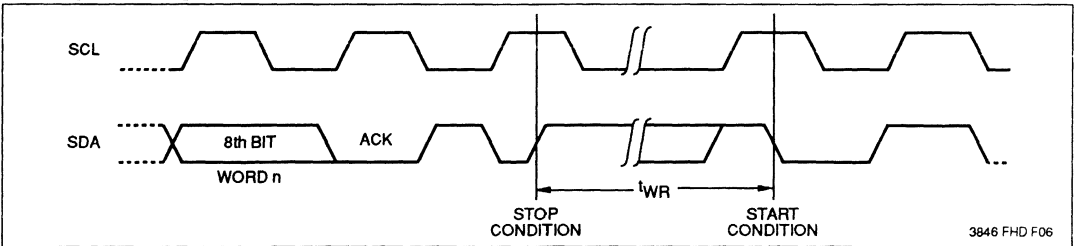
Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
$T_{WR}^{(6)}$	Write Cycle Time		5	10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24164

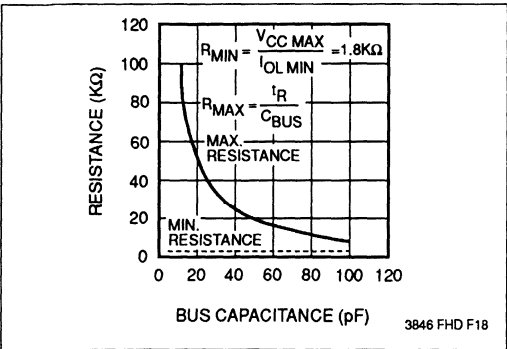
bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Write Cycle Timing



**Notes:** (5) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage (5V).  
(6)  $t_{WR}$  is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**X24164**

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**NOTES**



## Preliminary Information

2K

X25C02

256 x 8 Bit

## SPI Serial E<sup>2</sup>PROM

### FEATURES

- 1MHz Clock Rate
- 256 X 8 Bits
  - 4 Byte Page Mode
- Low Power CMOS
  - 150 $\mu$ A Standby Current
  - 2mA Active Current
- 3V To 5.5V Power Supply
- Built-In Inadvertent Write Protection
  - Power-Up/Power-Down protection circuitry
  - Write Latch
  - Write Protect Pin
- Self-Timed Write Cycle
  - 5mS Write Cycle Time (Typical)
- High Reliability
  - Endurance: 100,000 cycles per byte
  - Data Retention: 100 Years
  - ESD protection: 2000V on all pins
- 8-Pin Mini-DIP Package
- 8-Pin SOIC Package

### DESCRIPTION

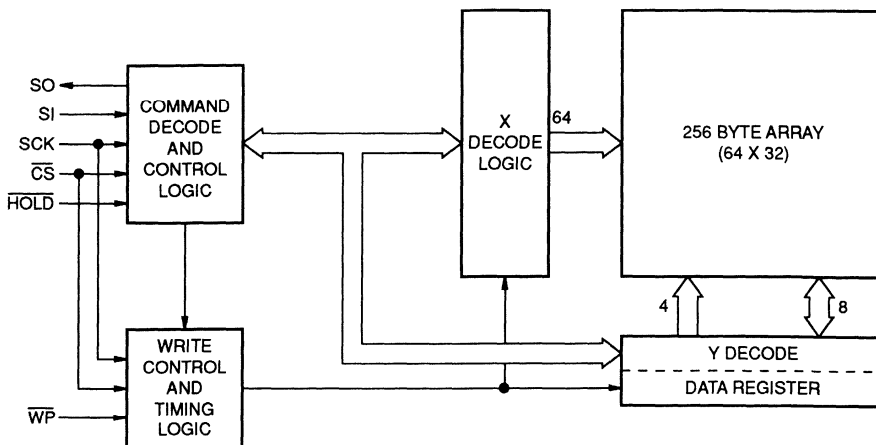
The X25C02 is a CMOS 2048 bit serial E<sup>2</sup>PROM, internally organized as 256 x 8. The X25C02 features a serial interface and software protocol allowing operation on a simple three wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ( $\overline{CS}$ ) input, allowing any number of devices to share the same bus.

The X25C02 also features two additional inputs that provide the end user with added flexibility. By asserting the HOLD input, the X25C02 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The WP input can be used as a hardwire input to the X25C02 disabling all write attempts; thus providing a mechanism for limiting end user capability of altering the memory.

The X25C02 utilizes Xicor's proprietary Direct Write<sup>TM</sup> cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

2

### FUNCTIONAL DIAGRAM



3843 FHD F01



## X25C02

### PIN DESCRIPTIONS

#### Serial Output (SO)

SO is a push-pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

#### Serial Input (SI)

SI is the serial data input pin. All data, opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

#### Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are sampled or latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

#### Chip Select ( $\overline{CS}$ )

When  $\overline{CS}$  is high, the X25C02 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway the X25C02 will be in the

standby power mode.  $\overline{CS}$  low enables the X25C02, placing it in the active power mode. It should be noted that after power-on, a high to low transition on  $\overline{CS}$  is required prior to the start of any operation.

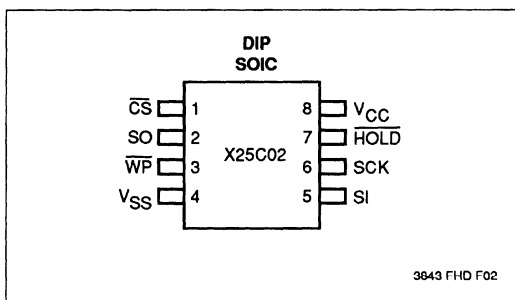
#### Write Protect ( $\overline{WP}$ )

When  $\overline{WP}$  is low, nonvolatile writes to the X25C02 are disabled, but the part otherwise functions normally. When  $\overline{WP}$  is held high, all functions, including nonvolatile writes operate normally.  $\overline{WP}$  going low while  $\overline{CS}$  is still low will interrupt a write to the X25C02. If the internal write cycle has already been initiated,  $\overline{WP}$  going low will have no effect on write.

#### Hold ( $\overline{HOLD}$ )

$\overline{HOLD}$  is used in conjunction with the  $\overline{CS}$  pin to select the device. Once the part is selected and a serial sequence is underway,  $\overline{HOLD}$  may be used to pause the serial communication with the controller without resetting the serial sequence. To pause,  $\overline{HOLD}$  must be brought low while SCK is Low. To resume communication,  $\overline{HOLD}$  is brought high, again while SCK is low. If the pause feature is not used,  $\overline{HOLD}$  should be held high at all times.

### PIN CONFIGURATION



### PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
VSS	Ground
VCC	Supply Voltage
$\overline{HOLD}$	Hold Input

3843 PGM T01

# X25C02

## PRINCIPLES OF OPERATION

The X25C02 is a 256 x 8 E<sup>2</sup>PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of the popular 6805 and 68HC11 microcontroller families.

The X25C02 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. CS must be low and the HOLD and WP inputs must be high during the entire operation.

Table 1 contains a list of the instructions and their operation codes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after CS goes low. SCK is static, allowing the user to stop the

clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the HOLD input to place the X25C02 into a "PAUSE" condition. After releasing HOLD, the X25C02 will resume operation from the point when HOLD was first asserted.

### Write Enable (WREN) and Write Disable (WRDI)

The X25C02 contains a write enable latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-on condition and after the completion of a byte or page write cycle. The latch is also reset if WP is brought low.

2

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 4 Bytes)

3843 PGM T02

\*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

## X25C02

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### DEVICE OPERATION

#### Clock and Data Timing

Data input on the SI line is sampled and latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

#### Read Sequence

The  $\overline{CS}$  line is first pulled low to select the device. The 8 bit read opcode is transmitted to the X25C02, followed by the 8 bit byte address. After the read opcode and byte address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (\$FF) the address counter rolls over to address \$00 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking  $\overline{CS}$  high. Refer to the read operation sequence illustrated in Figure 1.

#### Write Sequence

Prior to any attempt to write data into the X25C02, the write enable latch must first be set by issuing the WREN instruction. (See Fig. 2)  $\overline{CS}$  is first taken low, then the instruction is clocked into the X25C02. After all eight bits of the instruction are transmitted,  $\overline{CS}$  must then be taken high. If the user continues the write operation without taking  $\overline{CS}$  high after issuing the WREN instruction the write operation will be ignored.

Once the write enable latch is set, the user may proceed by issuing the write instruction, followed by the address and then the data to be written. This is minimally a twenty-four clock operation.  $\overline{CS}$  must go low and remain low for the duration of the operation. The host may continue to write up to four bytes of data to the X25C02. The only restriction is the four bytes must reside on the same page. A page address begins with address XXXX XX00 and ends with XXXX XX11. If the byte address counter reaches XXXX XX11 and the clock continues the counter will roll back to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed,  $\overline{CS}$  can only be brought high after the twenty-fourth, thirty-second, fortieth or fortyeighth clock. If it is brought high at any other time the write operation will not be completed. Refer to Figure 4 below for a detailed illustration of the page write sequence and time frames in which  $\overline{CS}$  going high are valid.

#### Hold Operation

The  $\overline{HOLD}$  input should be high (at VIH) under normal operation. If a data transfer is to be interrupted  $\overline{HOLD}$  can be pulled low to suspend the transfer until it can be resumed. The only restriction is the SCK input must be low when  $\overline{HOLD}$  is first pulled low and SCK must also be low when  $\overline{HOLD}$  is released.

The  $\overline{HOLD}$  input may be tied high either directly to VCC or tied to VCC through a resistor.

# X25C02

## Operational Notes

The X25C02 powers-on in the following state:

- The device is in the low power standby state.
- A high to low transition on  $\overline{CS}$  is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The write enable latch is reset.

## Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The write enable latch is reset upon power-up.
- A write enable instruction must be issued to set the write enable latch.
- $\overline{CS}$  must come high at the proper clock count in order to start a write cycle.

The write enable latch is reset when  $\overline{WP}$  is brought low.

2

Figure 1. Read Operation Sequence

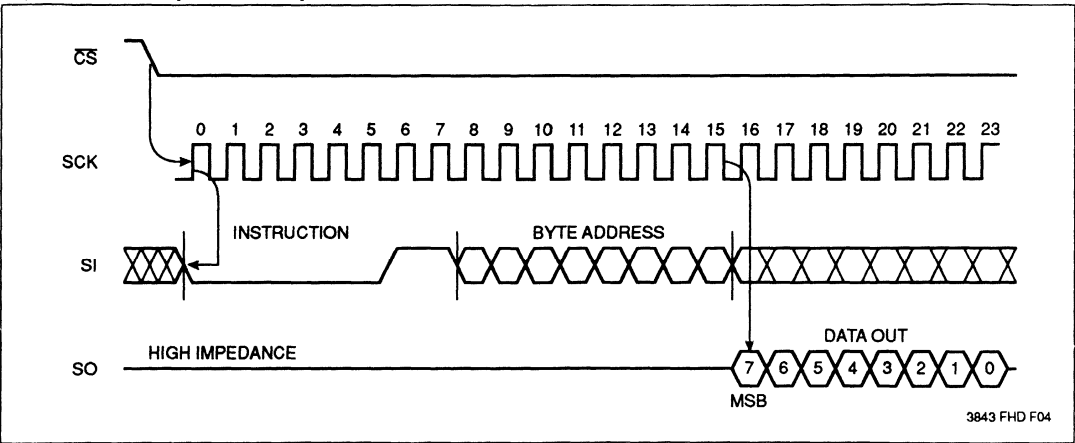
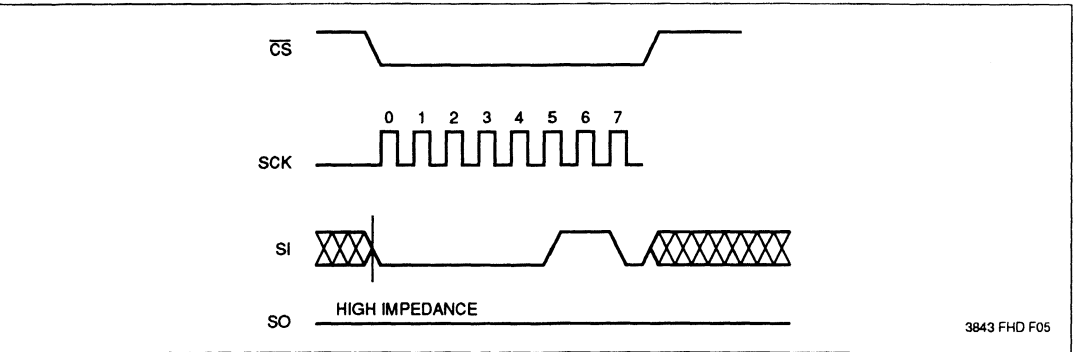
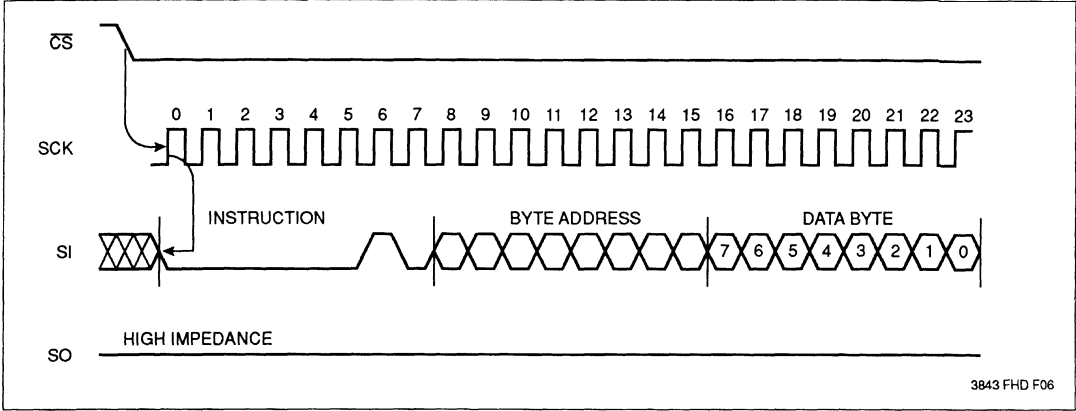


Figure 2. Write Enable Latch

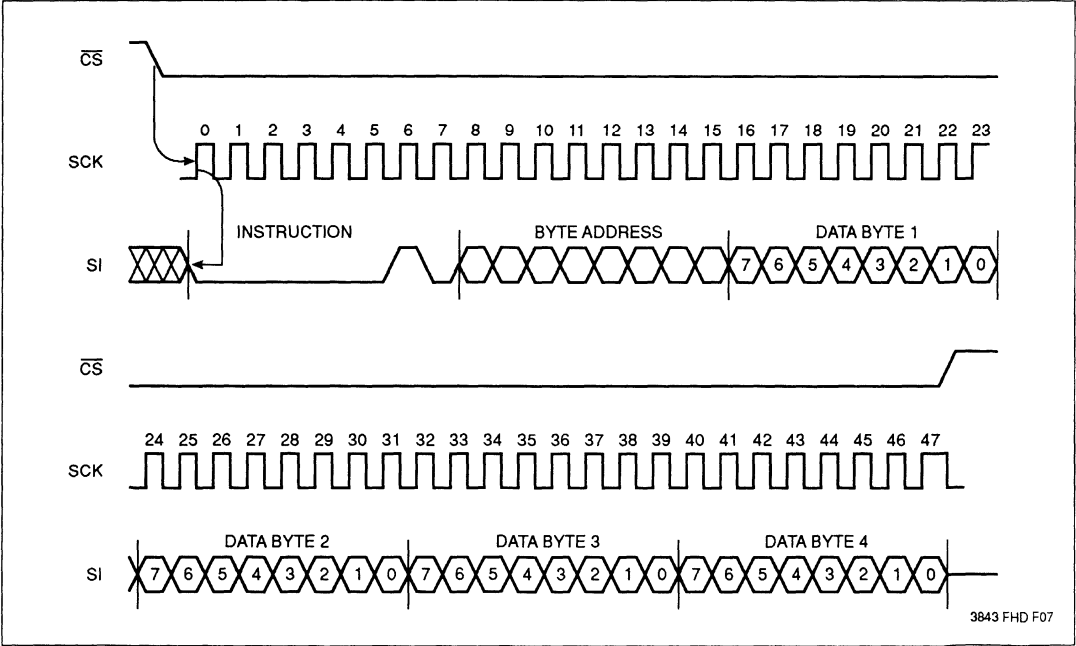


**X25C02**

**Figure 3. Write Operation Sequence**



**Figure 4. Page Write Operation Sequence**



X25C02

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	–65°C to +135°C
Storage Temperature .....	–65°C to +150°C
Voltage on any Pin with Respect to Ground	–1.0V to +7V
D.C. Output Current .....	5mA
Lead Temperature	
(Soldering, 10 Seconds) .....	300°C

\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3843 PGM T03

Supply Voltage	Limits
X25C02	5V ± 10%
X25C02-3	3V to 5.5V

3843 PGM T04

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Supply Current (Active)		2	mA	SCK = V <sub>CC</sub> × 0.1/V <sub>CC</sub> × 0.9 @ 1MHz, SO = OPEN
I <sub>SB</sub>	V <sub>CC</sub> Supply Current (Standby)		150	µA	$\overline{CS}$ = V <sub>CC</sub> , V <sub>IN</sub> = Gnd or V <sub>CC</sub> – 0.3V
I <sub>LI</sub>	Input Leakage Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> <sup>(1)</sup>	Input Low Voltage	–1.0	V <sub>CC</sub> × 0.3	V	
V <sub>IH</sub> <sup>(1)</sup>	Input High Voltage	V <sub>CC</sub> × 0.7	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2mA
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> –0.8		V	I <sub>OH</sub> = –1.0mA

3843 PGM T05

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t <sub>PUR</sub> <sup>(1)</sup>	Power-up to Read Operation		1	ms
t <sub>PUW</sub> <sup>(1)</sup>	Power-up to Write Operation		5	ms

3843 PGM T09

CAPACITANCE T<sub>A</sub> = 25°C, f = 1.0MHz, V<sub>CC</sub> = 5V.

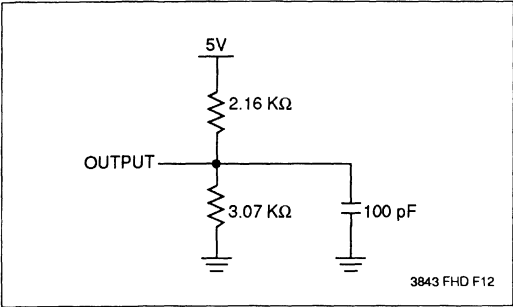
Symbol	Test	Max.	Units	Conditions
C <sub>OUT</sub> <sup>(2)</sup>	Output Capacitance (SO)	8	pF	V <sub>OUT</sub> = 0V
C <sub>IN</sub> <sup>(2)</sup>	Input Capacitance (SCK, SI, CS, WP, HOLD)	6	pF	V <sub>IN</sub> = 0V

3843 PGM T06

Notes: (1) V<sub>IL</sub> Min and V<sub>IH</sub> Max. are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.

X25C02

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
Input and Output Timing Level	$V_{CC} \times 0.5$

3843 PGM T07

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
$f_{SCK}$	Clock Frequency	0	1	MHz
$t_{CYC}$	Cycle Time	1000		ns
$t_{LEAD}$	$\overline{CS}$ Lead Time	500		ns
$t_{LAG}$	$\overline{CS}$ Lag Time	500		ns
$t_{WH}$	Clock High Time	400		ns
$t_{WL}$	Clock Low Time	400		ns
$t_{SU}$	Data Setup Time	100		ns
$t_H$	Data Hold Time	100		ns
$t_{RI}$	Data In Rise Time		2.0	μs
$t_{FI}$	Data In Fall Time		2.0	μs
$t_{HD}$	HOLD Setup Time	200		ns
$t_{CD}$	HOLD Hold Time	200		ns
$t_{CS}$	$\overline{CS}$ Deselect Time	500		ns
$t_{WC}^{(3)}$	Write Cycle Time		10	ms

3843 PGM T08

Data Output Timing

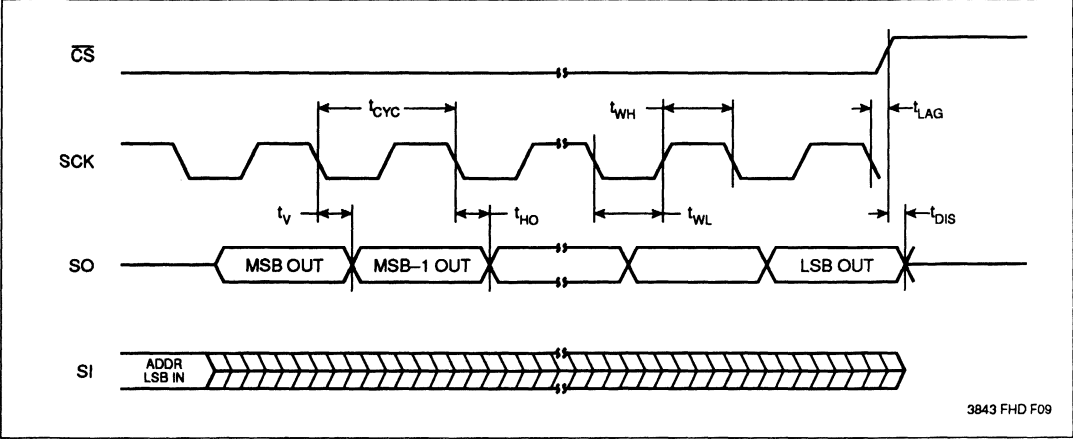
Symbol	Parameter	Min.	Max.	Units
$f_{SCK}$	Clock Frequency	0	1	MHz
$t_{DIS}$	Output Disable Time		500	ns
$t_V$	Output Valid from clock Low		400	ns
$t_{HO}$	Output Hold Time	0		ns
$t_{RO}^{(1)}$	Output Rise Time		300	ns
$t_{FO}^{(1)}$	Output Fall Time		300	ns
$t_{LZ}$	HOLD High to Output in Low Z	100		ns
$t_{HZ}$	HOLD Low to Output in High Z	100		ns

3843 PGM T09

Notes: (3)  $t_{WC}$  is the time from the rising edge of  $\overline{CS}$  after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

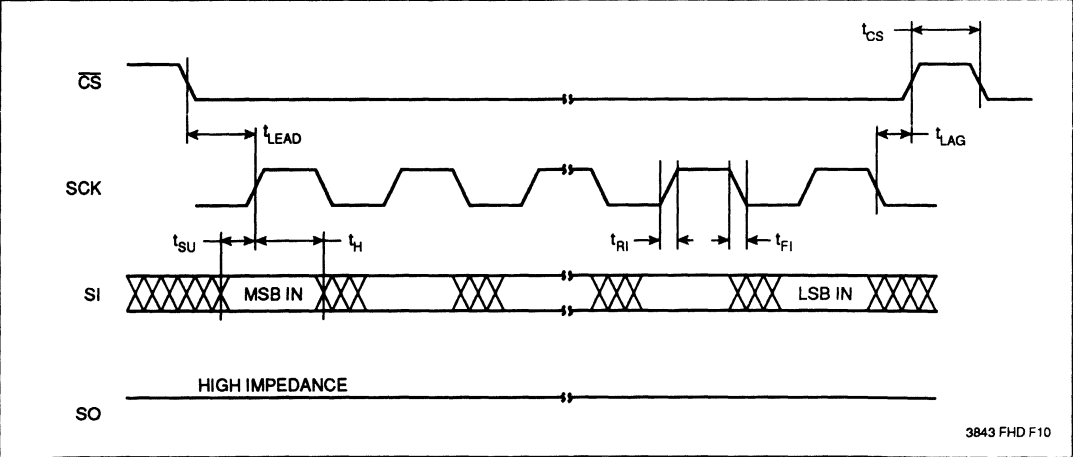
# X25C02

## Serial Output Timing



2

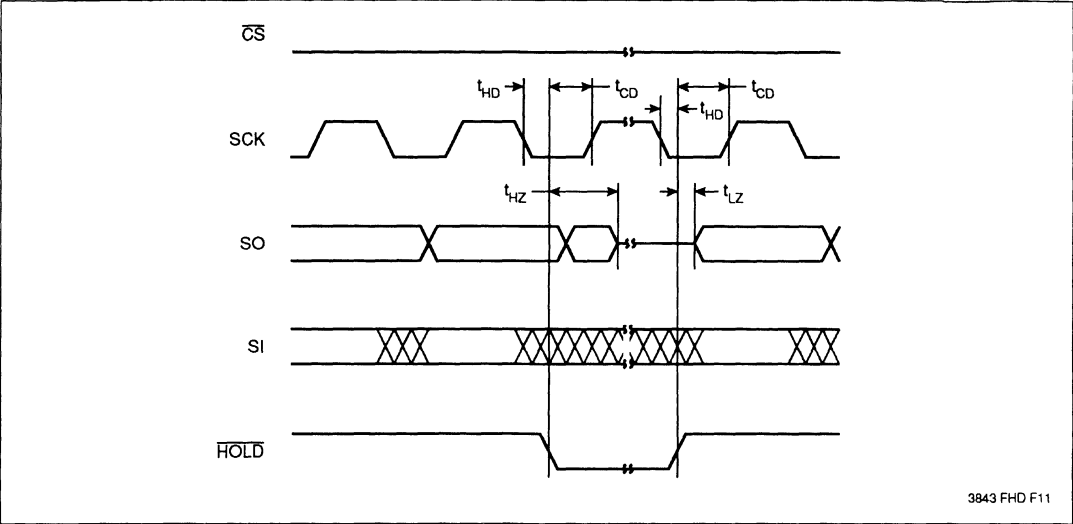
## Serial Input Timing





X25C02

Hold Timing



SPI Serial E<sup>2</sup>PROM

## FEATURES

- 1MHz Clock Rate
- 128 X 8 Bits
  - 4 Byte Page Mode
- Low Power CMOS
  - 150 $\mu$ A Standby Current
  - 3mA Active Write Current
- 3V To 5.5V Power Supply
- Block Write Protection
  - Protect 1/4, 1/2 or all of E<sup>2</sup>PROM Array
- Built-in Inadvertent Write Protection
  - Power-Up/Power-Down Protection Circuitry
  - Write Latch
  - Write Protect Pin
- Self-Timed Write Cycle
  - 5mS Write Cycle Time (Typical)
- High Reliability
  - Endurance: 100,000 Cycles per byte
  - Data Retention: 100 Years
  - ESD Protection: 2000V on all Pins
- 8-Pin Mini-DIP Package
- 8-Pin SOIC Package

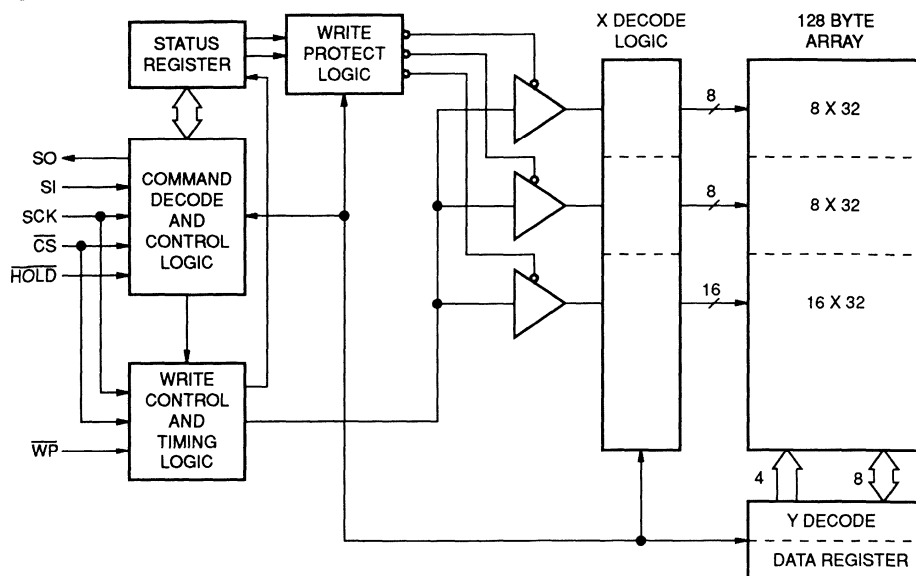
## DESCRIPTION

The X25010 is a CMOS 1024 bit serial E<sup>2</sup>PROM, internally organized as 128 x 8. The X25010 features a serial interface and software protocol allowing operation on a simple three wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ( $\overline{CS}$ ) input, allowing any number of devices to share the same bus.

The X25010 also features two additional inputs that provide the end user with added flexibility. By asserting the  $\overline{HOLD}$  input, the X25010 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The WP input can be used as a hardware input to the X25010 disabling all write attempts; thus providing a mechanism for limiting end user capability of altering the memory.

The X25010 utilizes Xicor's proprietary Direct Write<sup>TM</sup> cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

## FUNCTIONAL DIAGRAM



3835 FHD F01

## X25010

### PIN DESCRIPTIONS

#### Serial Output (SO)

SO is a push-pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

#### Serial Input (SI)

SI is the serial data input pin. All data, opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

#### Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are sampled or latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

#### Chip Select ( $\overline{CS}$ )

When  $\overline{CS}$  is high, the X25010 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway the X25010 will be in the standby power mode.  $\overline{CS}$  low enables the X25010, placing it in the active power mode. It should be noted that after power-on, a high to low transition on  $\overline{CS}$  is required prior to the start of any operation.

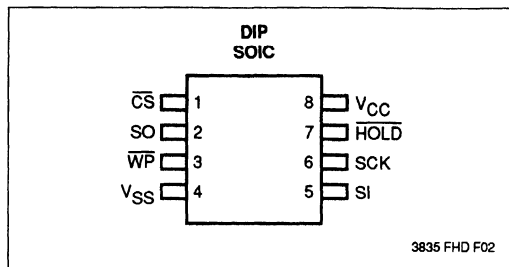
#### Write Protect ( $\overline{WP}$ )

When  $\overline{WP}$  is low, nonvolatile writes to the X25010 are disabled, but the part otherwise functions normally. When  $\overline{WP}$  is held high, all functions, including nonvolatile writes operate normally.  $\overline{WP}$  going low while  $\overline{CS}$  is still low will interrupt a write to the X25010. If the internal write cycle has already been initiated,  $\overline{WP}$  going low will have no affect on write.

#### Hold ( $\overline{HOLD}$ )

$\overline{HOLD}$  is used in conjunction with the  $\overline{CS}$  pin to select the device. Once the part is selected and a serial sequence is underway,  $\overline{HOLD}$  may be used to pause the serial communication with the controller without resetting the serial sequence. To pause,  $\overline{HOLD}$  must be brought low while SCK is Low. To resume communication,  $\overline{HOLD}$  is brought high, again while SCK is low. If the pause feature is not used,  $\overline{HOLD}$  should be held high at all times.

### PIN CONFIGURATION



### PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
$V_{SS}$	Ground
$V_{CC}$	Supply Voltage
$\overline{HOLD}$	Hold Input

3835 PGM T01

# X25010

## PRINCIPLES OF OPERATION

The X25010 is a 128 x 8 E<sup>2</sup>PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of the popular 6805 and 68HC11 microcontroller families.

The X25010 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK.  $\overline{CS}$  must be low and the  $\overline{HOLD}$  and  $\overline{WP}$  inputs must be high during the entire operation.

Table 1 contains a list of the instructions and their operation codes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after  $\overline{CS}$  goes low. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the  $\overline{HOLD}$  input to place the X25010 into a "PAUSE" condition. After releasing  $\overline{HOLD}$ , the X25010 will resume operation from the point when  $\overline{HOLD}$  was first asserted.

### Write Enable (WREN) and Write Disable (WRDI)

The X25010 contains a write enable latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-on condition and after the completion of a byte or page write cycle. The latch is also reset if  $\overline{WP}$  is brought low.

## Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP

The **Write-In-Process (WIP)** bit indicates whether the X25010 is busy with a write operation. When set to a "1" a write is in progress, when set to a "0" no write is in progress. During a write all other bits are set to "1".

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a "1" the latch is set, when set to a "0" the latch is reset.

The **Block Protect (BP0 and BP1)** bits indicate the extent of protection employed. These bits are set by the user issuing the WRSR instruction.

## Write Status Register (WRSR)

The write status register instruction allows the user to select one of four levels of protection. The X25010 is divided into four 128-bit segments. One, two or all four of the segments may be protected. That is, the user may read the segment but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	NONE
0	1	\$60-\$7F (1/4)
1	0	\$40-\$7F (1/2)
1	1	\$00-\$7F (All)

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register (Block Protect Bits)
READ	0000 0011	Read Data from Memory Array beginning at Selected Address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 4 Bytes)

\*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

## X25010

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### DEVICE OPERATION

#### Clock and Data Timing

Data input on the SI line is sampled and latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

#### Read Sequence

The  $\overline{CS}$  line is first pulled low to select the device. The 8 bit read opcode is transmitted to the X25010, followed by the 8 bit byte address. After the read opcode and byte address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (\$7F) the address counter rolls over to address \$00 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking  $\overline{CS}$  high. Refer to the read operation sequence illustrated in Figure 1.

#### Write Sequence

Prior to any attempt to write data into the X25010 the write enable latch must first be set by issuing the WREN instruction. (See Fig. 2)  $\overline{CS}$  is first taken low, then the instruction is clocked into the X25010. After all eight bits of the instruction are transmitted,  $\overline{CS}$  must then be taken high. If the user continues the write operation without taking  $\overline{CS}$  high after issuing the WREN instruction the write operation will be ignored.

Once the write enable latch is set, the user may proceed by issuing the write instruction, followed by the address and then the data to be written. This is minimally a twenty-four clock operation.  $\overline{CS}$  must go low and remain low for the duration of the operation. The host may continue to write up to four bytes of data to the X25010. The only restriction is the four bytes must reside on the same page. A page address begins with address XXXX XX00 and ends with XXXX XX11. If the byte address counter reaches XXXX XX11 and the clock continues the counter will roll back to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed,  $\overline{CS}$  can only be brought high after the twenty-fourth, thirty-second, fortieth or fortyeighth clock. If it is brought high at any other time the write operation will not be completed. Refer to Figure 4 below for a detailed illustration of the page write sequence and time frames in which  $\overline{CS}$  going high are valid.

While the write is in progress the stats register may be read to check the WIP bit. During this time the WIP bit will be high and all other bits in the status register will be high.

#### Hold Operation

The  $\overline{HOLD}$  input should be high (at  $V_{IH}$ ) under normal operation. If a data transfer is to be interrupted  $\overline{HOLD}$  can be pulled low to suspend the transfer until it can be resumed. The only restriction is the SCK input must be low when  $\overline{HOLD}$  is first pulled low and SCK must also be low when  $\overline{HOLD}$  is released.

The  $\overline{HOLD}$  input may be tied high either directly to  $V_{CC}$  or tied to  $V_{CC}$  through a resistor.

# X25010

## Operational Notes

The X25010 powers-on in the following state:

- The device is in the low power standby state.
- A high to low transition on  $\overline{CS}$  is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The write enable latch is reset.

## Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The write enable latch is reset upon power-up.
- A write enable instruction must be issued to set the write enable latch.
- $\overline{CS}$  must come high at the proper clock count in order to start a write cycle.

The write enable latch is reset when  $\overline{WP}$  is brought low.

2

Figure 1. Read Operation Sequence

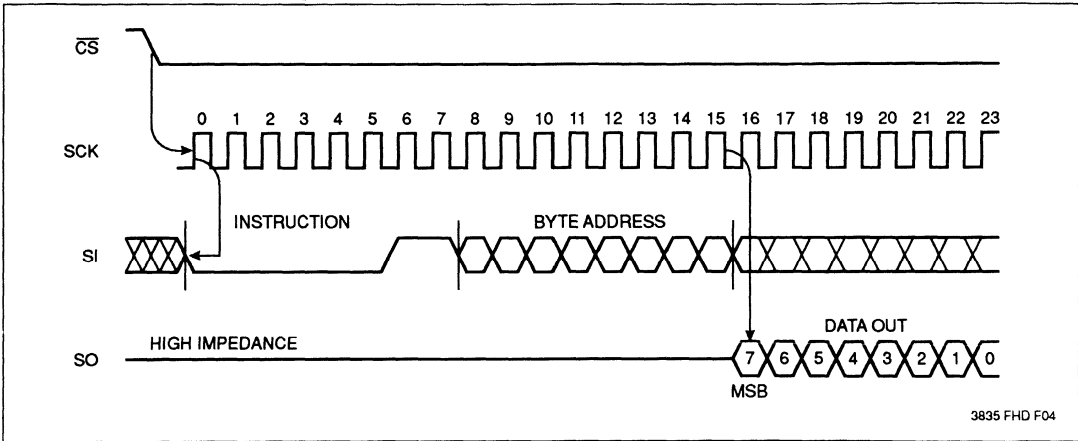
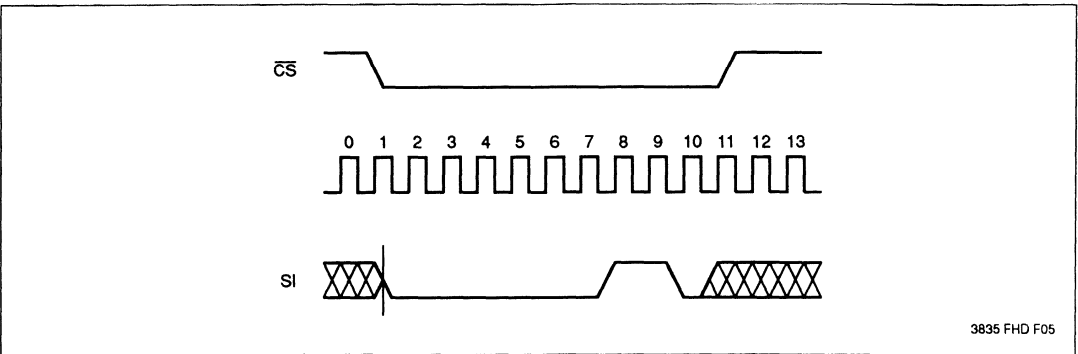
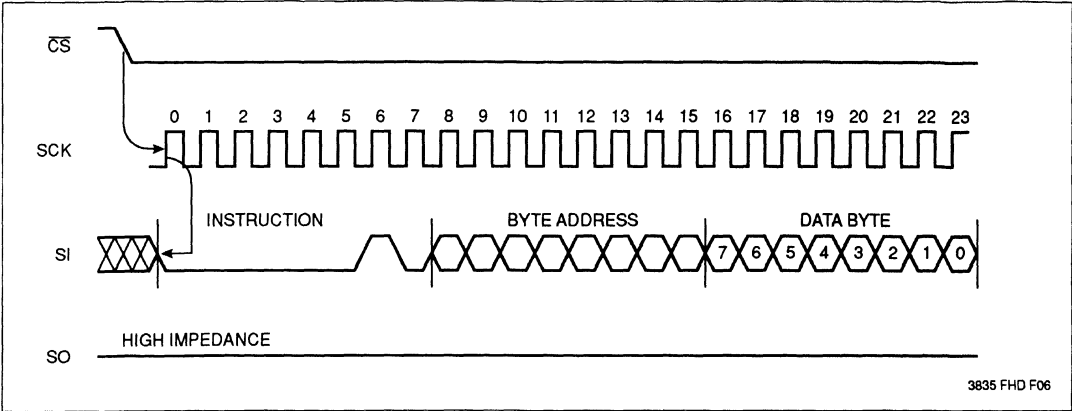


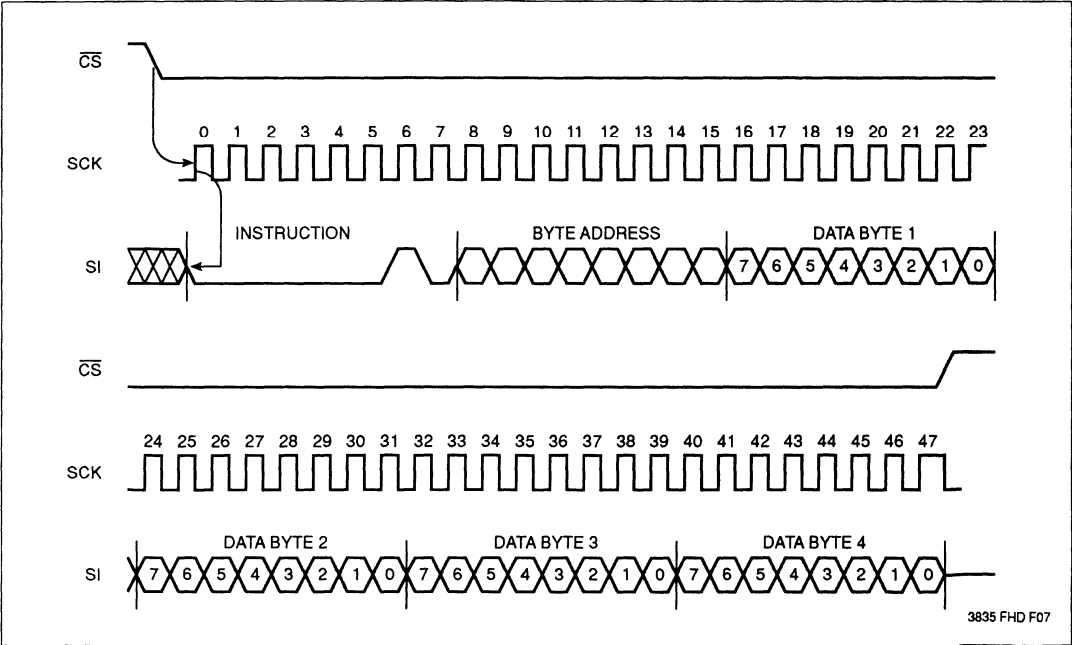
Figure 2. Write Enable Latch



**Figure 3. Write Operation Sequence**



**Figure 4. Page Write Operation Sequence**



X25010

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	–65°C to +135°C
Storage Temperature .....	–65°C to +150°C
Voltage on any Pin with Respect to Ground	–1.0V to +7V
D.C. Output Current .....	5mA
Lead Temperature	
(Soldering, 10 Seconds) .....	300°C

\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3835 PGM T03

Supply Voltage	Limits
X25010	5V ± 10%
X25010-3	3V to 5.5V

3835 PGM T04

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D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Supply Current (Active)		3	mA	SCK = V <sub>CC</sub> × 0.1/V <sub>CC</sub> × 0.9 @ 1MHz, SO = OPEN
I <sub>SB</sub>	V <sub>CC</sub> Supply Current (Standby)		150	μA	CS = V <sub>CC</sub> , V <sub>IN</sub> = Gnd or V <sub>CC</sub> – 0.3V
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> <sup>(1)</sup>	Input Low Voltage	–1.0	V <sub>CC</sub> × 0.3	V	
V <sub>IH</sub> <sup>(1)</sup>	Input High Voltage	V <sub>CC</sub> × 0.7	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2mA
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> –0.8		V	I <sub>OH</sub> = –1.0mA

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POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t <sub>PUR</sub> <sup>(2)</sup>	Power-up to Read Operation		1	ms
t <sub>PUW</sub> <sup>(2)</sup>	Power-up to Write Operation		5	ms

3835 PGM T09

CAPACITANCE T<sub>A</sub> = 25°C, f = 1.0MHz, V<sub>CC</sub> = 5V.

Symbol	Test	Max.	Units	Conditions
C <sub>OUT</sub> <sup>(2)</sup>	Output Capacitance (SO)	8	pF	V <sub>OUT</sub> = 0V
C <sub>IN</sub> <sup>(2)</sup>	Input Capacitance (SCK, SI, CS, WP, HOLD)	6	pF	V <sub>IN</sub> = 0V

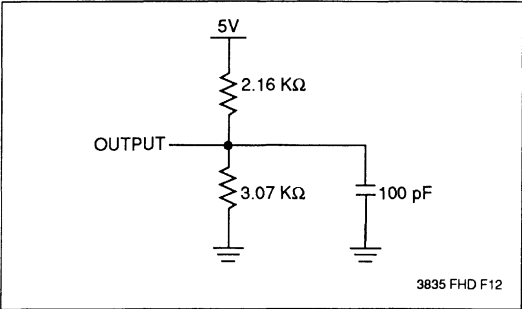
Notes: (1) V<sub>IL</sub> Min and V<sub>IH</sub> Max. are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.

3835 PGM T06



X25010

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
Input and Output Timing Level	$V_{CC} \times 0.5$

3835 PGM T07

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
fSCK	Clock Frequency	0	1	MHz
tCYC	Cycle Time	1000		ns
tLEAD	CS Lead Time	500		ns
tLAG	CS Lag Time	500		ns
tWH	Clock High Time	400		ns
tWL	Clock Low Time	400		ns
tSU	Data Setup Time	100		ns
tH	Data Hold Time	100		ns
tRI	Data In Rise Time		2.0	μs
tFI	Data In Fall Time		2.0	μs
tHD	HOLD Setup Time	200		ns
tCD	HOLD Hold Time	200		ns
tCS	CS Deselect Time	500		ns
tWC <sup>(3)</sup>	Write Cycle Time		10	ms

3835 PGM T08

Data Output Timing

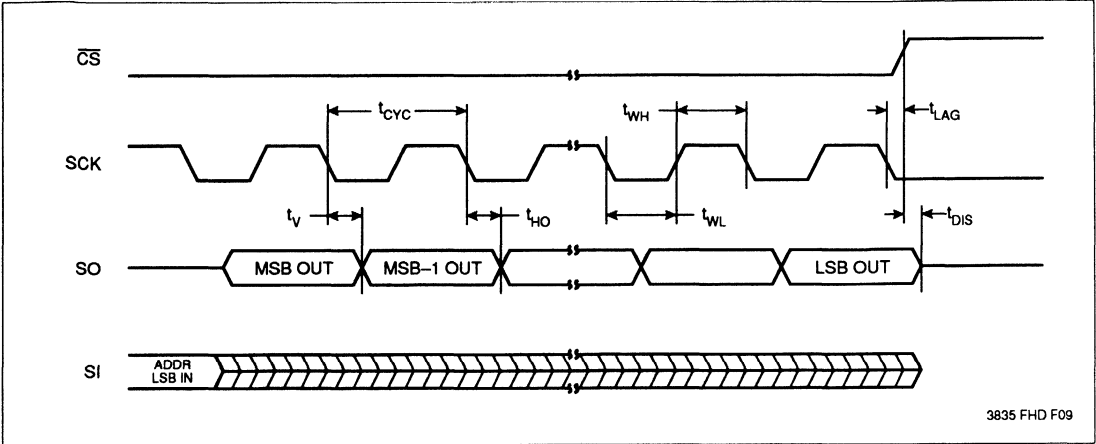
Symbol	Parameter	Min.	Max.	Units
fSCK	Clock Frequency	0	1	MHz
tDIS	Output Disable Time		500	ns
tV	Output Valid from clock Low		360	ns
tHO	Output Hold Time	0		ns
tRO <sup>(1)</sup>	Output Rise Time		300	ns
tFO <sup>(1)</sup>	Output Fall Time		300	ns
tLZ	HOLD High to Output in Low Z	100		ns
tHZ	HOLD Low to Output in High Z	100		ns

3835 PGM T09

Notes: (3) t<sub>WC</sub> is the time from the rising edge of  $\overline{CS}$  after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

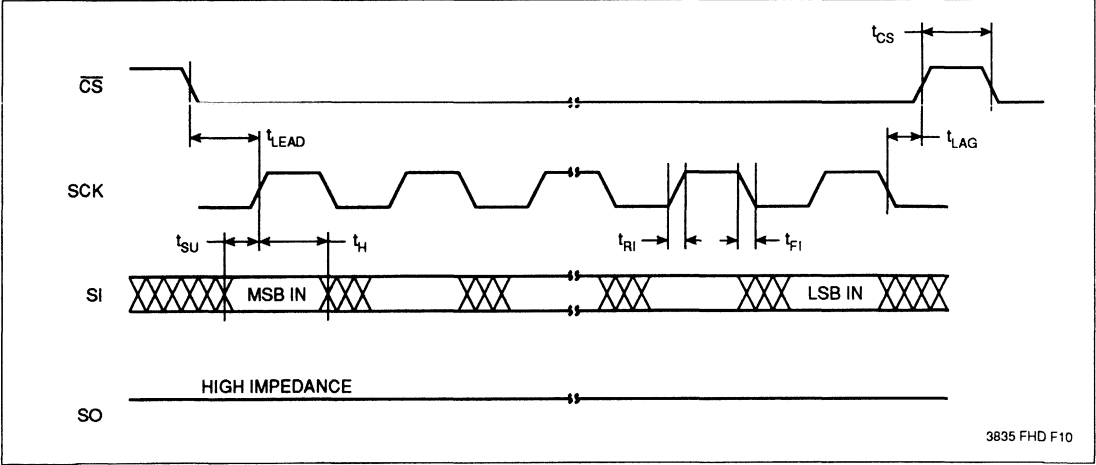
X25010

Serial Output Timing



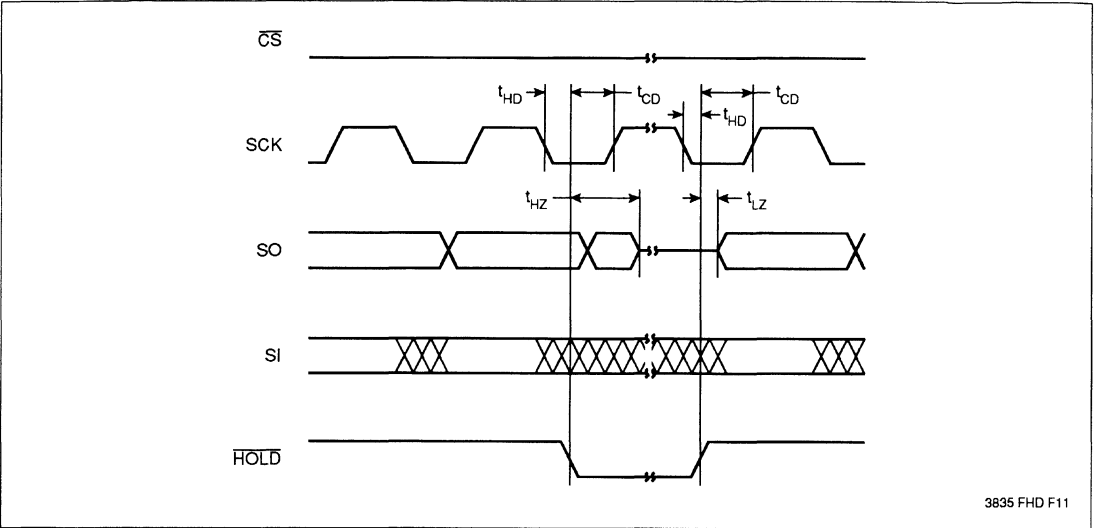
2

Serial Input Timing



X25010

Hold Timing





2K

X25020

256 x 8 Bit

SPI Serial E<sup>2</sup>PROM

## FEATURES

- 1MHz Clock Rate
- 256 X 8 Bits
  - 4 Byte Page Mode
- Low Power CMOS
  - 150 $\mu$ A Standby Current
  - 2mA Active Write Current
- 3V To 5.5V Power Supply
- Block Write Protection
  - Protect 1/4, 1/2 or all of E<sup>2</sup>PROM Array
- Built-In Inadvertent Write Protection
  - Power-Up/Power-Down protection circuitry
  - Write Latch
  - Write Protect Pin
- Self-Timed Write Cycle
  - 5mS Write Cycle Time (Typical)
- High Reliability
  - Endurance: 100,000 cycles per byte
  - Data Retention: 100 Years
  - ESD protection: 2000V on all pins
- 8-Pin Mini-DIP Package
- 8-Pin SOIC Package

## DESCRIPTION

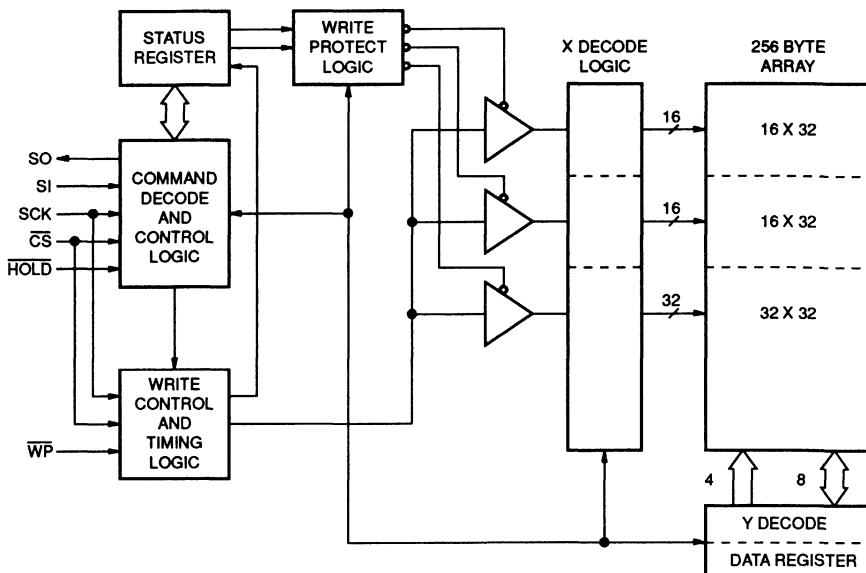
The X25020 is a CMOS 2048 bit serial E<sup>2</sup>PROM, internally organized as 256 x 8. The X25020 features a serial interface and software protocol allowing operation on a simple three wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ( $\overline{CS}$ ) input, allowing any number of devices to share the same bus.

The X25020 also features two additional inputs that provide the end user with added flexibility. By asserting the  $\overline{HOLD}$  input, the X25020 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The  $\overline{WP}$  input can be used as a hardware input to the X25020 disabling all write attempts; thus providing a mechanism for limiting end user capability of altering the memory.

The X25020 utilizes Xicor's proprietary Direct Write<sup>TM</sup> cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

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## FUNCTIONAL DIAGRAM



3834 FHD F01

Direct Write<sup>TM</sup> is a trademark of Xicor, Inc.

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# X25020

## PIN DESCRIPTIONS

### Serial Output (SO)

SO is a push-pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

### Serial Input (SI)

SI is the serial data input pin. All data, opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

### Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are sampled or latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

### Chip Select ( $\overline{\text{CS}}$ )

When  $\overline{\text{CS}}$  is high, the X25020 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway the X25020 will be in the standby power mode.  $\overline{\text{CS}}$  low enables the X25020, placing it in the active power mode. It should be noted that after power-on, a high to low transition on  $\overline{\text{CS}}$  is required prior to the start of any operation.

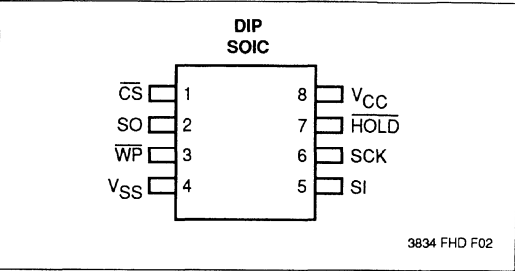
### Write Protect ( $\overline{\text{WP}}$ )

When  $\overline{\text{WP}}$  is low, nonvolatile writes to the X25020 are disabled, but the part otherwise functions normally. When  $\overline{\text{WP}}$  is held high, all functions, including nonvolatile writes operate normally.  $\overline{\text{WP}}$  going low while  $\overline{\text{CS}}$  is still low will interrupt a write to the X25020. If the internal write cycle has already been initiated,  $\overline{\text{WP}}$  going low will have no affect on write.

### Hold ( $\overline{\text{HOLD}}$ )

$\overline{\text{HOLD}}$  is used in conjunction with the  $\overline{\text{CS}}$  pin to select the device. Once the part is selected and a serial sequence is underway,  $\overline{\text{HOLD}}$  may be used to pause the serial communication with the controller without resetting the serial sequence. To pause,  $\overline{\text{HOLD}}$  must be brought low while SCK is Low. To resume communication,  $\overline{\text{HOLD}}$  is brought high, again while SCK is low. If the pause feature is not used,  $\overline{\text{HOLD}}$  should be held high at all times.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
$\overline{\text{CS}}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{\text{WP}}$	Write Protect Input
Vss	Ground
Vcc	Supply Voltage
$\overline{\text{HOLD}}$	Hold Input

3834 PGM T01

X25020

PRINCIPLES OF OPERATION

The X25020 is a 256 x 8 E<sup>2</sup>PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of the popular 6805 and 68HC11 microcontroller families.

The X25020 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. CS must be low and the HOLD and WP inputs must be high during the entire operation.

Table 1 contains a list of the instructions and their operation codes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after CS goes low. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the HOLD input to place the X25020 into a "PAUSE" condition. After releasing HOLD, the X25020 will resume operation from the point when HOLD was first asserted.

Write Enable (WREN) and Write Disable (WRDI)

The X25020 contains a write enable latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-on condition and after the completion of a byte or page write cycle. The latch is also reset if WP is brought low.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP

The **Write-In-Process (WIP)** bit indicates whether the X25020 is busy with a write operation. When set to a "1" a write is in progress, when set to a "0" no write is in progress. During a write all other bits are set to "1".

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a "1" the latch is set, when set to a "0" the latch is reset.

The **Block Protect (BP0 and BP1)** bits indicate the extent of protection employed. These bits are set by the user issuing the WRSR instruction.

Write Status Register (WRSR)

The write status register instruction allows the user to select one of four levels of protection. The X25020 is divided into four 512-bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	None
0	1	CO-\$FF (1/4)
1	0	\$80-\$FF (1/2)
1	1	\$00-\$FF (all)

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register (Block Protect Bits)
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 4 Bytes)

\*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

## X25020

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### DEVICE OPERATION

#### Clock and Data Timing

Data input on the SI line is sampled and latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

#### Read Sequence

The  $\overline{CS}$  line is first pulled low to select the device. The 8 bit read opcode is transmitted to the X25020, followed by the 8 bit byte address. After the read opcode and byte address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (\$FF) the address counter rolls over to address \$00 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking  $\overline{CS}$  high. Refer to the read operation sequence illustrated in Figure 1.

#### Write Sequence

Prior to any attempt to write data into the X25020 the write enable latch must first be set by issuing the WREN instruction. (See Fig. 2)  $\overline{CS}$  is first taken low, then the instruction is clocked into the X25020. After all eight bits of the instruction are transmitted,  $\overline{CS}$  must then be taken high. If the user continues the write operation without taking  $\overline{CS}$  high after issuing the WREN instruction the write operation will be ignored.

Once the write enable latch is set, the user may proceed by issuing the write instruction, followed by the address and then the data to be written. This is minimally a twenty-four clock operation.  $\overline{CS}$  must go low and remain low for the duration of the operation. The host may continue to write up to four bytes of data to the X25020. The only restriction is the four bytes must reside on the same page. A page address begins with address XXXX XX00 and ends with XXXX XX11. If the byte address counter reaches XXXX XX11 and the clock continues the counter will roll back to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed,  $\overline{CS}$  can only be brought high after the twenty-fourth, thirty-second, fortieth or forty-eighth clock. If it is brought high at any other time the write operation will not be completed. Refer to Figure 4 below for a detailed illustration of the page write sequence and time frames in which  $\overline{CS}$  going high are valid.

While the write is in progress the status register may be read to check the WIP bit. During this time the WIP bit will be high and all other bits in the status register will be high.

#### Hold Operation

The  $\overline{HOLD}$  input should be high (at  $V_{IH}$ ) under normal operation. If a data transfer is to be interrupted  $\overline{HOLD}$  can be pulled low to suspend the transfer until it can be resumed. The only restriction is the SCK input must be low when  $\overline{HOLD}$  is first pulled low and SCK must also be low when  $\overline{HOLD}$  is released.

The  $\overline{HOLD}$  input may be tied high either directly to  $V_{CC}$  or tied to  $V_{CC}$  through a resistor.

# X25020

## Operational Notes

- The X25020 powers-on in the following state:
- The device is in the low power standby state.
  - A high to low transition on  $\overline{CS}$  is required to enter an active state and receive an instruction.
  - SO pin is high impedance.
  - The write enable latch is reset.

## Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The write enable latch is reset upon power-up.
- A write enable instruction must be issued to set the write enable latch.
- $\overline{CS}$  must come high at the proper clock count in order to start a write cycle.

The write enable latch is reset when  $\overline{WP}$  is brought low.

Figure 1. Read Operation Sequence

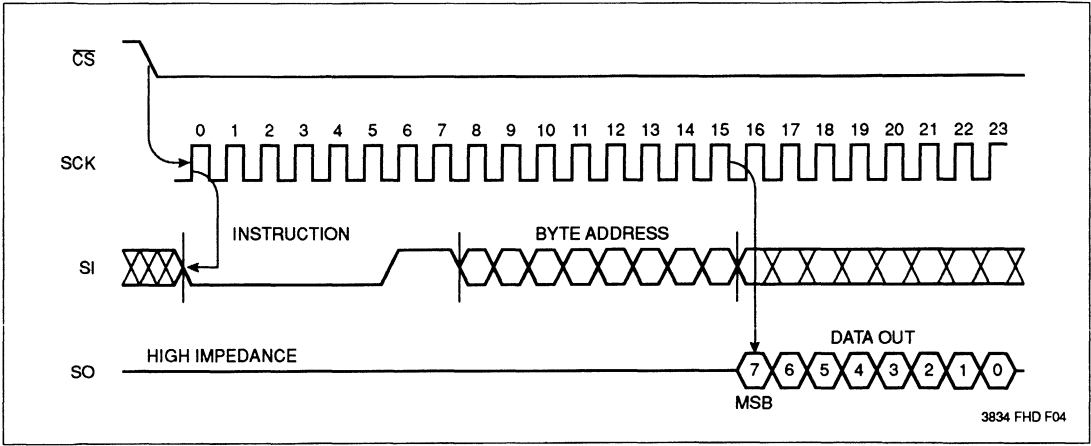


Figure 2. Write Enable Latch

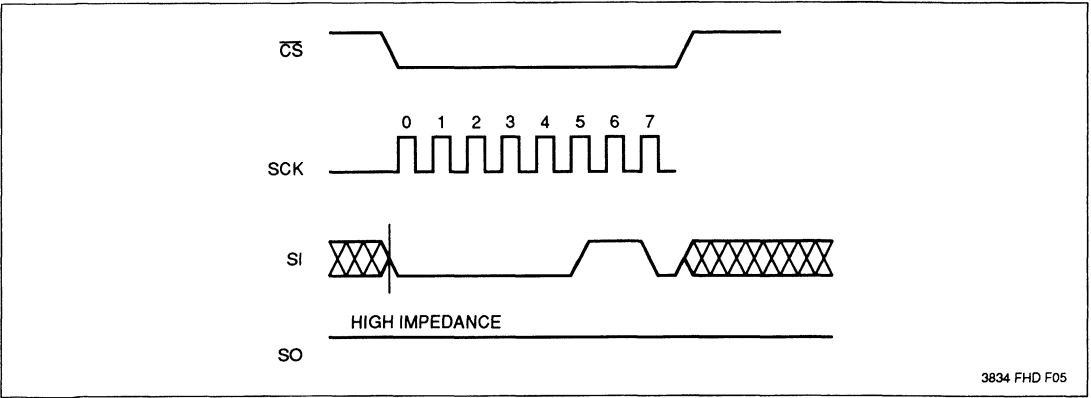




Figure 3. Write Operation Sequence

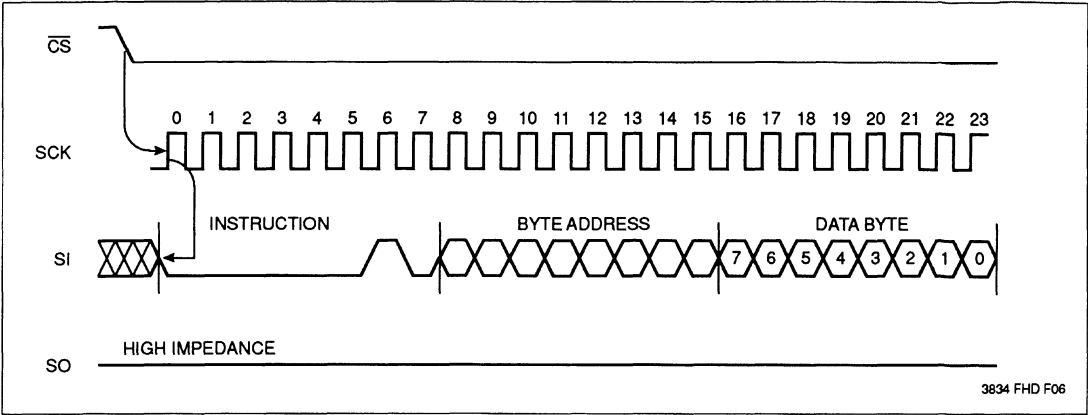
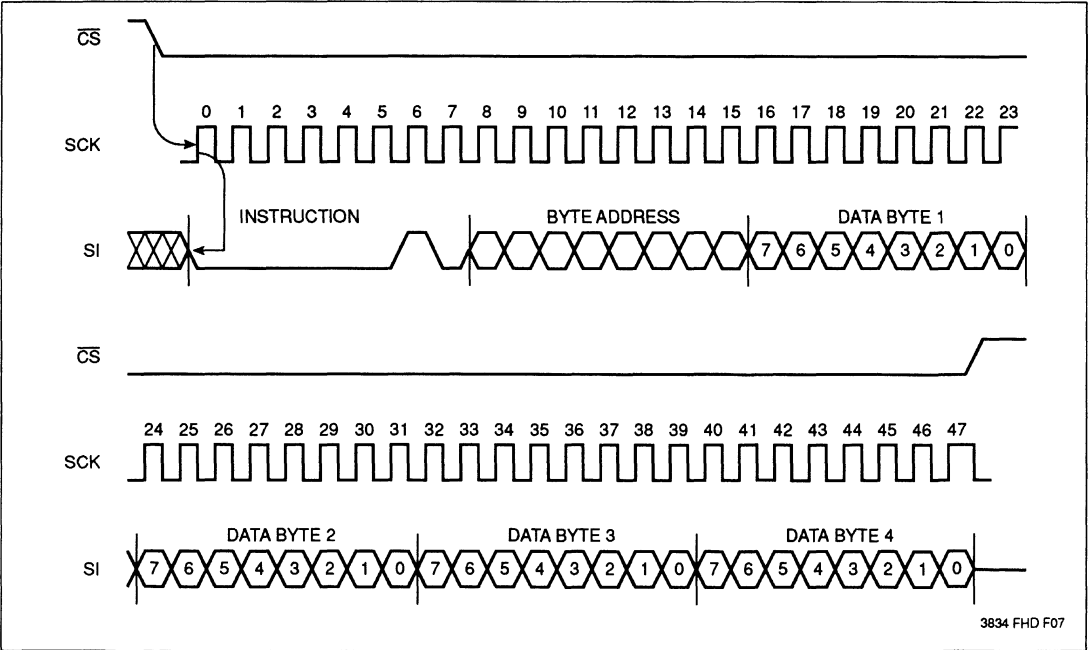


Figure 4. Page Write Operation Sequence



X25020

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	–65°C to +135°C
Storage Temperature .....	–65°C to +150°C
Voltage on any Pin with Respect to Ground	–1.0V to +7V
D.C. Output Current .....	5mA
Lead Temperature	
(Soldering, 10 Seconds) .....	300°C

\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3834 PGM T03

Supply Voltage	Limits
X25020	5V ± 10%
X25020-3	3V to 5.5V

3834 PGM T04

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Supply Current (Active)		3	mA	SCK = V <sub>CC</sub> x 0.1/V <sub>CC</sub> x 0.9 @ 1MHz, SO = OPEN
I <sub>SB</sub>	V <sub>CC</sub> Supply Current (Standby)		150	µA	CS = V <sub>CC</sub> , V <sub>IN</sub> = Gnd or V <sub>CC</sub> – 0.3V
I <sub>LI</sub>	Input Leakage Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> <sup>(1)</sup>	Input Low Voltage	–1.0	V <sub>CC</sub> • 0.3	V	
V <sub>IH</sub> <sup>(1)</sup>	Input High Voltage	V <sub>CC</sub> • 0.7	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2mA
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> –0.8		V	I <sub>OH</sub> = –1.0mA

3834 PGM T05

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t <sub>PUR</sub> <sup>(2)</sup>	Power-up to Read Operation		1	ms
t <sub>PUW</sub> <sup>(2)</sup>	Power-up to Write Operation		5	ms

3834 PGM T09

CAPACITANCE T<sub>A</sub> = 25°C, f = 1.0MHz, V<sub>CC</sub> = 5V.

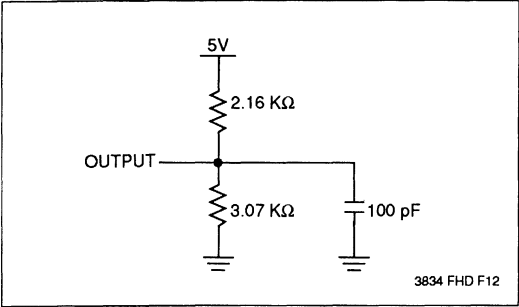
Symbol	Test	Max.	Units	Conditions
C <sub>OUT</sub> <sup>(2)</sup>	Output Capacitance (SO)	8	pF	V <sub>OUT</sub> = 0V
C <sub>IN</sub> <sup>(2)</sup>	Input Capacitance (SCK, SI, CS, WP, HOLD)	6	pF	V <sub>IN</sub> = 0V

3834 PGM T06

Notes: (1) V<sub>IL</sub> Min and V<sub>IH</sub> Max. are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.

# X25020

## EQUIVALENT A.C. LOAD CIRCUIT



## A.C. TEST CONDITIONS

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
Input and Output Timing Level	$V_{CC} \times 0.5$

3834 PGM T07

## A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

### Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f <sub>SCK</sub>	Clock Frequency	0	1	MHz
t <sub>CYC</sub>	Cycle Time	1000		ns
t <sub>LEAD</sub>	$\overline{CS}$ Lead Time	500		ns
t <sub>LAG</sub>	$\overline{CS}$ Lag Time	500		ns
t <sub>WH</sub>	Clock High Time	400		ns
t <sub>WL</sub>	Clock Low Time	400		ns
t <sub>SU</sub>	Data Setup Time	100		ns
t <sub>H</sub>	Data Hold Time	100		ns
t <sub>RI</sub>	Data In Rise Time		2.0	μs
t <sub>FI</sub>	Data In Fall Time		2.0	μs
t <sub>HD</sub>	HOLD Setup Time	200		ns
t <sub>CD</sub>	HOLD Hold Time	200		ns
t <sub>CS</sub>	CS Deselect Time	500		ns
t <sub>WC</sub> <sup>(3)</sup>	Write Cycle Time		10	ms

3834 PGM T08

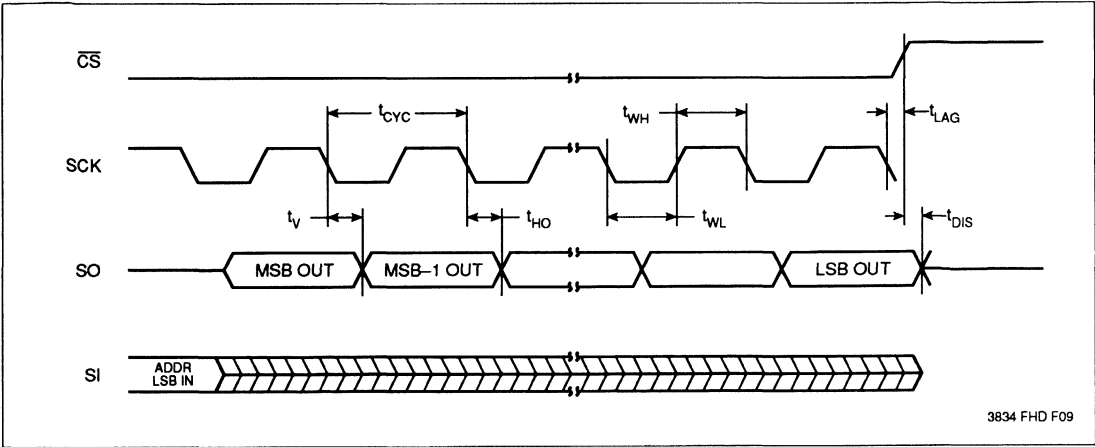
### Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f <sub>SCK</sub>	Clock Frequency	0	1	MHz
t <sub>DIS</sub>	Output Disable Time		500	ns
t <sub>V</sub>	Output Valid from clock Low		360	ns
t <sub>HO</sub>	Output Hold Time	0		ns
t <sub>RO</sub>	Output Rise Time		300	ns
t <sub>FO</sub>	Output Fall Time		300	ns
t <sub>LZ</sub>	HOLD High to Output in Low Z	100		ns
t <sub>HZ</sub>	HOLD Low to Output in High Z	100		ns

3834 PGM T09

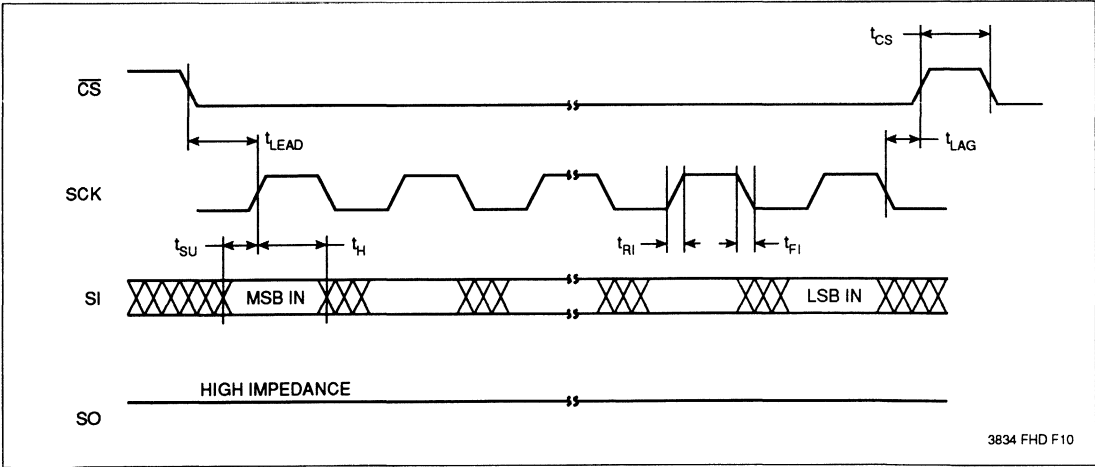
**Notes:** (3) t<sub>WC</sub> is the time from the rising edge of  $\overline{CS}$  after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

Serial Output Timing



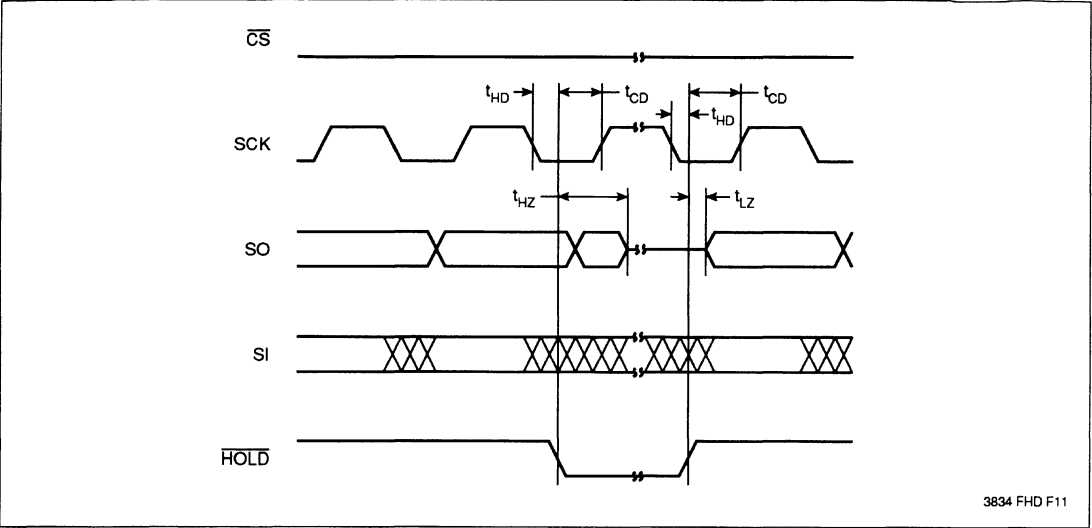
2

Serial Input Timing



# X25020

## Hold Timing





4K

X25040

512 x 8 Bit

SPI Serial E<sup>2</sup>PROM

## FEATURES

- 1MHz Clock Rate
- 512 X 8 Bits
  - 4 Byte Page Mode
- Low Power CMOS
  - 150 $\mu$ A Standby Current
  - 3mA Active Current
- 3V To 5.5V Power Supply
- Block Write Protection
  - Protect 1/4, 1/2 or all of E<sup>2</sup>PROM Array
- Built-In Inadvertent Write Protection
  - Power-Up/Power-Down protection circuitry
  - Write Latch
  - Write Protect Pin
- Self-Timed Write Cycle
  - 5mS Write Cycle Time (Typical)
- High Reliability
  - Endurance: 100,000 cycles per byte
  - Data Retention: 100 Years
  - ESD protection: 2000V on all pins
- 8-Pin Mini-DIP Package
- 8-Pin SOIC Package

## DESCRIPTION

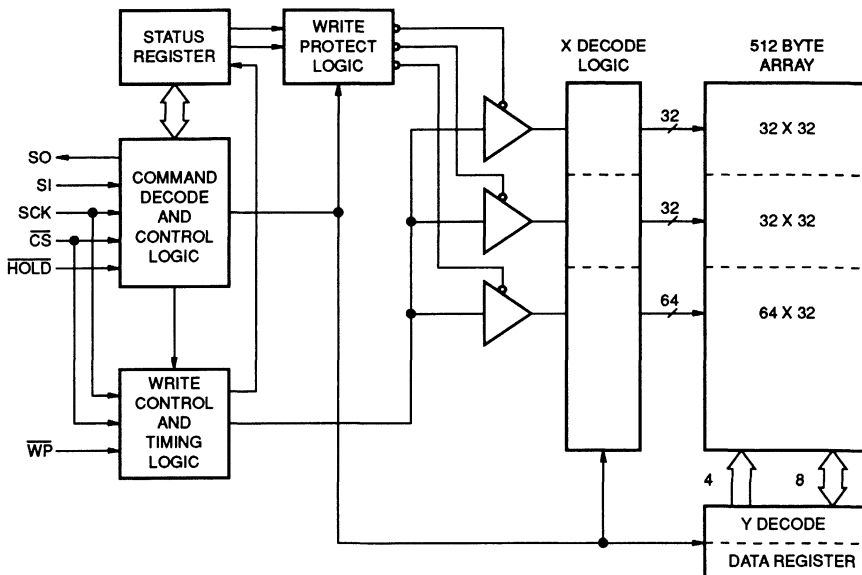
The X25040 is a CMOS 4096 bit serial E<sup>2</sup>PROM, internally organized as 512 x 8. The X25040 features a serial interface and software protocol allowing operation on a simple three wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select (CS) input, allowing any number of devices to share the same bus.

The X25040 also features two additional inputs that provide the end user with added flexibility. By asserting the HOLD input, the X25040 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The WP input can be used as a hardwire input to the X25040 disabling all write attempts; thus providing a mechanism for limiting end user capability of altering the memory.

The X25040 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

2

## FUNCTIONAL DIAGRAM



3844 FHD F01

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## X25040

### PIN DESCRIPTIONS

#### Serial Output (SO)

SO is a push-pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

#### Serial Input (SI)

SI is the serial data input pin. All data, opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

#### Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are sampled or latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

#### Chip Select ( $\overline{CS}$ )

When  $\overline{CS}$  is high, the X25040 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway the X25040 will be in the standby power mode.  $\overline{CS}$  low enables the X25040, placing it in the active power mode. It should be noted that after power-on, a high to low transition on  $\overline{CS}$  is required prior to the start of any operation.

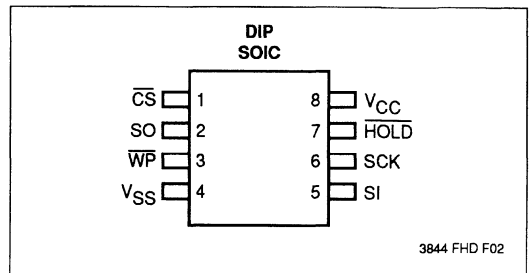
#### Write Protect ( $\overline{WP}$ )

When  $\overline{WP}$  is low, nonvolatile writes to the X25040 are disabled, but the part otherwise functions normally. When  $\overline{WP}$  is held high, all functions, including nonvolatile writes operate normally.  $\overline{WP}$  going low while  $\overline{CS}$  is still low will interrupt a write to the X25040. If the internal write cycle has already been initiated,  $\overline{WP}$  going low will have no effect on write.

#### Hold ( $\overline{HOLD}$ )

$\overline{HOLD}$  is used in conjunction with the  $\overline{CS}$  pin to select the device. Once the part is selected and a serial sequence is underway,  $\overline{HOLD}$  may be used to pause the serial communication with the controller without resetting the serial sequence. To pause,  $\overline{HOLD}$  must be brought low while SCK is Low. To resume communication,  $\overline{HOLD}$  is brought high, again while SCK is low. If the pause feature is not used,  $\overline{HOLD}$  should be held high at all times.

### PIN CONFIGURATION



### PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
$V_{SS}$	Ground
$V_{CC}$	Supply Voltage
$\overline{HOLD}$	Hold Input

3844 PGM T01

X25040

PRINCIPLES OF OPERATION

The X25040 is a 512 x 8 E<sup>2</sup>PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of the popular 6805 and 68HC11 microcontroller families.

The X25040 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. CS must be low and the HOLD and WP inputs must be high during the entire operation.

Table 1 contains a list of the instructions and their operation codes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after CS goes low. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the HOLD input to place the X25040 into a "PAUSE" condition. After releasing HOLD, the X25040 will resume operation from the point when HOLD was first asserted.

Write Enable (WREN) and Write Disable (WRDI)

The X25040 contains a write enable latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-on condition and after the completion of a byte or page write cycle. The latch is also reset if WP is brought low.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP

The **Write-In-Process (WIP)** bit indicates whether the X25040 is busy with a write operation. When set to a "1" a write is in progress, when set to a "0" no write is in progress. During a write all other bits are set to "1".

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a "1" the latch is set, when set to a "0" the latch is reset.

The **Block Protect (BP0 and BP1)** bits indicate the extent of protection employed. These bits are set by the user issuing the WRSR instruction.

Write Status Register (WRSR)

The write status register instruction allows the user to select one of four levels of protection. The X25040 is divided into four 1024-bit segments. One, two, or all four of the segments may be protected. That is, the user may read the segments but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	None
0	1	\$180-\$1FF
1	0	\$100-\$1FF
1	1	\$000-\$1FF

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register (Block Protect Bits)
READ	0000 0011	Read Data from Memory Array beginning at selected address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 4 Bytes)

\*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.



## X25040

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### DEVICE OPERATION

#### Clock and Data Timing

Data input on the SI line is sampled and latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

#### Read Sequence

The  $\overline{CS}$  line is first pulled low to select the device. The 8 bit read opcode is transmitted to the X25040, followed by the 8 bit byte address. After the read opcode and byte address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (\$1FF) the address counter rolls over to address \$000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking  $\overline{CS}$  high. Refer to the read operation sequence illustrated in Figure 2.

#### Write Sequence

Prior to any attempt to write data into the X25040 the write enable latch must first be set by issuing the WREN instruction. (See Fig. 3)  $\overline{CS}$  is first taken low, then the instruction is clocked into the X25040. After all eight bits of the instruction are transmitted,  $\overline{CS}$  must then be taken high. If the user continues the write operation without taking  $\overline{CS}$  high after issuing the WREN instruction the write operation will be ignored.

Once the write enable latch is set, the user may proceed by issuing the write instruction, followed by the address and then the data to be written. This is minimally a twenty-four clock operation.  $\overline{CS}$  must go low and remain low for the duration of the operation. The host may continue to write up to four bytes of data to the X25040. The only restriction is the four bytes must reside on the same page. A page address begins with address XXXX XX00 and ends with XXXX XX11. If the byte address counter reaches XXXX XX11 and the clock continues the counter will roll back to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed,  $\overline{CS}$  can only be brought high after the twenty-fourth, thirty-second, fortieth or fortyeighth clock. If it is brought high at any other time the write operation will not be completed. Refer to Figure 4 below for a detailed illustration of the page write sequence and time frames in which  $\overline{CS}$  going high are valid.

While the write is in progress the status register may be read to check the WIP bit. During this time the WIP bit will be high and all other bits in the status register will be high.

#### Hold Operation

The  $\overline{HOLD}$  input should be high (at  $V_{IH}$ ) under normal operation. If a data transfer is to be interrupted  $\overline{HOLD}$  can be pulled low to suspend the transfer until it can be resumed. The only restriction is the SCK input must be low when  $\overline{HOLD}$  is first pulled low and SCK must also be low when  $\overline{HOLD}$  is released.

The  $\overline{HOLD}$  input may be tied high either directly to  $V_{CC}$  or tied to  $V_{CC}$  through a resistor.

X25040

Operational Notes

- The X25040 powers-on in the following state:
- The device is in the low power standby state.
  - A high to low transition on  $\overline{CS}$  is required to enter an active state and receive an instruction.
  - $SO$  pin is high impedance.
  - The write enable latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The write enable latch is reset upon power-up.
- A write enable instruction must be issued to set the write enable latch.
- $\overline{CS}$  must come high at the proper clock count in order to start a write cycle.

The write enable latch is reset when  $\overline{WP}$  is brought low.

Figure 1. Read Operation Sequence

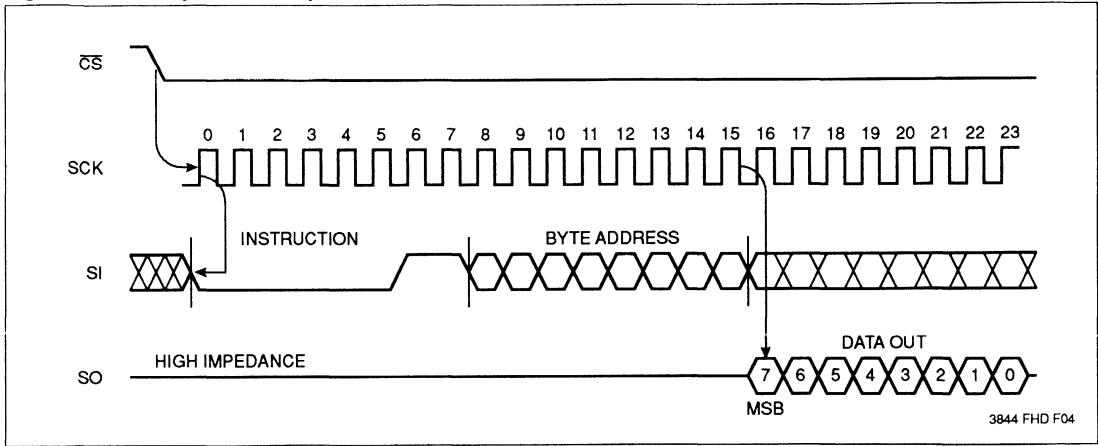


Figure 2. Write Enable Latch

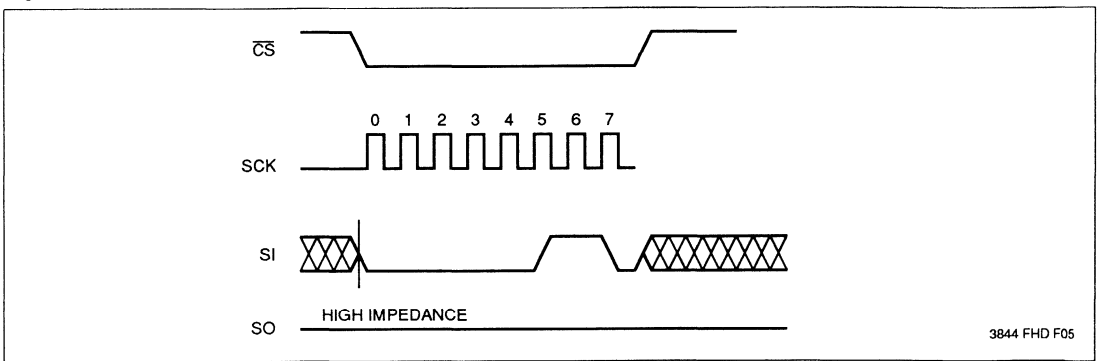


Figure 3. Write Operation Sequence

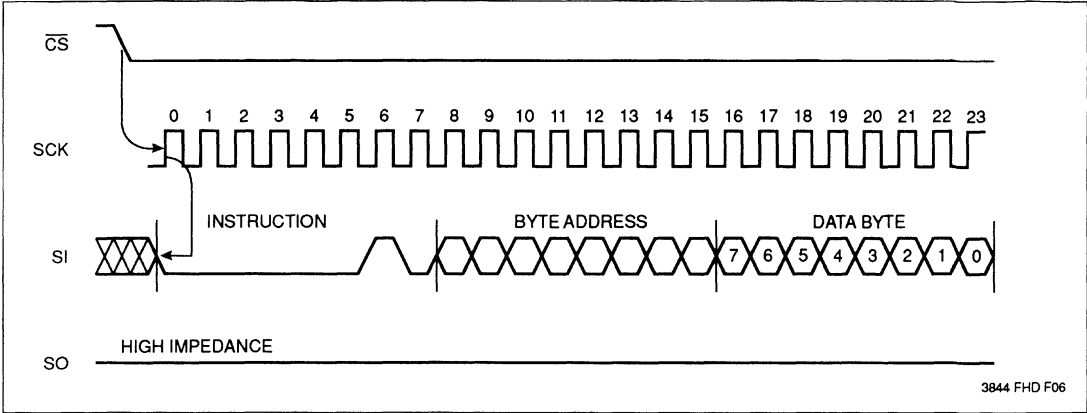
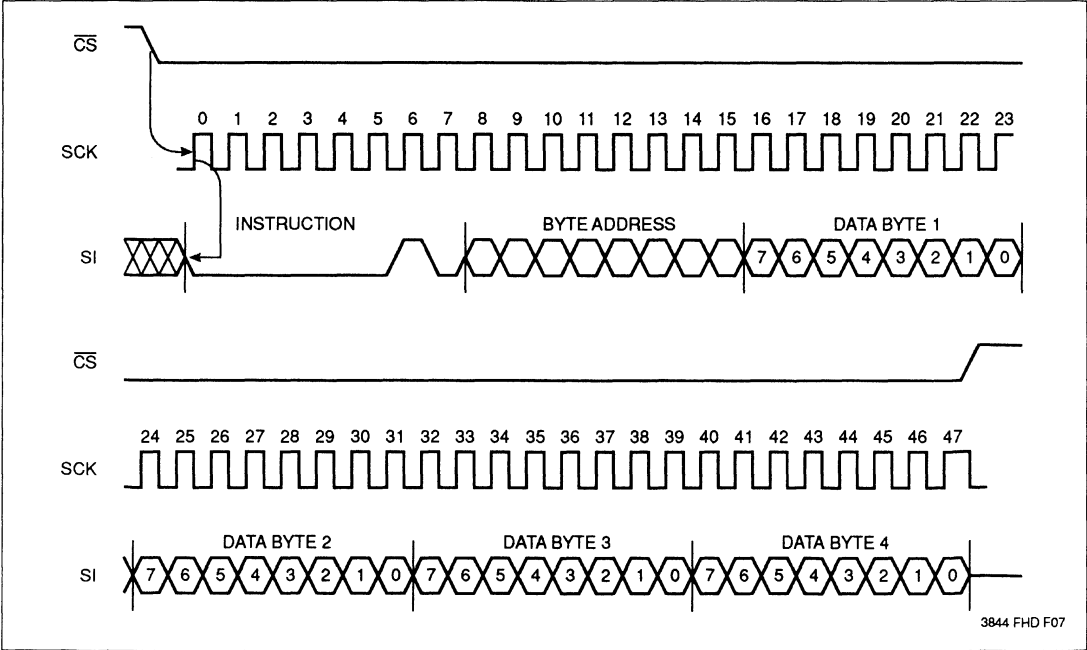


Figure 4. Page Write Operation Sequence



X25040

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	−65°C to +135°C
Storage Temperature .....	−65°C to +150°C
Voltage on any Pin with Respect to Ground	−1.0V to +7V
D.C. Output Current .....	5mA
Lead Temperature	
(Soldering, 10 Seconds) .....	300°C

\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

3844 PGM T03

Supply Voltage	Limits
X25040	5V ± 10%
X25040-3	3V to 5.5V

3844 PGM T04

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Supply Current (Active)		3	mA	SCK = V <sub>CC</sub> x 0.1/V <sub>CC</sub> x 0.9 @ 1MHz, SO = OPEN
I <sub>SB</sub>	V <sub>CC</sub> Supply Current (Standby)		150	µA	CS = V <sub>CC</sub> , V <sub>IN</sub> = Gnd or V <sub>CC</sub> − 0.3V
I <sub>LI</sub>	Input Leakage Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = GND to V <sub>CC</sub>
V <sub>IL</sub> <sup>(1)</sup>	Input Low Voltage	−1.0	V <sub>CC</sub> x 0.3	V	
V <sub>IH</sub> <sup>(1)</sup>	Input High Voltage	V <sub>CC</sub> x 0.7	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2mA
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> −0.8		V	I <sub>OH</sub> = −1.0mA

3844 PGM T05

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t <sub>PUR</sub> <sup>(1)</sup>	Power-up to Read Operation		1	ms
t <sub>PUW</sub> <sup>(1)</sup>	Power-up to Write Operation		5	ms

3844 PGM T09

CAPACITANCE T<sub>A</sub> = 25°C, f = 1.0MHz, V<sub>CC</sub> = 5V.

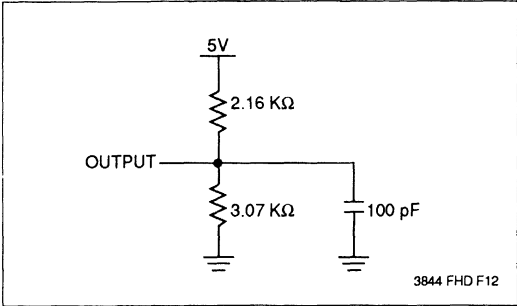
Symbol	Test	Max.	Units	Conditions
C <sub>OUT</sub> <sup>(2)</sup>	Output Capacitance (SO)	8	pF	V <sub>OUT</sub> = 0V
C <sub>IN</sub> <sup>(2)</sup>	Input Capacitance (SCK, SI, CS, WP, HOLD)	6	pF	V <sub>IN</sub> = 0V

3844 PGM T06

Notes: (1) V<sub>IL</sub> Min and V<sub>IH</sub> Max. are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.

# X25040

## EQUIVALENT A.C. LOAD CIRCUIT



## A.C. TEST CONDITIONS

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
Input and Output Timing Level	$V_{CC} \times 0.5$

3844 PGM T07

## A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

### Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f <sub>SCK</sub>	Clock Frequency	0	1	MHz
t <sub>CYC</sub>	Cycle Time	1000		ns
t <sub>LEAD</sub>	CS Lead Time	500		ns
t <sub>LAG</sub>	CS Lag Time	500		ns
t <sub>WH</sub>	Clock High Time	400		ns
t <sub>WL</sub>	Clock Low Time	400		ns
t <sub>SU</sub>	Data Setup Time	100		ns
t <sub>H</sub>	Data Hold Time	100		ns
t <sub>RI</sub>	Data In Rise Time		2.0	μs
t <sub>FI</sub>	Data In Fall Time		2.0	μs
t <sub>HD</sub>	HOLD Setup Time	200		ns
t <sub>CD</sub>	HOLD Hold Time	200		ns
t <sub>CS</sub>	CS Deselect Time	500		ns
t <sub>WC</sub> <sup>(4)</sup>	Write Cycle Time		10	ms

3844 PGM T08

### Data Output Timing

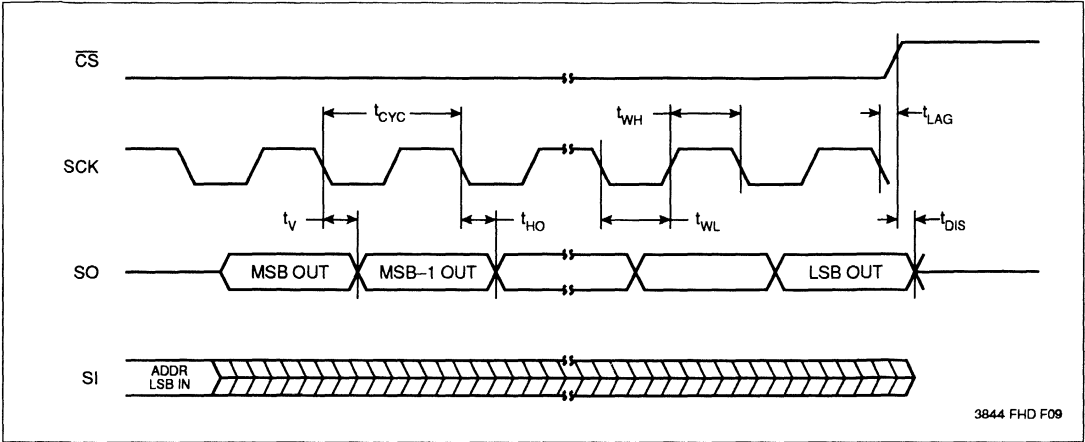
Symbol	Parameter	Min.	Max.	Units
f <sub>SCK</sub>	Clock Frequency	0	1	MHz
t <sub>DIS</sub>	Output Disable Time		500	ns
t <sub>V</sub>	Output Valid from clock Low		400	ns
t <sub>HO</sub>	Output Hold Time	0		ns
t <sub>RO</sub> <sup>(3)</sup>	Output Rise Time		300	ns
t <sub>FO</sub> <sup>(3)</sup>	Output Fall Time		300	ns
t <sub>LZ</sub>	HOLD High to Output in Low Z	100		ns
t <sub>HZ</sub>	HOLD Low to Output in High Z	100		ns

3844 PGM T09

**Notes:** (3) This parameter is periodically sampled and not 100% tested.

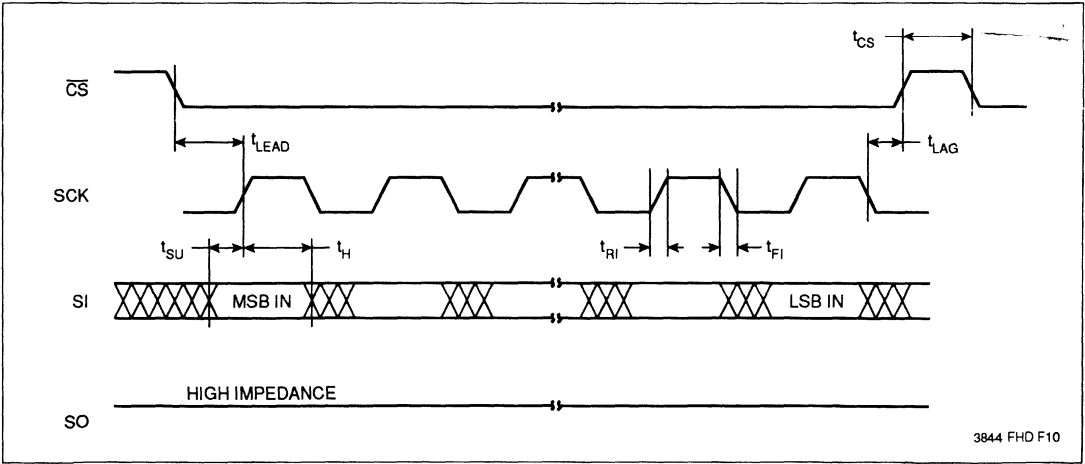
(4) t<sub>WC</sub> is the time from the rising edge of CS after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

Serial Output Timing



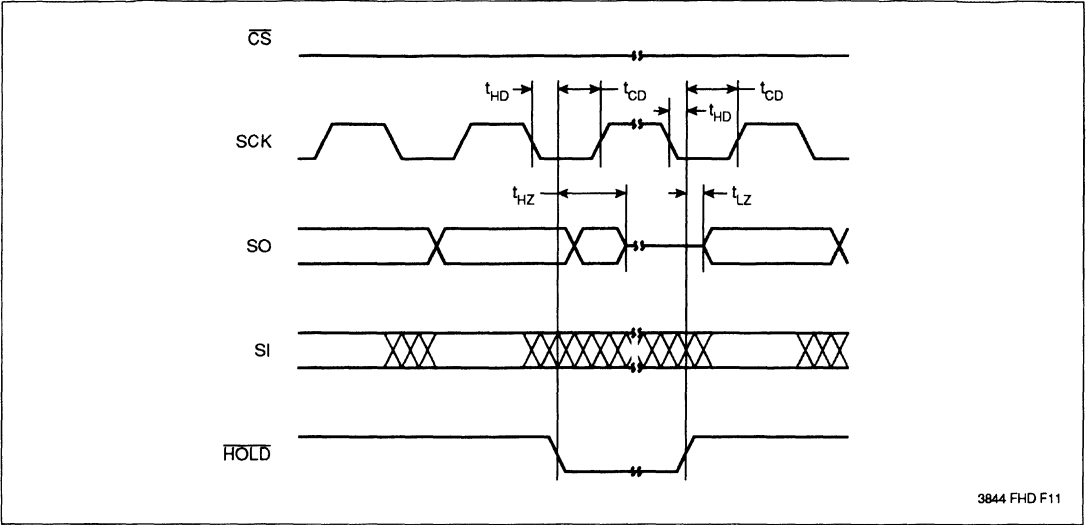
2

Serial Input Timing



**X25040**

**Hold Timing**



## SECURE Serial E<sup>2</sup>PROM

### FEATURES

- **64-Bit Password Security**
- **Three Password Modes**
  - Secure Read Access
  - Secure Write Access
  - Secure Configuration Access
- **Programmable Configuration**
  - Read, Write and Configuration Access Passwords
  - Block Access
  - Retry Register
  - ISO Response to Retry
- **Low Power CMOS**
  - 100µA Standby Current
  - 3mA Active Current
- **High Reliability**
  - Endurance: 100,000 Cycles Per Byte
  - Data Retention: 100 Years
  - ESD Protection: 2000V on All Pins

### DESCRIPTION

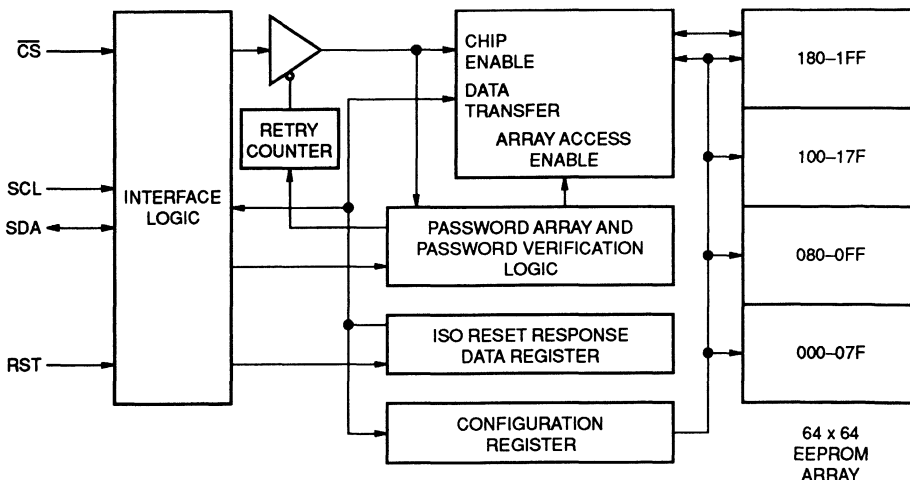
The X76041 is a CMOS 4096 bit serial E<sup>2</sup>PROM, internally organized as 512 x 8. The X76041 features a serial interface and software protocol allowing operation on a simple two wire bus. The bus signals are a clock input (SCL) and a bidirectional data input and output (SDA). Access to the device is controlled through a chip select input (CS), allowing any number of devices to share the same bus.

The X76041 also features three 64-bit programmable passwords for controlled access to the device; one for read operations, one for write operations and one for configuration of the device.

The X76041 also features a programmable response to reset output; providing an automatic output of a pre-configured 32-bit data stream conforming to the ISO standard for memory cards.

The X76041 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

### FUNCTIONAL DIAGRAM



3845 FHD F01



# X76041

## PIN DESCRIPTIONS

### Serial Data Input/Output (SDA)

SDA is a true three state serial data input/output pin. During a read cycle, data is shifted out on this pin. During a write cycle, data is shifted in on this pin.

### Reset (RST)

RST is a device reset pin. When pulsed high the X76041 will output the pre-configured 32-bit response to reset data word.

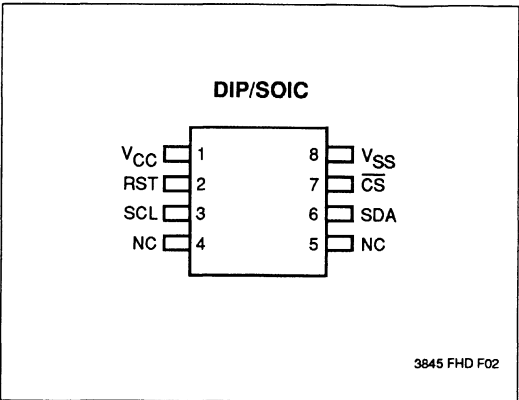
### Serial Clock (SCL)

The Serial Clock controls the serial bus timing for data input and output.

### Chip Select ( $\overline{CS}$ )

When CS is high, the X76041 is deselected and the SDA pin is at high impedance and unless an internal write operation is underway the X76041 will be in the standby power mode.  $\overline{CS}$  low enables the X76041, placing it in the active power mode.

## PIN CONFIGURATION



Symbol	Description
$\overline{CS}$	Chip Select Input
SDA	Serial Data Input/Output
RST	Reset Input
SCL	Serial Clock Input
Vss	Ground
Vcc	Supply Voltage
NC	No Connect

3845 PGM T01

### DEVICE OPERATION

The X76041 protocol is similar to that employed by the Xicor X24C02 family. The major difference is the absence of a device type identifier and device address. These are replaced by the  $\overline{CS}$  input which would allow multiple devices to occupy a single bus. The SDA I/O is not open drain but a true tri-state I/O with push/pull output.

The basic method of communication is established by first enabling the device ( $\overline{CS}$  low), generating a start condition and then transmitting a command and address field followed by the correct password; only then can the data transfer occur. The data are transferred in 8-bit segments, with each transfer being followed by an ACK generated by the receiving device. The basic sequence is illustrated in Figure 1.

There are three programmable passwords; one for read operations, one for write operations and one for configuration operations.

The device is shipped from the factory with the passwords in the programmed state—all 0's. This known state will allow the end user access into the configuration mode for programming of the passwords to be utilized.

#### Configuration Register

The array is divided into four 1K segments, each programmable to different levels of security and functionality.

Mode 0: Read/Write access.

Mode 1: Read access, all write operations locked out.

Mode 2: Read access and program only (writing, but only able to change a 1 to 0). If an attempt to change a 0 to a 1 occurs the X76041 will reset the command register, not respond with an ACK and enter the standby power mode.

Mode 3: No read or write access to the memory. Access only through use of the configuration password.

#### Retry Register/Counter

The retry register is accessible in the configuration mode and a value of 0 to 255 may be programmed. This defines the number of unsuccessful attempts to access the device the user will allow. Operating in conjunction with this retry register is a nonvolatile counter maintaining a count of unsuccessful access attempts. A compare is made between register and counter and if equal a user defined action will be taken.

#### Response to Reset

Whenever the RST input is driven high, the X76041 will automatically output a 32-bit data stream. The data are output at the same rate as the SCL input; in this mode as fast as 1 MHz.

#### User Modes

User modes require issuing the 3-bit command followed by the address, password and then the data transfer as illustrated in Figure 1. The commands are:

Write = 000

Read = 001

Write operations may be 1 or more (up to 8) bytes to the selected address.

#### Read Operations

Sequential—Once past the password acceptance area, the host can read sequentially within the originally addressed 1K-bit segment of memory. An acknowledge must follow each 8-bit data transfer. After the last bit has been read a stop condition is generated without a preceding acknowledge.

Random—truly random in that the address is supplied with the read command. Once past the password and first byte has been read another start can be issued followed by a new 8-bit address. Note this is an 8-bit address allowing random reads only within the original block. To access the other blocks a stop must be issued followed by a new command address password sequence.





16K

X2816C

2048 x 8 Bit

## 5 Volt, Byte Alterable E<sup>2</sup>PROM

### FEATURES

- 90 ns Access Time
- SIMPLE Byte and Page Write
  - Single 5 Volt Supply
  - No External High Voltages or V<sub>PP</sub> Control Circuits
  - Self Timed
  - No Erase Before Write
  - No Complex Programming Algorithms
  - No Overerase Problem
- High Performance Advanced NMOS Technology
- Fast Write Cycle Times
  - 16-Byte Page Write Operation
  - Byte or Page Write Cycle: 5 ms Typical
  - Complete Memory Rewrite: 640 ms Typical
  - Effective Byte Write Cycle Time: 300  $\mu$ s Typical
- DATA Polling
  - Allows User to Minimize Write Cycle Time
- JEDEC Approved Byte-Wide Pinout
- High Reliability
  - Endurance: 10,000 Cycles
  - Data Retention: 100 Years

### DESCRIPTION

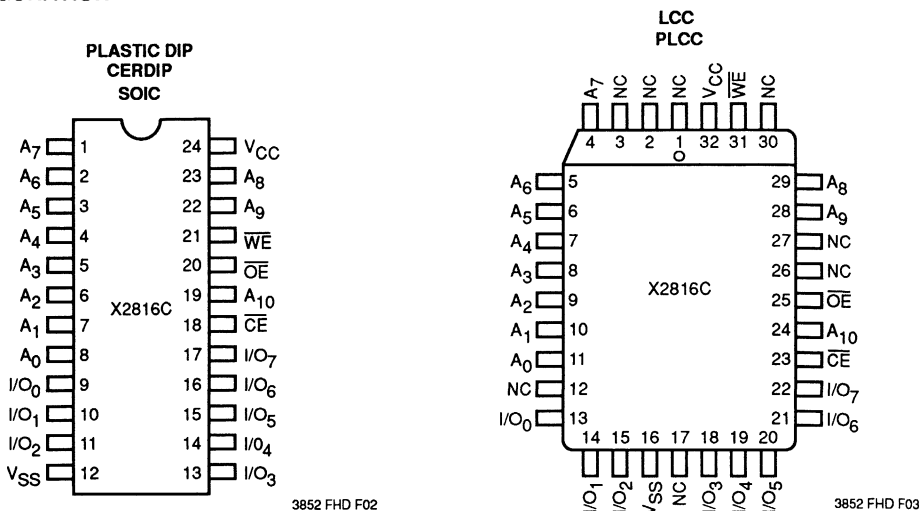
The Xicor X2816C is a 2K x 8 E<sup>2</sup>PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor Programmable nonvolatile memories it is a 5V only device. The X2816C features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2816C supports a 16-byte page write operation, typically providing a 300  $\mu$ s/byte write cycle, enabling the entire memory to be written in less than 640 ms. The X2816C also features DATA Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

3

### PIN CONFIGURATION



# X2816C

## PIN DESCRIPTIONS

### Addresses (A<sub>0</sub>–A<sub>10</sub>)

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{\text{CE}}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{\text{CE}}$  is HIGH, power consumption is reduced.

### Output Enable ( $\overline{\text{OE}}$ )

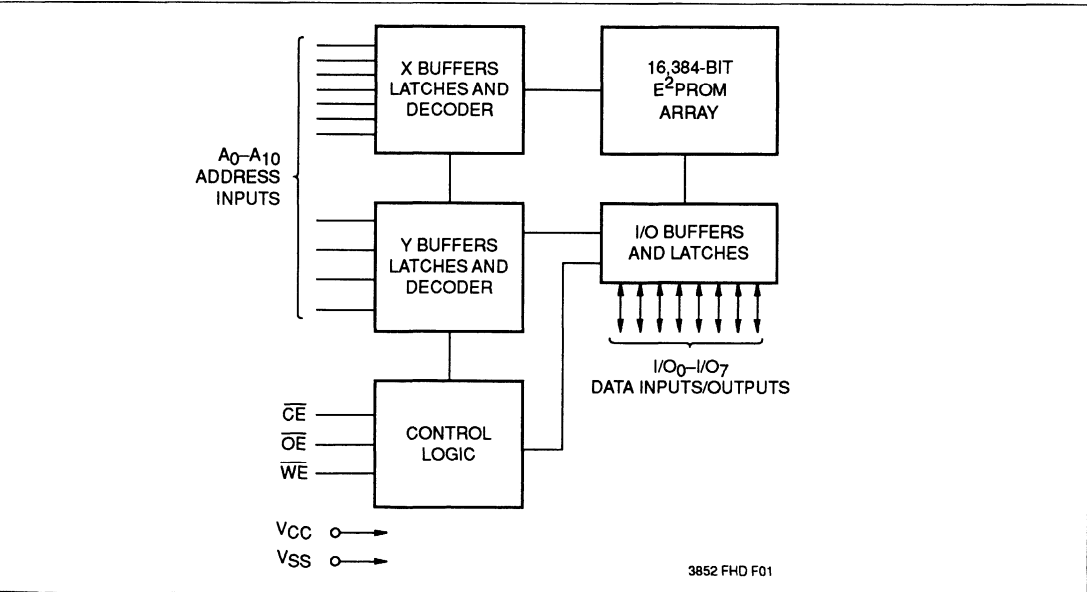
The Output Enable input controls the data output buffers and is used to initiate read operations.

## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>10</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Data Input/Output
WE	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

3852 PGM T01

## FUNCTIONAL DIAGRAM



## X2816C

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### DEVICE OPERATION

#### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW and  $\overline{WE}$  HIGH. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

#### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The X2816C supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

#### Page Write Operation

The page write feature of the X2816C allows the entire memory to be typically written in 640 ms. Page write allows two to sixteen bytes of data to be consecutively written to the X2816C prior to the commencement of the internal programming cycle. Although the host system may read data from any location in the system to transfer to the X2816C, the destination page address of the X2816C should be the same on each subsequent strobe of the  $\overline{WE}$  and  $\overline{CE}$  inputs. That is,  $A_4$  through  $A_{10}$  must be the same for each transfer of data to the X2816C during a page write cycle.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to fifteen bytes in the same manner as the first byte was written. Each successive

byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 20  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 20  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 20  $\mu$ s.

#### DATA Polling

The X2816C features  $\overline{DATA}$  Polling as a method to indicate to the host system that the byte write or page write cycle has completed.  $\overline{DATA}$  Polling allows a simple bit test operation to determine the status of the X2816C, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on  $I/O_7$  (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete,  $I/O_7$  will reflect true data.

#### WRITE PROTECTION

There are three features that protect the nonvolatile data from inadvertent writes.

- Noise Protection—A  $\overline{WE}$  pulse which is typically less than 10 ns will not initiate a write cycle.
- Vcc Sense—All functions are inhibited when  $V_{cc}$  is  $\leq 3V$ , typically.
- Write Inhibit—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH, or  $\overline{CE}$  HIGH during power-on and power-off, will inhibit inadvertent writes. Write cycle timing specifications must be observed concurrently.

#### ENDURANCE

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance.

## X2816C

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### SYSTEM CONSIDERATIONS

Because the X2816C is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2816C has two power modes, standby and active, proper decoupling of the memory array is of

prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu$ F high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7  $\mu$ F electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

X2816C

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X2816C	−10°C to +85°C
X2816CI, X2816CM	−65°C to +135°C
Storage Temperature	
Voltage on any Pin with	−65°C to +150°C
Respect to Ground	−1.0V to +7V
D.C. Output Current	5 mA
Lead Temperature (Soldering, 10 Seconds)	300°C

\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

3852 PGM T02

Supply Voltage	Limits
X2816C	5V ± 10%

3852 PGM T03

3

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Current (Active)		70	110	mA	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = V <sub>CC</sub>
I <sub>SB1</sub>	V <sub>CC</sub> Current (Standby)		35	50	mA	$CE = V_{IH}, \overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = V <sub>CC</sub>
I <sub>LI</sub>	Input Leakage Current			10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current			10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , $\overline{CE} = V_{IH}$
V <sub>IL</sub> (2)	Input Low Voltage	−1.0		0.8	V	
V <sub>IH</sub> (2)	Input High Voltage	2.0		V <sub>CC</sub> + 1.0	V	
V <sub>OL</sub>	Output Low Voltage			0.4	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = −400 μA

3852 PGM T02

Notes: (1) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage and are not tested.  
(2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.



X2816C

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Unit
Minimum Endurance	10,000		Cycles/Byte
Data Retention	100		Years

3852 PGM T03

POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
tPUR(3)	Power-Up to Read Operation	1	ms
tPUW(3)	Power-Up to Write Operation	5	ms

3852 PGM T04

CAPACITANCE TA = 25°C, f = 1.0 MHz, VCC = 5V

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (3)	Input/Output Capacitance	10	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (3)	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

3852 PGM T05

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

3852 PGM T06

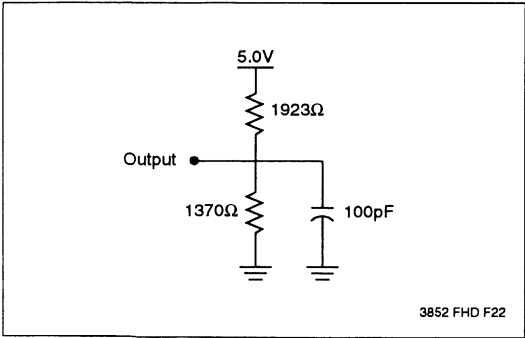
MODE SELECTION

CE	OE	WE	Mode	I/O	Power
L	L	H	Read	DOUT	Active
L	H	L	Write	DIN	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3852 PGM T07

Note: (3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUITS



3852 FHD F22

X2816C

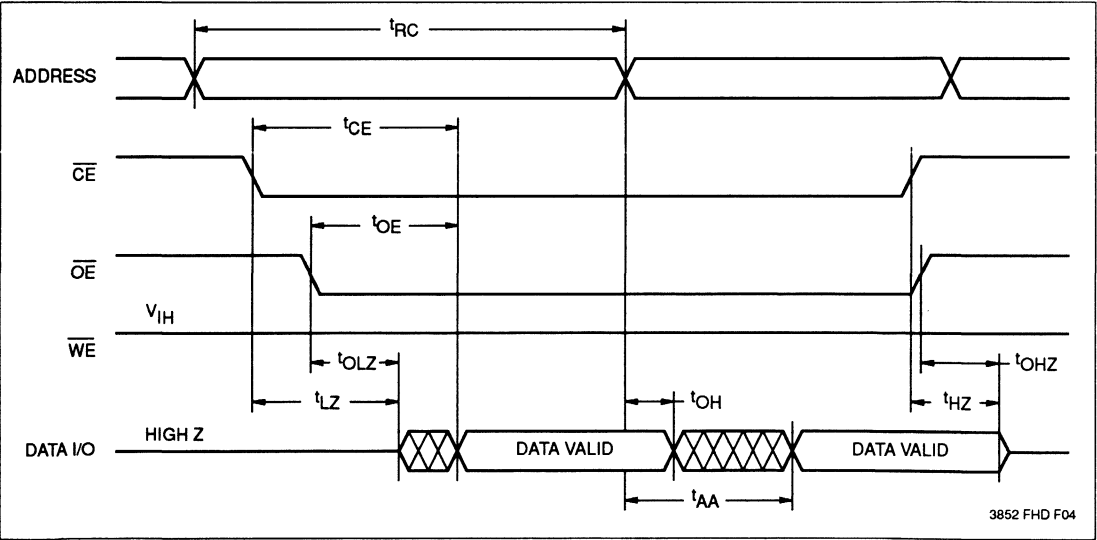
A.C. CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X2816C-90		X2816C-12		X2816C-15		X2816C-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	90		120		150		200		ns
t <sub>CE</sub>	Chip Enable Access Time		90		120		150		200	ns
t <sub>AA</sub>	Address Access Time		90		120		150		200	ns
t <sub>OE</sub>	Output Enable Access Time		60		60		80		100	ns
t <sub>LZ</sub> <sup>(4)</sup>	CE Low to Active Output	0		0		0		0		ns
t <sub>OLZ</sub> <sup>(4)</sup>	OE Low to Active Output	0		0		0		0		ns
t <sub>HZ</sub> <sup>(4)</sup>	CE High to High Z Output		50		60		60		60	ns
t <sub>OHZ</sub> <sup>(4)</sup>	OE High to High Z Output		50		60		60		60	ns
t <sub>OH</sub>	Output Hold from Address Change	0		0		0		0		ns

3852 pgm 110

Read Cycle



3852 FHD F04

Notes: (4)  $t_{LZ}$  min.,  $t_{HZ}$ ,  $t_{OLZ}$ , and  $t_{OHZ}$  are periodically sampled and not 100% tested.  $t_{HZ}$  max. and  $t_{OHZ}$  max. are measured from the point when  $\overline{CE}$  or  $\overline{OE}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

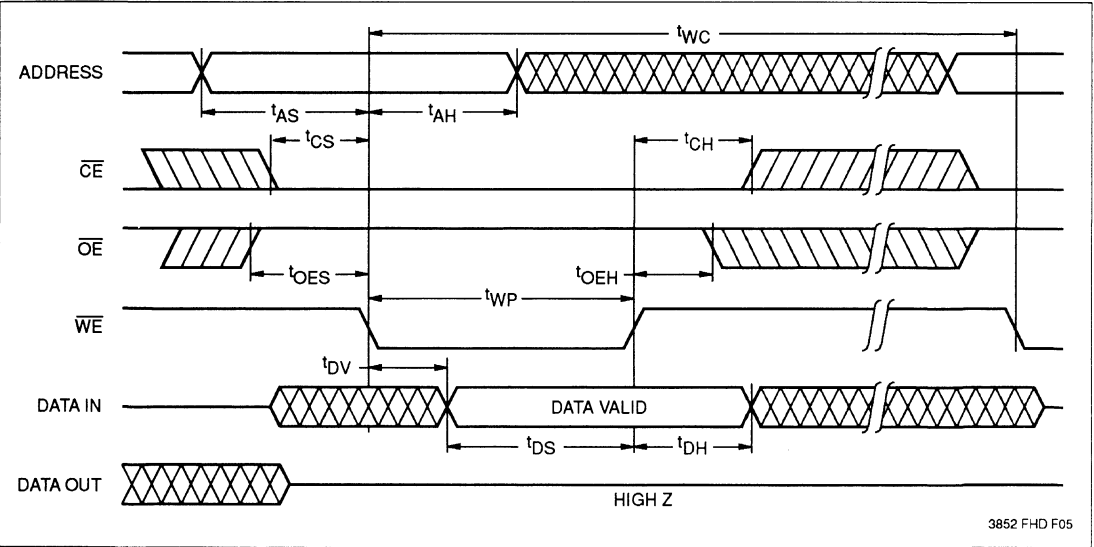
# X2816C

## Write Cycle Limits

Symbol	Parameter	X2816C-90		X2816C-12,-15,-20		Units
		Min.	Max.	Min.	Max.	
$t_{WC}^{(5)}$	Write Cycle Time		10		10	ms
$t_{AS}$	Address Setup Time	5		5		ns
$t_{AH}$	Address Hold Time	80		100		ns
$t_{CS}$	Write Setup Time	0		0		ns
$t_{CH}$	Write Hold Time	0		0		ns
$t_{CW}$	$\overline{CE}$ Pulse Width	80		100		ns
$t_{OES}$	$\overline{OE}$ High Setup Time	10		10		ns
$t_{OEH}$	$\overline{OE}$ High Hold Time	5		10		ns
$t_{WP}$	$\overline{WE}$ Pulse Width	80		100		ns
$t_{WPH}$	$\overline{WE}$ High Recovery	50		50		ns
$t_{DV}$	Data Valid		100		100	$\mu$ s
$t_{DS}$	Data Setup	35		50		ns
$t_{DH}$	Data Hold	5		10		ns
$t_{DW}$	Delay to Next Write	10		10		$\mu$ s
$t_{BLC}$	Byte Load Cycle	1	100	1	100	$\mu$ s

3852 PGM T09

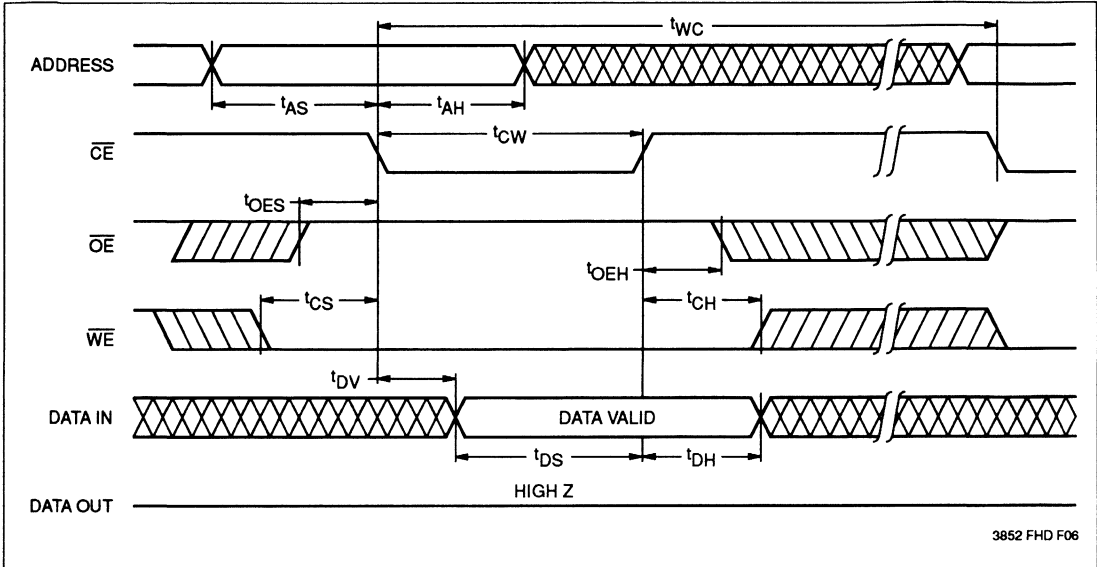
## WE Controlled Write Cycle



**Notes:** (5)  $t_{WC}$  is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation. For faster  $t_{WC}$ , please refer to X28C16 and X28HC16 product data sheets.

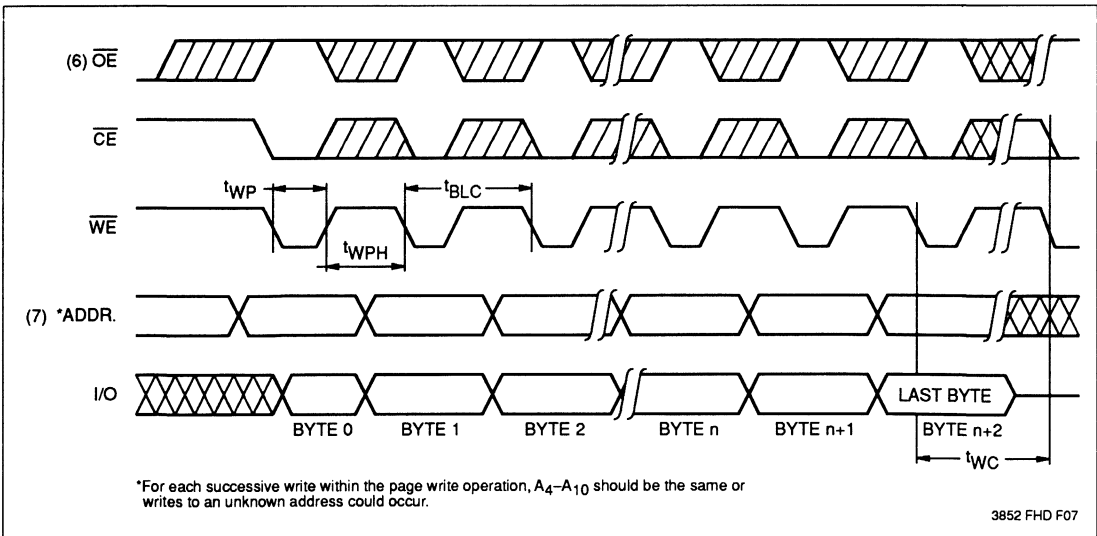
# X2816C

## $\overline{\text{CE}}$ Controlled Write Cycle



3

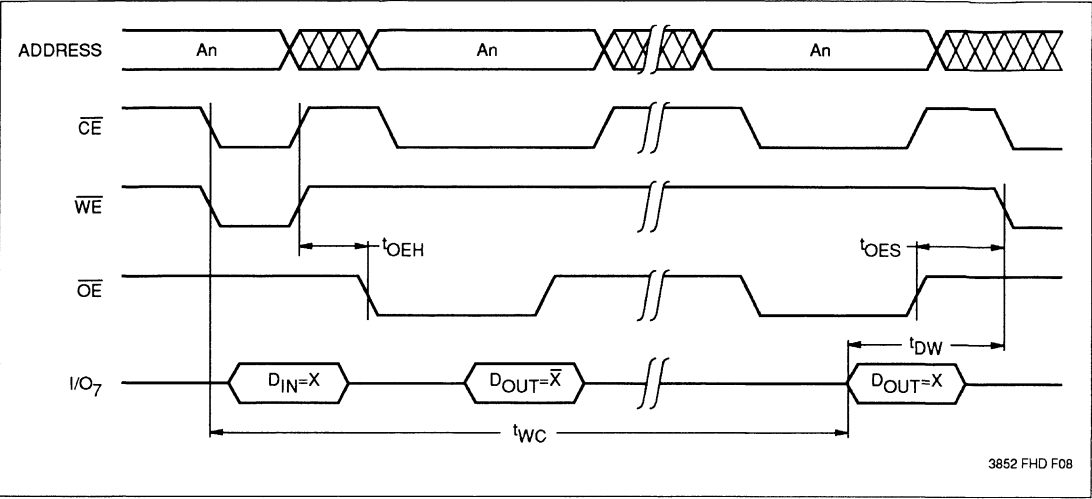
## Page Mode Write Cycle



- Notes:** (6) Between successive byte writes within a page write operation,  $\overline{\text{OE}}$  can be strobed LOW: e.g. this can be done with  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  HIGH to fetch data from another memory device within the system for the next write; or with  $\overline{\text{WE}}$  HIGH and  $\overline{\text{CE}}$  LOW effectively performing a polling operation.
- (7) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  controlled write cycle timing.

X2816C

DATA Polling Timing Diagram<sup>(10)</sup>



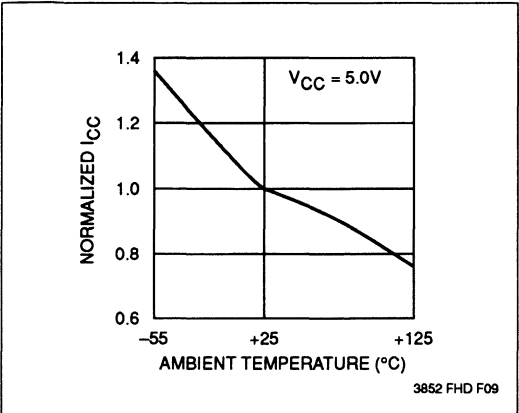
**Note:** (10) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

SYMBOL TABLE

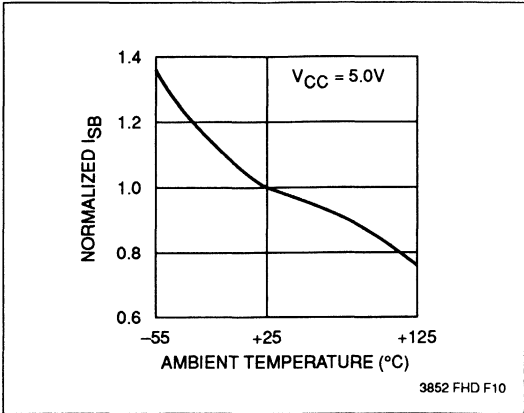
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

# X2816C

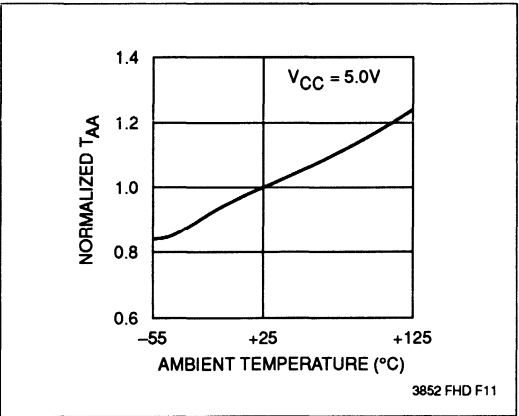
**Normalized Active Supply Current  
vs. Ambient Temperature**



**Normalized Standby Supply Current  
vs. Ambient Temperature**



**Normalized Access Time  
vs. Ambient Temperature**



**X2816C**

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**NOTES**



## Advance Information

16K

X28C16

2K x 8 Bit

## 5 Volt, Byte Alterable E<sup>2</sup>PROM

### FEATURES

- 150 ns Access Time
- SIMPLE Byte and Page Write
  - Single 5 Volt Supply
  - No External High Voltages or V<sub>PP</sub> Control Circuits
  - Self Timed
  - No Erase Before Write
  - No Complex Programming Algorithms
  - No Overerase Problem
- Low Power CMOS
  - 40 mA Active Current Max.
  - 200  $\mu$ A Standby Current Max.
- Fast Write Cycle Times
  - 64-Byte Page Write Operation
  - Byte or Page Write Cycle: 2 ms Typical
  - Complete Memory Rewrite: 0.1 Sec. Typical
  - Effective Byte Write Cycle Time: 32  $\mu$ s Typical
- Software Data Protection
- End of Write Detection
  - DATA Polling
  - Toggle Bit
- High Reliability
  - Endurance: 10,000 Cycles
  - Data Retention: 100 Years
- JEDEC Approved Byte-Wide Pinout

### DESCRIPTION

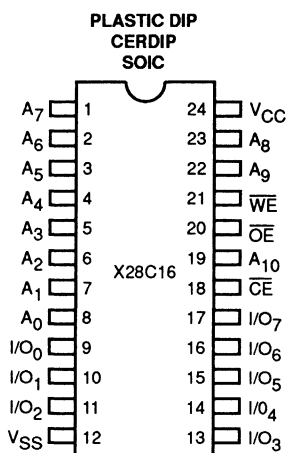
The X28C16 is an 2K x 8 E<sup>2</sup>PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C16 is a 5V only device. The X28C16 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C16 supports a 64-byte page write operation, effectively providing a 32 $\mu$ s/byte write cycle and enabling the entire memory to be typically written in 0.1 seconds. The X28C16 also features DATA and Toggle Bit Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C16 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

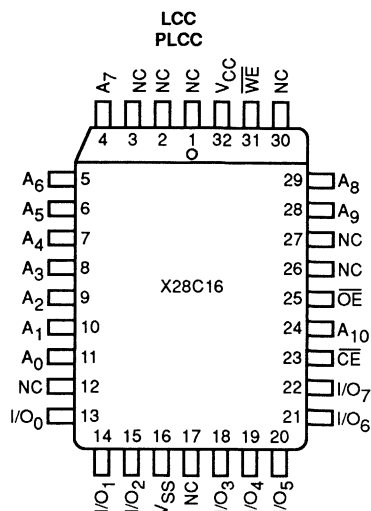
Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

3

### PIN CONFIGURATION



3851 FHD F02



3851 FHD F03



# X28C16

## PIN DESCRIPTIONS

### Addresses (A<sub>0</sub>–A<sub>10</sub>)

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{\text{CE}}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{\text{CE}}$  is HIGH, power consumption is reduced.

### Output Enable ( $\overline{\text{OE}}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

### Data In/Data Out (I/O<sub>0</sub>–I/O<sub>7</sub>)

Data is written to or read from the X28C16 through the I/O pins.

### Write Enable ( $\overline{\text{WE}}$ )

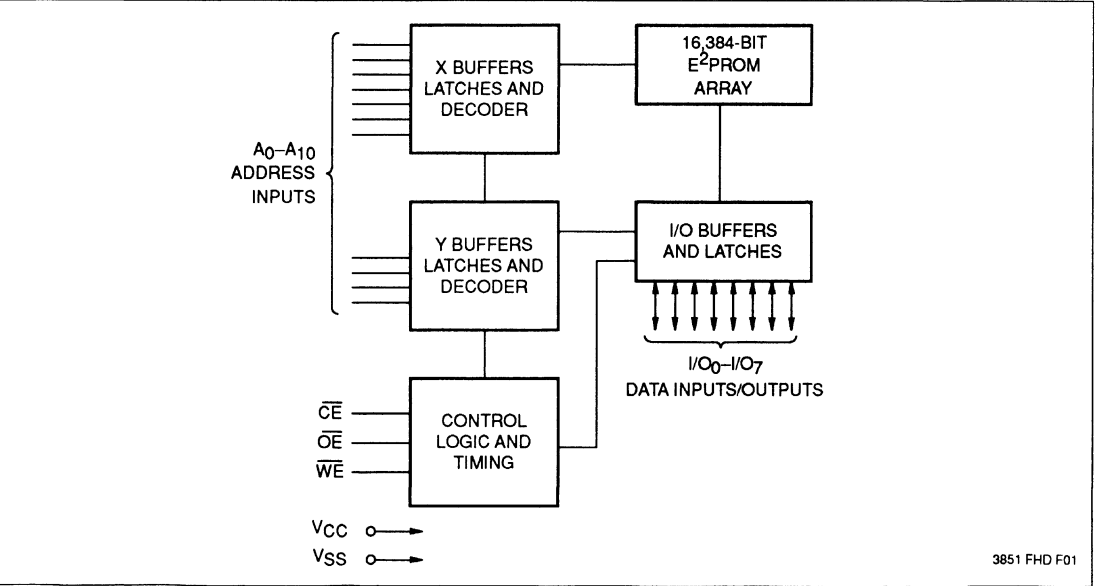
The Write Enable input controls the writing of data to the X28C16.

## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>10</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

3851 PGM T01

## FUNCTIONAL DIAGRAM



3851 FHD F01

# X28C16

## DEVICE OPERATION

### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The X28C16 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 2 ms.

### Page Write Operation

The page write feature of the X28C16 allows the entire memory to be written in 0.25 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C16 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address ( $A_6$  through  $A_{10}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

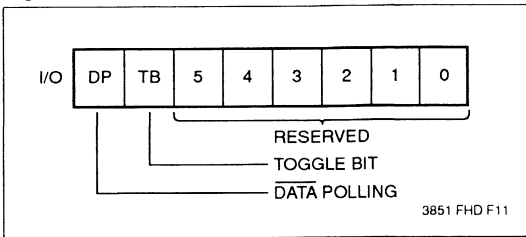
The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host

continues to access the device within the byte load cycle time of 100  $\mu$ s.

### Write Operation Status Bits

The X28C16 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



### DATA Polling (I/O<sub>7</sub>)

The X28C16 features  $\overline{DATA}$  Polling as a method to indicate to the host system that the byte write or page write cycle has completed.  $\overline{DATA}$  Polling allows a simple bit test operation to determine the status of the X28C16, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O<sub>7</sub> (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O<sub>7</sub> will reflect true data. Note: If the X28C16 is in the protected state and an illegal write operation is attempted  $\overline{DATA}$  Polling will not operate.

### Toggle Bit (I/O<sub>6</sub>)

The X28C16 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O<sub>6</sub> will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

# X28C16

DATA Polling I/O<sub>7</sub>  
Figure 2. DATA Polling Bus Sequence

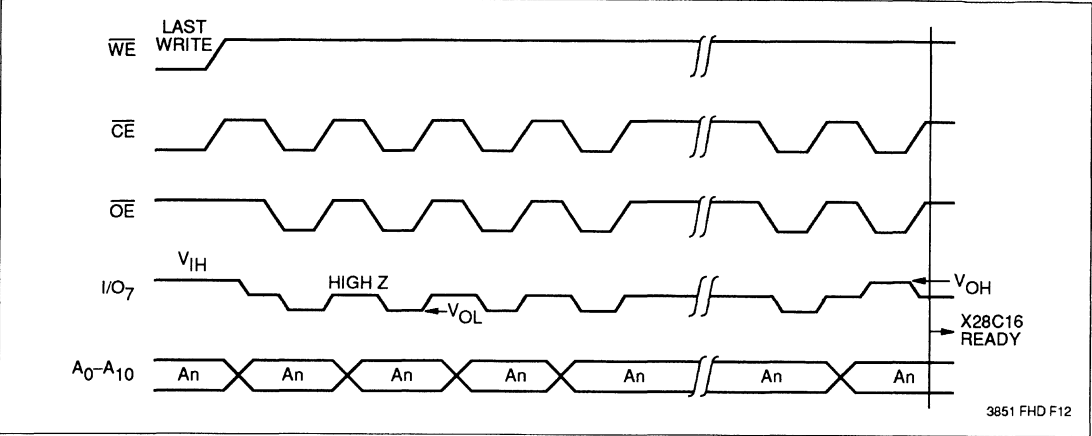
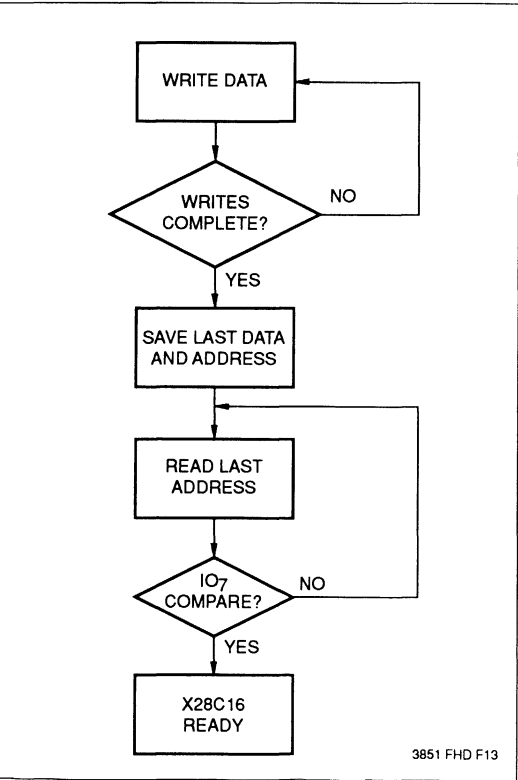


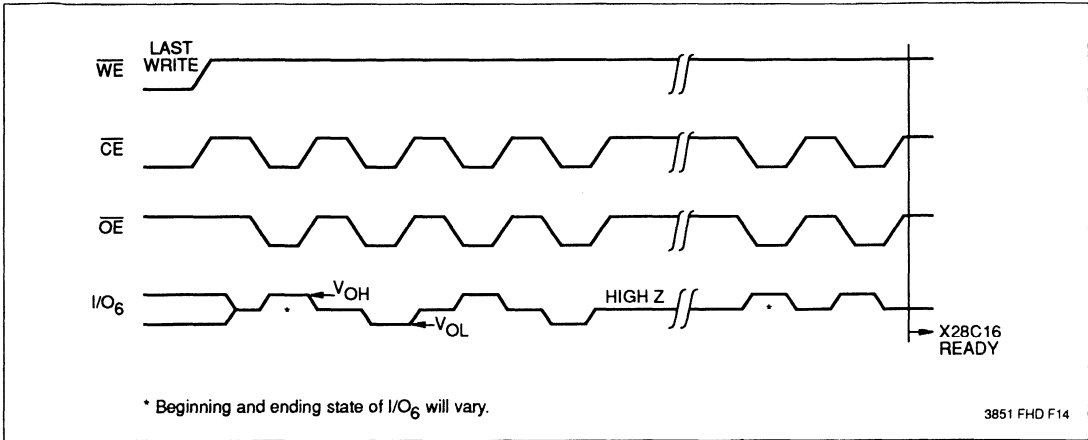
Figure 3. DATA Polling Software Flow



DATA Polling can effectively halve the time for writing to the X28C16. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

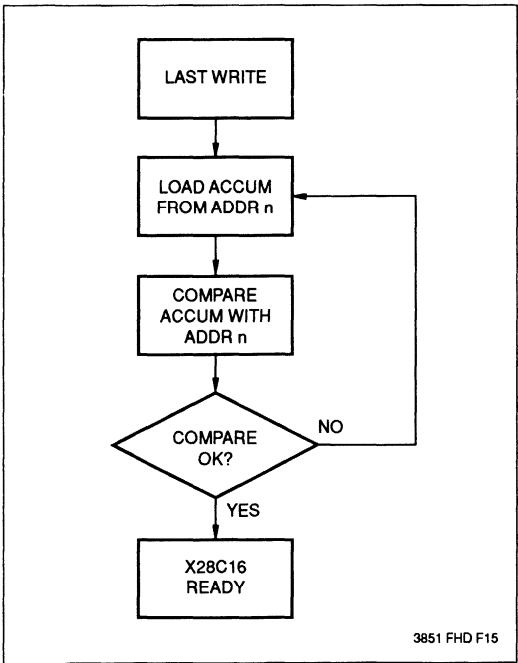
# X28C16

The Toggle Bit I/O<sub>6</sub>  
Figure 4. Toggle Bit Bus Sequence



3

Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28C16 memories that is frequently updated. Toggle Bit testing can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

## X28C16

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### HARDWARE DATA PROTECTION

The X28C16 provides three hardware features (compatible with X2816C) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A  $\overline{WE}$  pulse typically less than 20 ns will not initiate a write cycle.
- Default  $V_{CC}$  Sense—All write functions are inhibited when  $V_{CC}$  is  $\leq 3V$  typically.
- Write Inhibit—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH, or  $\overline{CE}$  HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

### SOFTWARE DATA PROTECTION

The X28C16 offers a software controlled data protection feature. The X28C16 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once  $V_{CC}$  was stable.

The X28C16 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C16 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

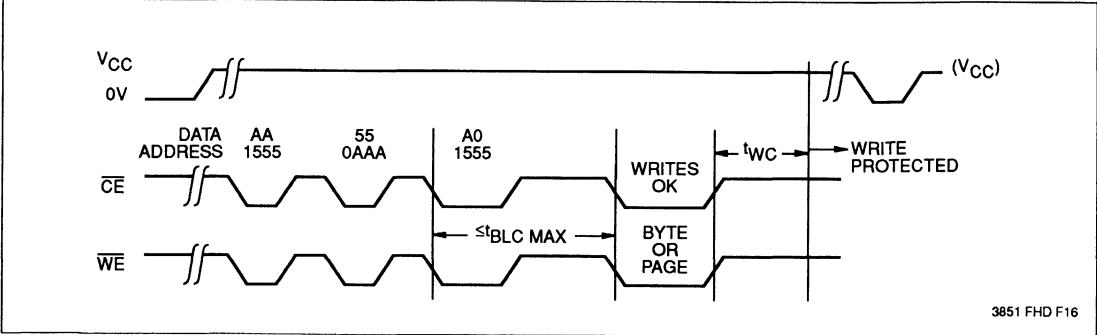
### SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data\*. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

*Note: \*Once the three byte sequence is issued it must be followed by a valid byte or page write operation.*

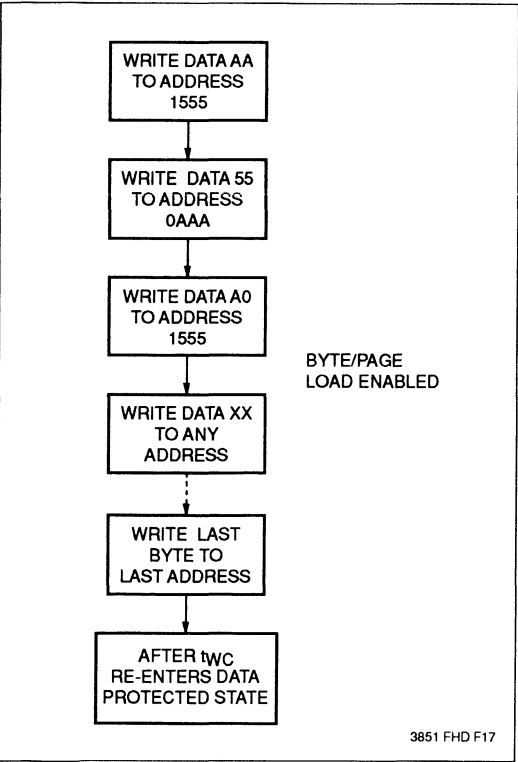
X28C16

Software Data Protection  
Figure 6. Timing Sequence—Byte or Page Write



3

Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C16 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C16 will be write protected during power-down and after any subsequent power-up.

*Note:* Once initiated, the sequence of write operations should not be interrupted.

## X28C16

### Resetting Software Data Protection

Figure 8. Reset Software Data Protection Timing Sequence

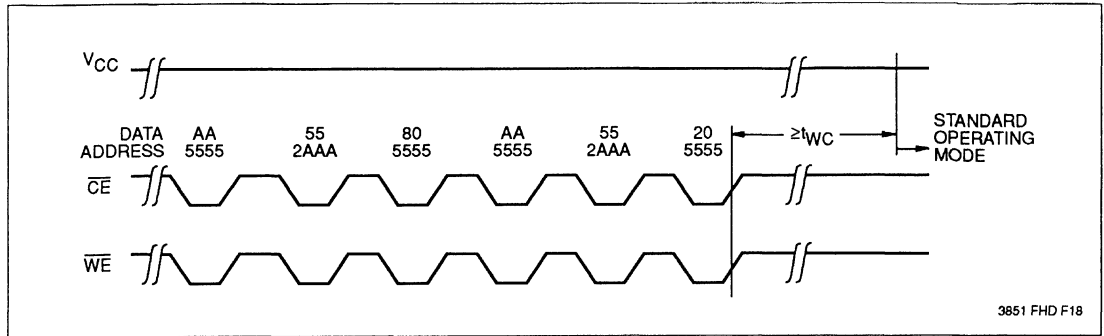
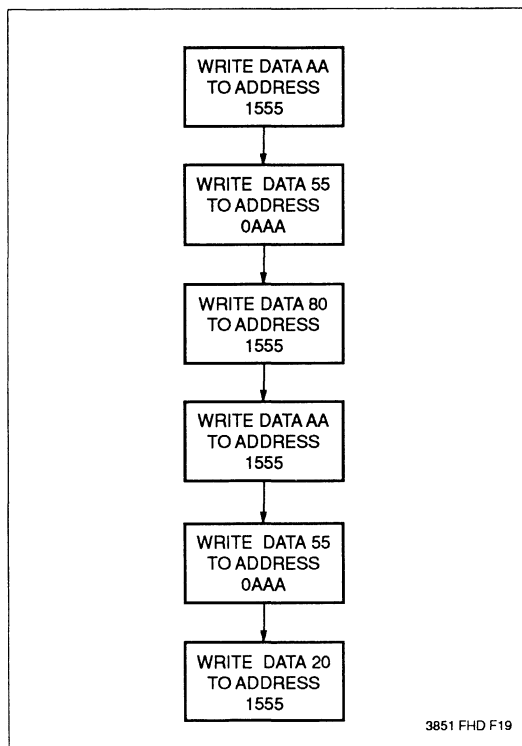


Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E<sup>2</sup>PROM programmer, the following six step algorithm will reset the internal protection circuit. After  $t_{WC}$ , the X28C16 will be in standard operating mode.

**Note:** \*Once initiated, the sequence of write operations should not be interrupted.

\*It should also be noted, the Reset SDP operation performs a device "program" operation; whereby **all** bytes are written to 00[H].

## X28C16

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### SYSTEM CONSIDERATIONS

Because the X28C16 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C16 has two power modes, standby and active, proper decoupling of the memory array is of

prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu\text{F}$  high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7  $\mu\text{F}$  electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.



# X28C16

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X28C16	–10°C to +85°C
X28C16I, X28C16M	–65°C to +135°C
Storage Temperature	–65°C to +150°C
Voltage on any Pin with Respect to Ground	–1.0V to +7.0V
D.C. Output Current	5 mA
Lead Temperature (Soldering, 10 Seconds)	300°C

## \*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

Supply Voltage	Limits
X28C16	5V ± 10%

## D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Current (Active) (TTL Inputs)		15	40	mA	$\overline{CE} = \overline{OE} = V_{IL}$ , $\overline{WE} = V_{IH}$ , All I/O's = Open, Address Inputs = 0.4V/2.4V Levels @ f = 5MHz
I <sub>SB1</sub>	V <sub>CC</sub> Current (Standby) (TTL Inputs)		1	2	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ , All I/O's = Open, Other Inputs = V <sub>IH</sub>
I <sub>SB2</sub>	V <sub>CC</sub> Current (Standby) (CMOS Inputs)		100	200	μA	$\overline{CE} = \overline{WE} = V_{CC} - 0.3V$ , All I/O's = Open, Other Inputs = Don't Care
I <sub>LI</sub>	Input Leakage Current			±10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current			±10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , $\overline{CE} = V_{IH}$
V <sub>IL</sub> (2)	Input Low Voltage	–1.0		0.8	V	
V <sub>IH</sub> (2)	Input High Voltage	2.0		V <sub>CC</sub> + 1.0	V	
V <sub>OL</sub>	Output Low Voltage			0.4	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = –400 μA

3851 PGM T02

Notes: (1) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage and are not tested.

(2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.

X28C16

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Minimum Endurance	10,000	Cycles/Byte
Data Retention	100	Years

3851 PGM T03

POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
tPUR(3)	Power-up to Read Operation	100	µs
tPUW(3)	Power-up to Write Operation	5	ms

3851 PGM T04

CAPACITANCE TA = 25°C, f = 1.0 MHz, VCC = 5V

Symbol	Parameter	Max.	Units	Test Conditions
CIO(3)	Input/Output Capacitance	10	pF	VIO = 0V
CIN(3)	Input Capacitance	6	pF	VIN = 0V

3851 PGM T05

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V

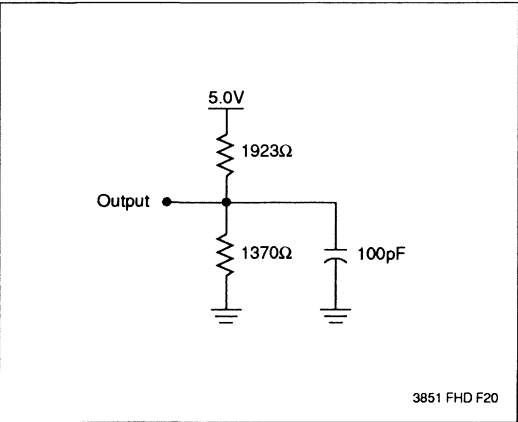
3851 PGM T06

MODE SELECTION

CE	OE	WE	Mode	I/O	Power
L	L	H	Read	DO <sub>OUT</sub>	Active
L	H	L	Write	DI <sub>IN</sub>	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3851 PGM T07

EQUIVALENT A.C. LOAD CIRCUIT



Note: (3) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

# X28C16

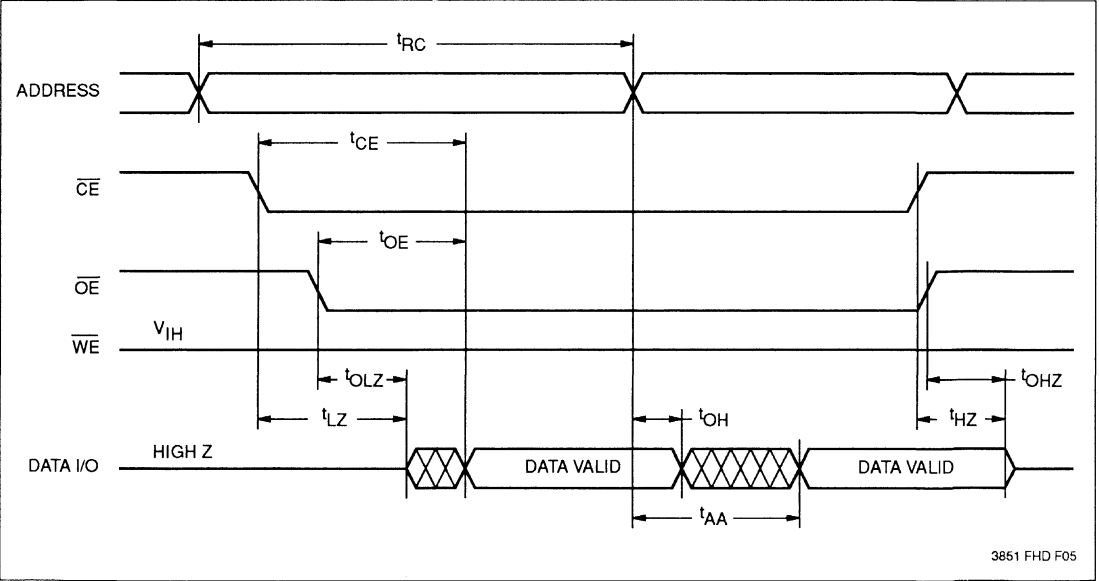
## A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified.)

### Read Cycle Limits

Symbol	Parameter	X28C16-15		X28C16-20		X28C16-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	150		200		250		ns
$t_{CE}$	Chip Enable Access Time		150		200		250	ns
$t_{AA}$	Address Access Time		150		200		250	ns
$t_{OE}$	Output Enable Access Time		70		80		100	ns
$t_{LZ}^{(4)}$	$\overline{CE}$ Low to Active Output	0		0		0		ns
$t_{OLZ}^{(4)}$	$\overline{OE}$ Low to Active Output	0		0		0		ns
$t_{HZ}^{(4)}$	$\overline{CE}$ High to High Z Output		50		50		50	ns
$t_{OHZ}^{(4)}$	$\overline{OE}$ High to High Z Output		50		50		50	ns
$t_{OH}$	Output Hold from Address Change	0		0		0		ns

3856 PGM T08

### Read Cycle



3851 FHD F05

**Notes:** (4)  $t_{LZ}$  min.,  $t_{HZ}$ ,  $t_{OLZ}$  min., and  $t_{OHZ}$  are periodically sampled and not 100% tested.  $t_{HZ}$  max. and  $t_{OHZ}$  max. are measured, with  $C_L = 5\text{pF}$ , from the point when  $\overline{CE}$  or  $\overline{OE}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

X28C16

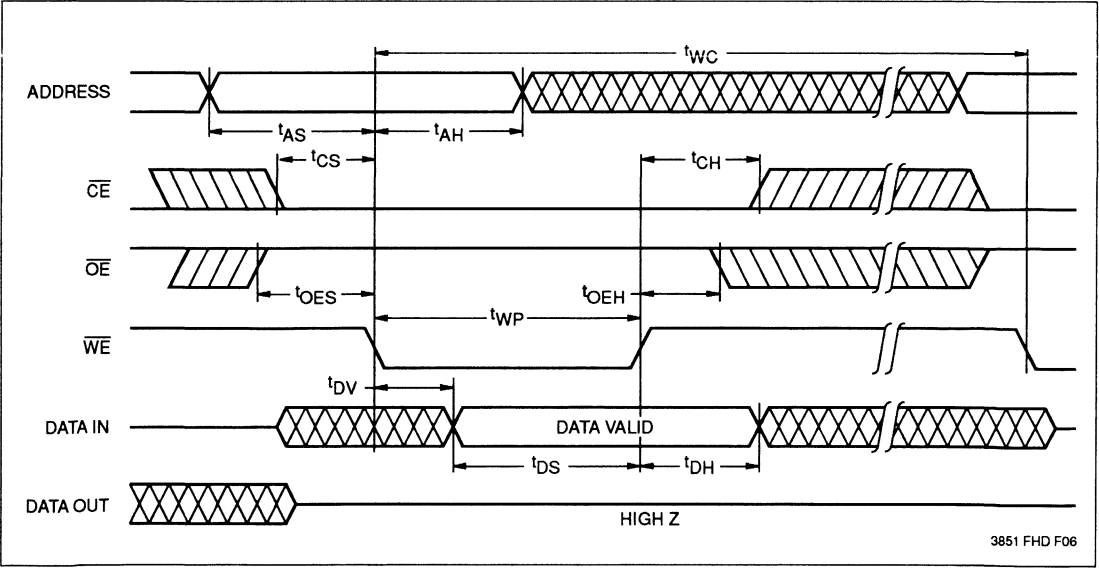
WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Typ. <sup>(1)</sup>	Max.	Units
t <sub>WC</sub> <sup>(5)</sup>	Write Cycle Time		2	5	ms
t <sub>AS</sub>	Address Setup Time	0			ns
t <sub>AH</sub>	Address Hold Time	100			ns
t <sub>CS</sub>	Write Setup Time	0			ns
t <sub>CH</sub>	Write Hold Time	0			ns
t <sub>CW</sub>	CE Pulse Width	100			ns
t <sub>OES</sub>	OE High Setup Time	10			ns
t <sub>OEH</sub>	OE High Hold Time	10			ns
t <sub>WP</sub>	WE Pulse Width	100			ns
t <sub>WPH</sub> <sup>(6)</sup>	WE High Recovery	200			ns
t <sub>DV</sub>	Data Valid			1	μs
t <sub>DS</sub>	Data Setup	50			ns
t <sub>DH</sub>	Data Hold	0			ns
t <sub>DW</sub>	Delay to Next Write	10			μs
t <sub>BLC</sub>	Byte Load Cycle	0.150		100	μs

3851 PGM T09

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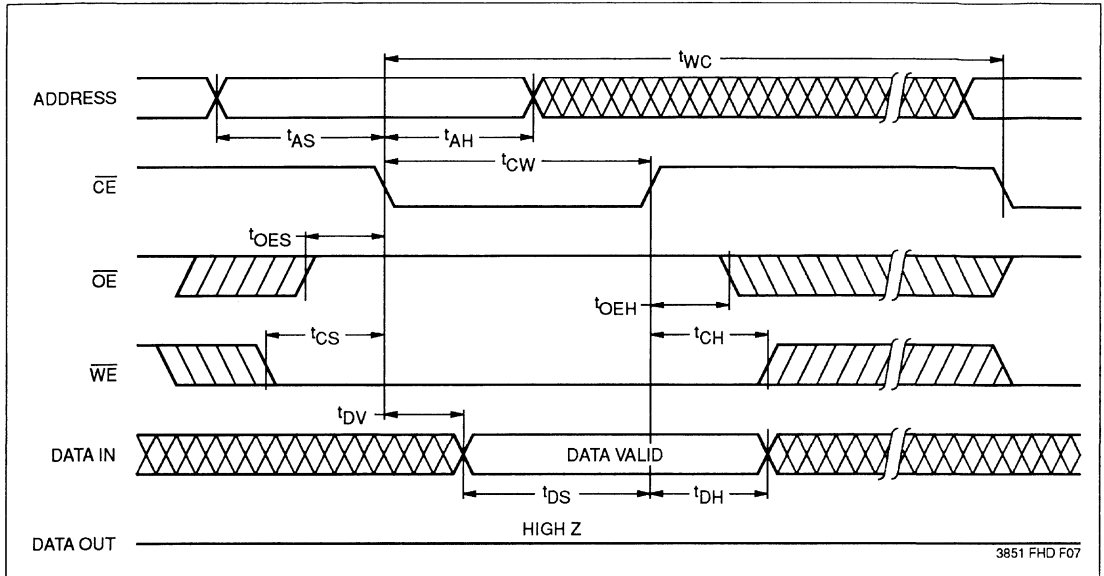
WE Controlled Write Cycle



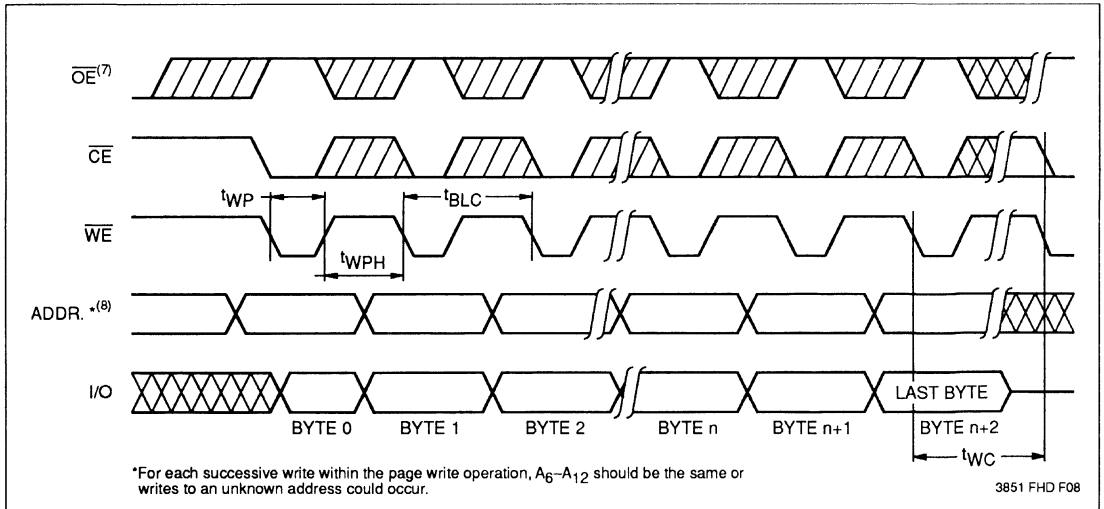
**Notes:** (5) t<sub>WC</sub> is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.  
(6) t<sub>WPH</sub> is the normal page write operation WE recovery time.

## X28C16

### $\overline{\text{CE}}$ Controlled Write Cycle



### Page Write Cycle

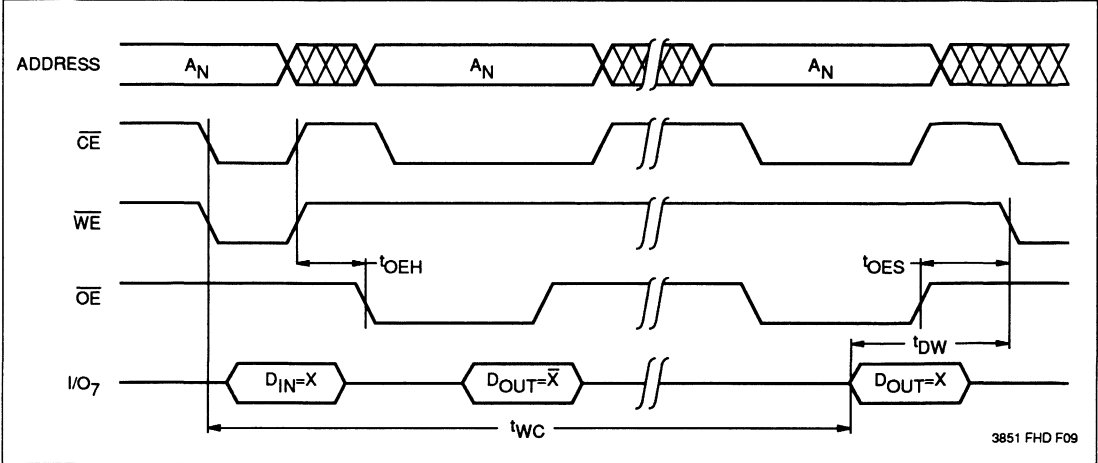


**Notes:** (7) Between successive byte writes within a page write operation,  $\overline{\text{OE}}$  can be strobed LOW: e.g. this can be done with  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  HIGH to fetch data from another memory device within the system for the next write; or with  $\overline{\text{WE}}$  HIGH and  $\overline{\text{CE}}$  LOW effectively performing a polling operation.

(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  controlled write cycle timing.

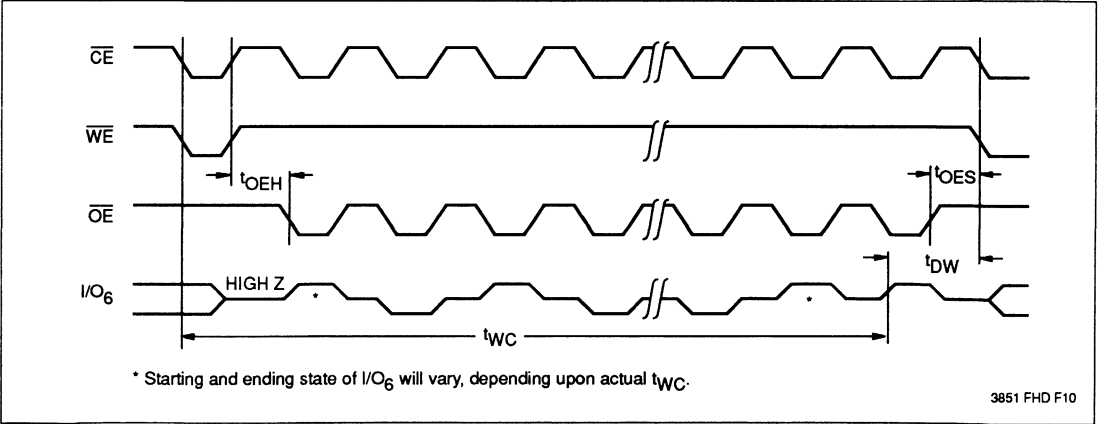
X28C16

DATA Polling Timing Diagram<sup>(9)</sup>



3

Toggle Bit Timing Diagram<sup>(9)</sup>



**Note:** (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

**X28C16**

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**NOTES**



16K

X28HC16

2K x 8 Bit

5 Volt, Byte Alterable E<sup>2</sup>PROM

## FEATURES

- 55 ns Access Time
- SIMPLE Byte and Page Write
  - Single 5 Volt Supply
  - No External High Voltages or V<sub>PP</sub> Control Circuits
  - Self Timed
  - No Erase Before Write
  - No Complex Programming Algorithms
  - No Overerase Problem
- Low Power CMOS
  - 40 mA Active Current Max.
  - 200  $\mu$ A Standby Current Max.
- Fast Write Cycle Times
  - 64-Byte Page Write Operation
  - Byte or Page Write Cycle: 2 ms Typical
  - Complete Memory Rewrite: 0.1 Sec. Typical
  - Effective Byte Write Cycle Time: 32  $\mu$ s Typical
- Software Data Protection
- End of Write Detection
  - DATA Polling
  - Toggle Bit
- High Reliability
  - Endurance: 10,000 Cycles
  - Data Retention: 100 Years
- JEDEC Approved Byte-Wide Pinout

## DESCRIPTION

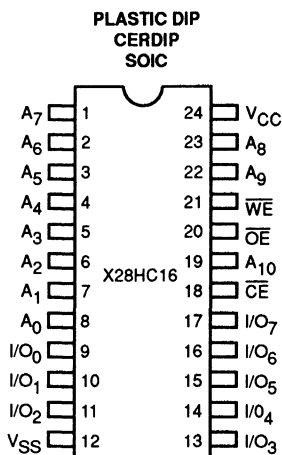
The X28HC16 is an 2K x 8 E<sup>2</sup>PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28HC16 is a 5V only device. The X28HC16 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28HC16 supports a 64-byte page write operation, effectively providing a 32  $\mu$ s/byte write cycle and enabling the entire memory to be typically written in 0.1 seconds. The X28HC16 also features DATA Polling and Toggle Bit Polling, two methods providing early end of write detection. In addition, the X28HC16 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

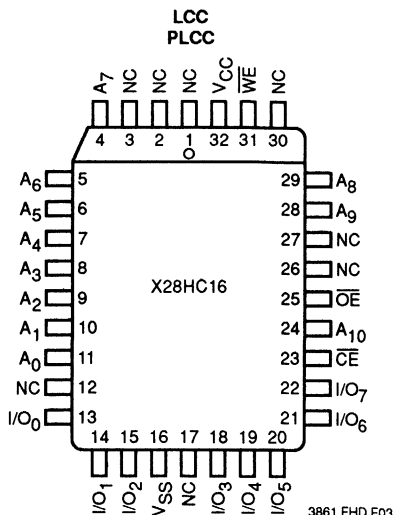
Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

3

## PIN CONFIGURATION



3861 FHD F02



3861 FHD F03



# X28HC16

## PIN DESCRIPTIONS

### Addresses (A<sub>0</sub>–A<sub>10</sub>)

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{\text{CE}}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{\text{CE}}$  is HIGH, power consumption is reduced.

### Output Enable ( $\overline{\text{OE}}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

### Data In/Data Out (I/O<sub>0</sub>–I/O<sub>7</sub>)

Data is written to or read from the X28HC16 through the I/O pins.

### Write Enable ( $\overline{\text{WE}}$ )

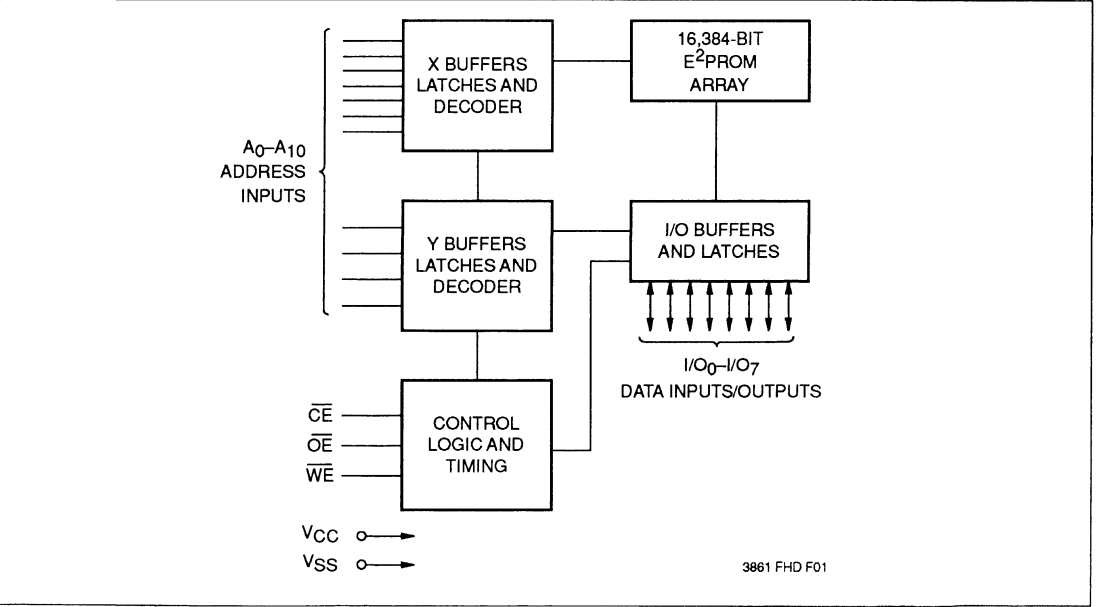
The Write Enable input controls the writing of data to the X28HC16.

## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>10</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

3861 PGM T01

## FUNCTIONAL DIAGRAM



# X28HC16

## DEVICE OPERATION

### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The X28HC16 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 2 ms.

### Page Write Operation

The page write feature of the X28HC16 allows the entire memory to be written in 0.25 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28HC16 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address ( $A_6$  through  $A_{10}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

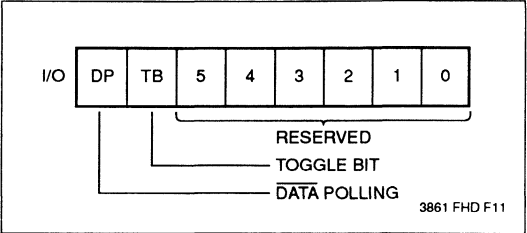
The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page

write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100  $\mu$ s.

### Write Operation Status Bits

The X28HC16 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



### DATA Polling (I/O<sub>7</sub>)

The X28HC16 features  $\overline{DATA}$  Polling as a method to indicate to the host system that the byte write or page write cycle has completed.  $\overline{DATA}$  Polling allows a simple bit test operation to determine the status of the X28HC16, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O<sub>7</sub> (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O<sub>7</sub> will reflect true data.

### Toggle Bit (I/O<sub>6</sub>)

The X28HC16 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O<sub>6</sub> will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

# X28HC16

DATA POLLING I/O,  
Figure 2. DATA Polling Bus Sequence

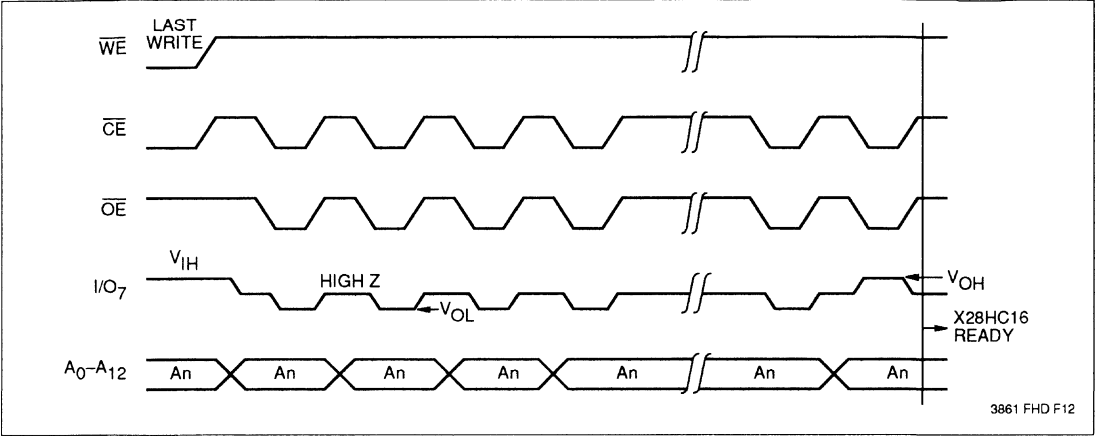
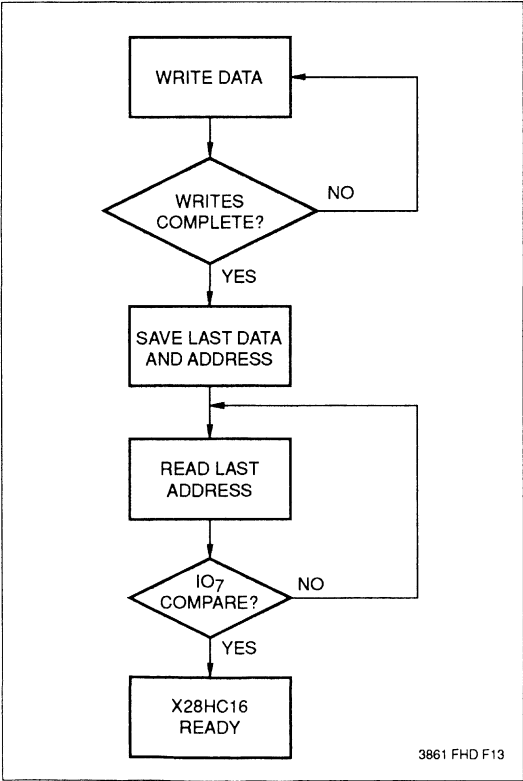


Figure 3. DATA Polling Software Flow



DATA Polling can effectively reduce the time for writing to the X28HC16. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

X28HC16

THE TOGGLE BIT I/O<sub>6</sub>  
Figure 4. Toggle Bit Bus Sequence

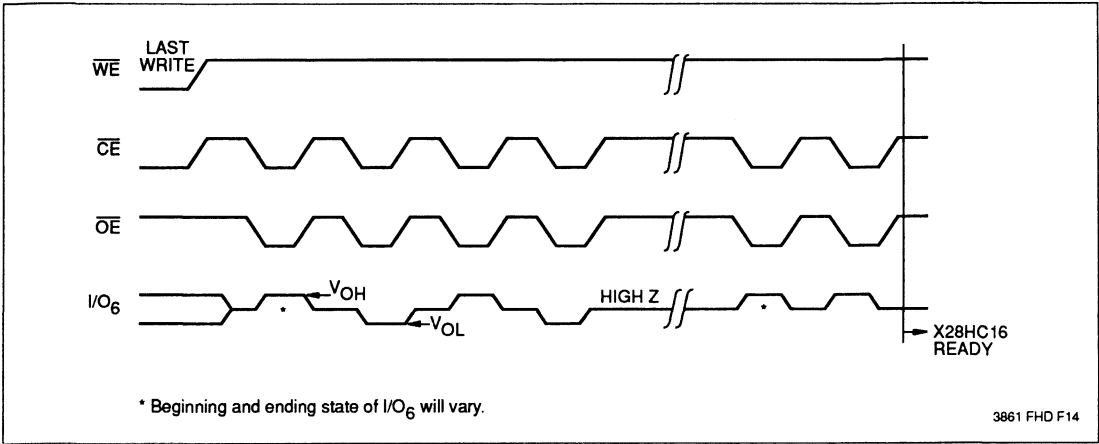
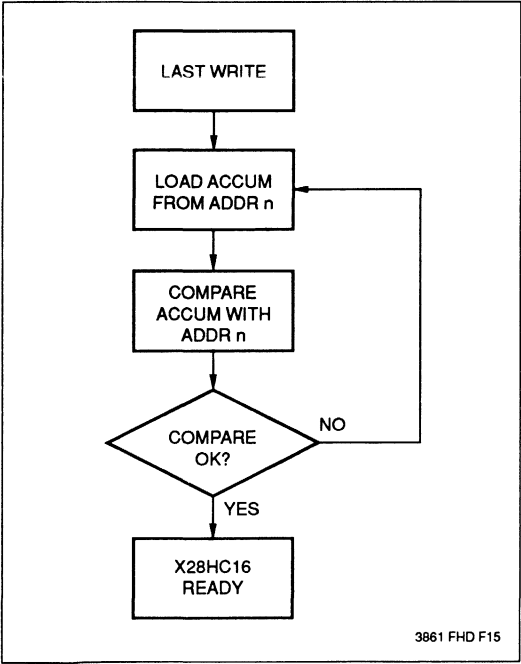


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28HC16 memories that is frequently updated. Toggle Bit testing can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

## X28HC16

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### HARDWARE DATA PROTECTION

The X28HC16 provides two hardware features that protect nonvolatile data from inadvertent writes.

- Default  $V_{CC}$  Sense—All write functions are inhibited when  $V_{CC}$  is  $\leq 3V$  typically.
- Write Inhibit—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH, or  $\overline{CE}$  HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

### SOFTWARE DATA PROTECTION

The X28HC16 offers a software controlled data protection feature. The X28HC16 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once  $V_{CC}$  was stable.

The X28HC16 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection fea-

ture. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

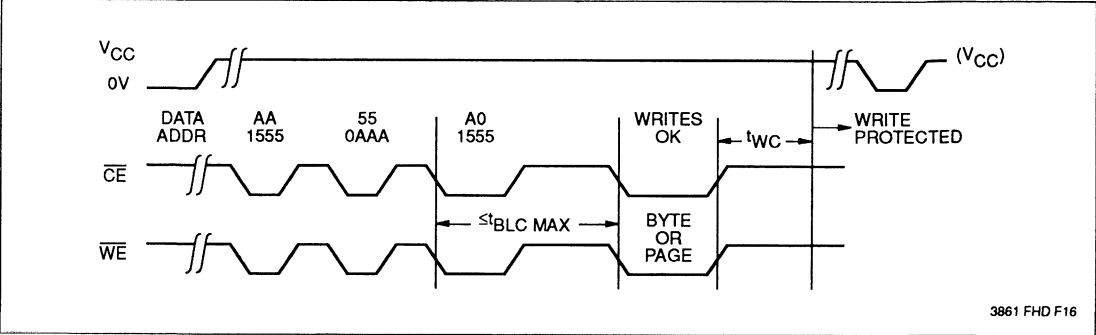
Once the software protection is enabled, the X28HC16 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

### SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

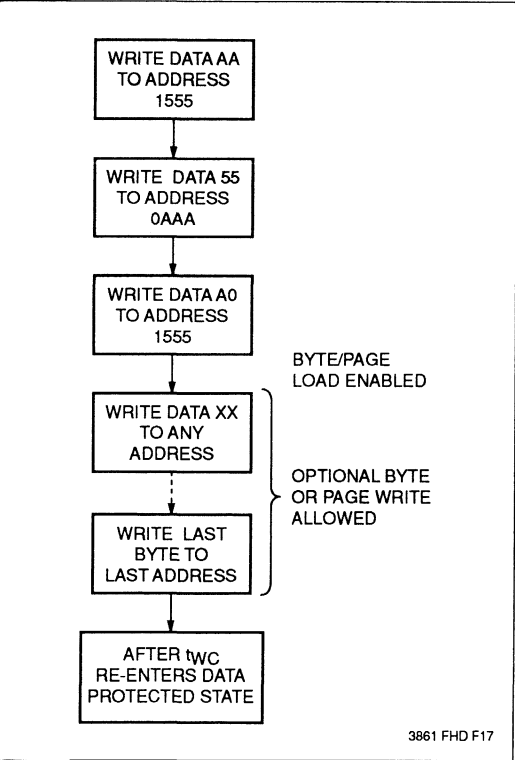
X28HC16

SOFTWARE DATA PROTECTION  
Figure 6. Timing Sequence—Byte or Page Write



3

Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used, the X28HC16 will automatically disable further writes unless another command is issued to deactivate it. If no further commands are issued the X28HC16 will be write protected during power-down and after any subsequent power-up.

*Note:* Once initiated, the sequence of write operations should not be interrupted.

# X28HC16

## RESETTING SOFTWARE DATA PROTECTION

Figure 8. Reset Software Data Protection Timing Sequence

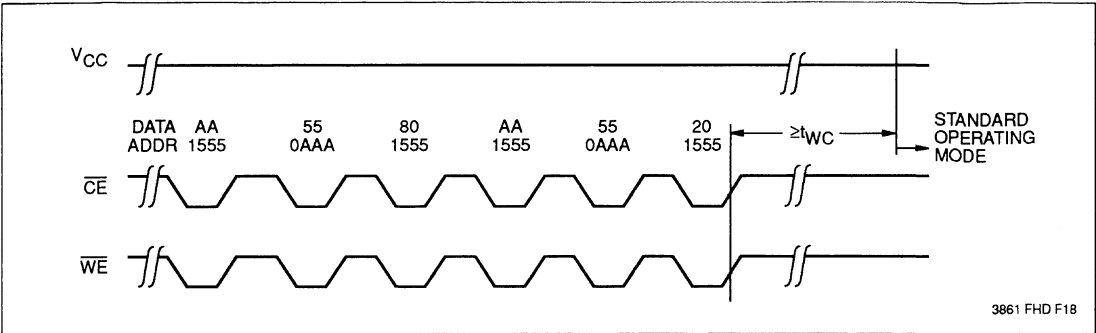
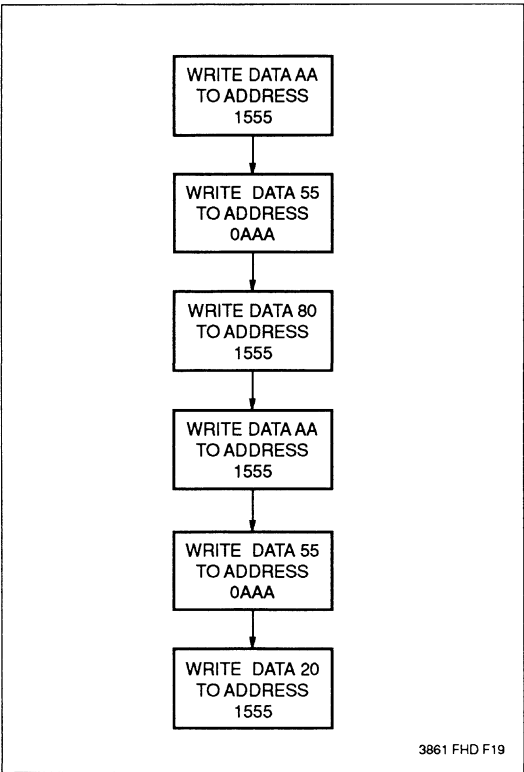


Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E<sup>2</sup>PROM programmer, the following six step algorithm will reset the internal protection circuit. After  $t_{wc}$ , the X28HC16 will be in standard operating mode.

*Note:* Once initiated, the sequence of write operations should not be interrupted.

*It should also be noted, the Reset SDP operation performs a device "program" operation; whereby all bytes are written to 00[H].*

# X28HC16

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## SYSTEM CONSIDERATIONS

Because the X28HC16 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28HC16 has two power modes, standby and active, proper decoupling of the memory array is of

prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu F$  high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7  $\mu F$  electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

3



# X28HC16

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X28HC16 .....	-10°C to +85°C
X28HC16L, X28HC16M .....	-65°C to +135°C
Storage Temperature .....	
-65°C to +150°C	
Voltage on any Pin with	
Respect to Ground .....	-1.0V to +7.0V
D.C. Output Current .....	5 mA
Lead Temperature	
(Soldering, 10 Seconds) .....	300°C

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

3861 PGM T02

Supply Voltage	Limits
X28HC16	5V ± 10%

3861 PGM T03

## D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Current (Active) (TTL Inputs)		15	40	mA	$\overline{CE} = \overline{OE} = V_{IL}$ , $\overline{WE} = V_{IH}$ , All I/O's = Open, Address Inputs = TTL Levels @ f = 10 MHz
I <sub>SB1</sub>	V <sub>CC</sub> Current (Standby) (TTL Inputs)		1	2	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V <sub>IH</sub>
I <sub>SB2</sub>	V <sub>CC</sub> Current (Standby) (CMOS Inputs)		100	200	μA	$\overline{CE} = V_{CC} - 0.3V$ , $\overline{OE} = GND$ All I/O's = Open, Other Inputs = V <sub>CC</sub> - 0.3V
I <sub>LI</sub>	Input Leakage Current			±10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current			±10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , $\overline{CE} = V_{IH}$
V <sub>IL</sub> (2)	Input Low Voltage	-1.0		0.8	V	
V <sub>IH</sub> (2)	Input High Voltage	2.0		V <sub>CC</sub> + 1.0	V	
V <sub>OL</sub>	Output Low Voltage			0.4	V	I <sub>OL</sub> = 5 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = -5 mA

3861 PGM T04

Notes: (1) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage  
(2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.

X28HC16

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Unit
Minimum Endurance	10,000		Cycles/Byte
Data Retention	100		Years

3861 PGM T05

POWER-UP TIMING

Symbol	Parameter	Typ. (1)	Units
tPUR(3)	Power-up to Read Operation	100	μs
tPUW(3)	Power-up to Write Operation	5	ms

3861 PGM T06

CAPACITANCE TA = 25°C, f = 1.0 MHz, VCC = 5V

Symbol	Parameter	Max.	Units	Test Conditions
CIO(3)	Input/Output Capacitance	10	pF	VIO = 0V
CIN(3)	Input Capacitance	6	pF	VIN = 0V

3861 PGM T07

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	1.5V

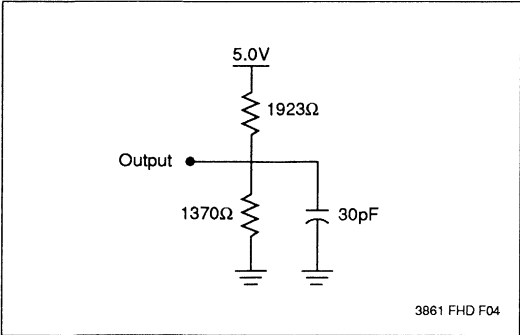
3861 PGM T08

MODE SELECTION

CE	OE	WE	Mode	I/O	Power
L	L	H	Read	DO <sub>OUT</sub>	Active
L	H	L	Write	DI <sub>IN</sub>	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3861 PGM T09

EQUIVALENT A.C. LOAD CIRCUITS



**Note:** (3) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

# X28HC16

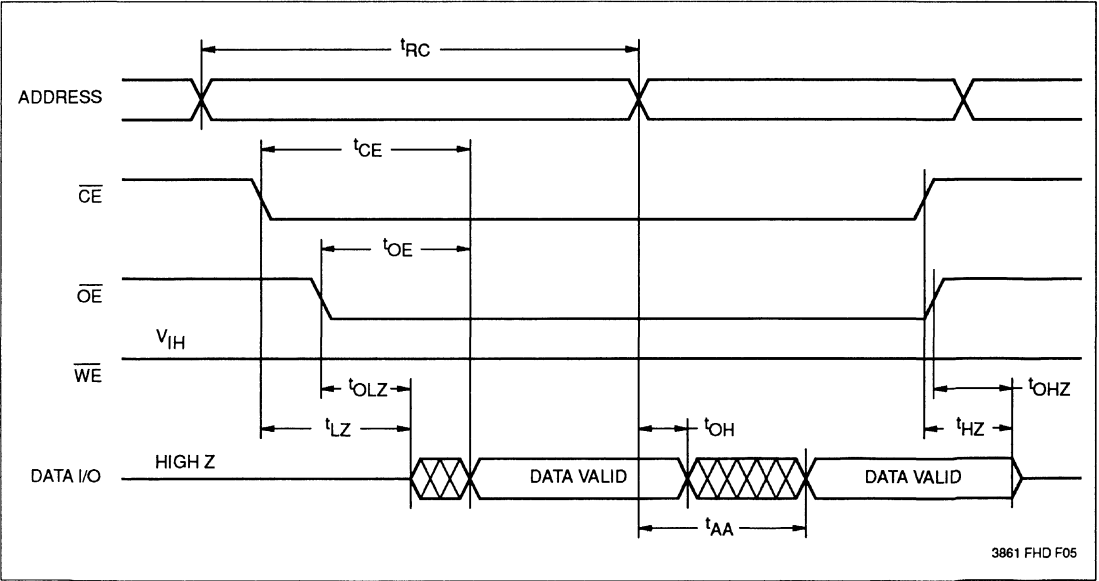
## A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

### Read Cycle Limits

Symbol	Parameter	X28HC16-55		X28HC16-70		X28HC16-90		X28HC16-12		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	55		70		90		120		ns
$t_{CE}$	Chip Enable Access Time		55		70		90		120	ns
$t_{AA}$	Address Access Time		55		70		90		120	ns
$t_{OE}$	Output Enable Access Time		30		35		40		50	ns
$t_{LZ}^{(4)}$	$\overline{CE}$ Low to Active Output	0		0		0		0		ns
$t_{OLZ}^{(4)}$	$\overline{OE}$ Low to Active Output	0		0		0		0		ns
$t_{HZ}^{(4)}$	$\overline{CE}$ High to High Z Output		30	0	30		30		30	ns
$t_{OHZ}^{(4)}$	$\overline{OE}$ High to High Z Output		30	0	30		30		30	ns
$t_{OH}$	Output Hold from Address Change	0		0		0		0		ns

3856 PGM T10

### Read Cycle



3861 FHD F05

**Notes:** (4)  $t_{LZ}$  min.,  $t_{HZ}$ ,  $t_{OLZ}$  min., and  $t_{OHZ}$  are periodically sampled and not 100%.  $t_{HZ}$  max. and  $t_{OHZ}$  max. are measured from the point when  $\overline{CE}$  or  $\overline{OE}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

X28HC16

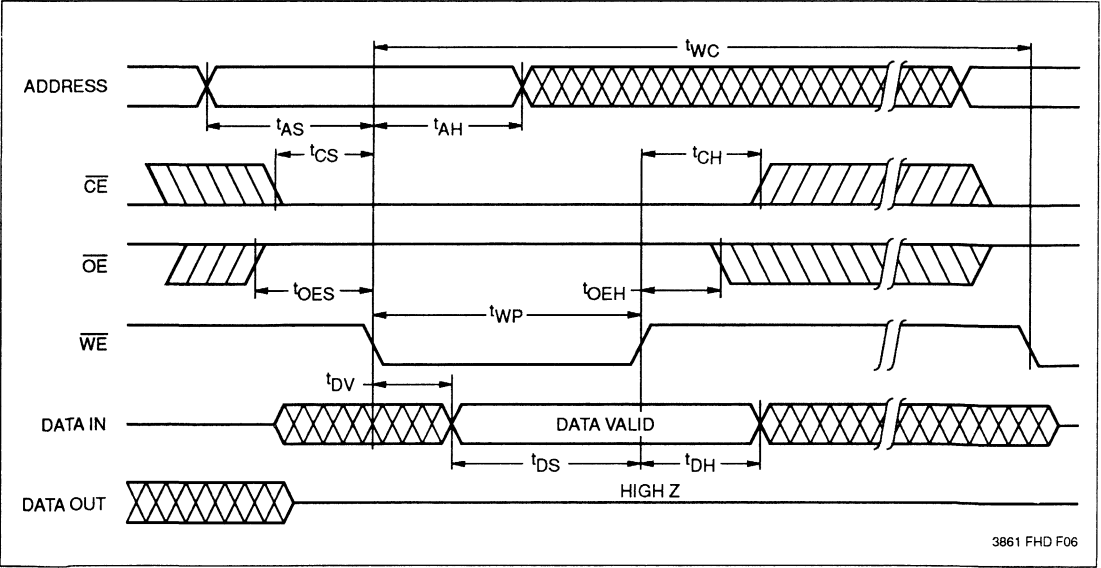
WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Typ. <sup>(1)</sup>	Max.	Units
t <sub>WC</sub> <sup>(5)</sup>	Write Cycle Time		2	5	ms
t <sub>AS</sub>	Address Setup Time	0			ns
t <sub>AH</sub>	Address Hold Time	50			ns
t <sub>CS</sub>	Write Setup Time	0			ns
t <sub>CH</sub>	Write Hold Time	0			ns
t <sub>CW</sub>	CE Pulse Width	50			ns
t <sub>OES</sub>	OE High Setup Time	0			ns
t <sub>OEH</sub>	OE High Hold Time	0			ns
t <sub>WP</sub>	WE Pulse Width	50			ns
t <sub>WPH</sub> <sup>(6)</sup>	WE High Recovery	50			ns
t <sub>DV</sub> <sup>(6)</sup>	Data Valid			1	μs
t <sub>DS</sub>	Data Setup	50			ns
t <sub>DH</sub>	Data Hold	0			ns
t <sub>DW</sub> <sup>(6)</sup>	Delay to Next Write	10			μs
t <sub>BLC</sub>	Byte Load Cycle	0.150		100	μs

3861 PGM T11

3

WE Controlled Write Cycle

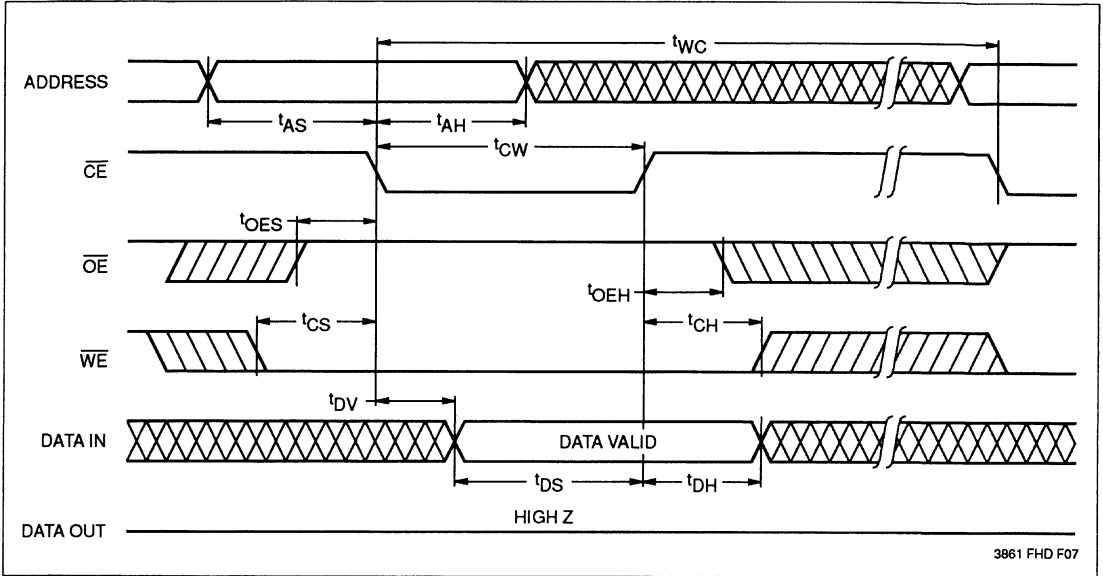


3861 FHD F06

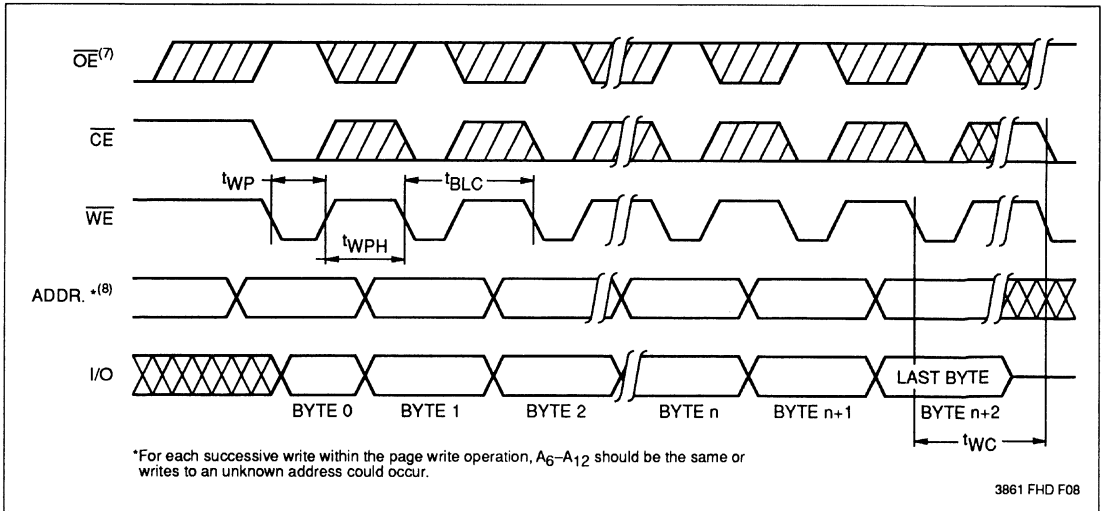
Notes: (5) t<sub>WC</sub> is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.  
(6) t<sub>WPH</sub> and t<sub>DW</sub> are periodically sampled and not 100% tested.

## X28HC16

### $\overline{\text{CE}}$ Controlled Write Cycle



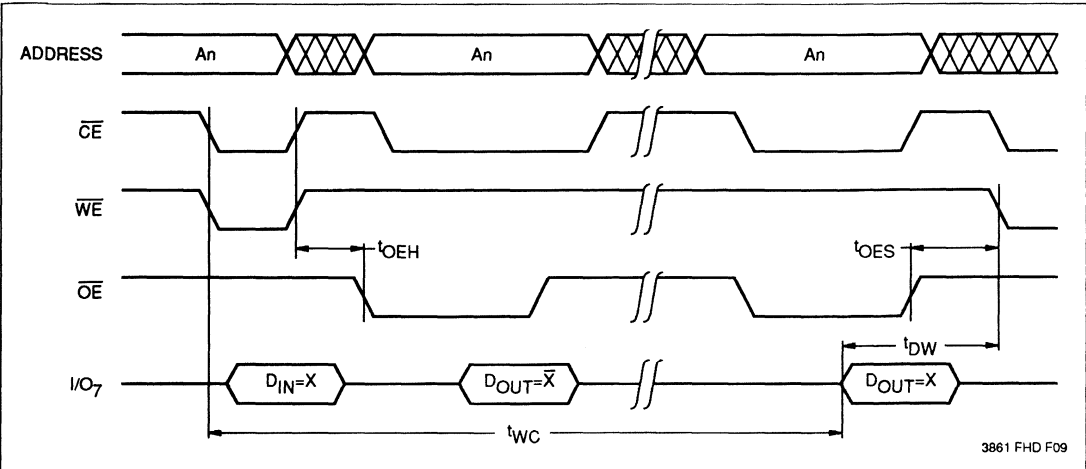
### Page Write Cycle



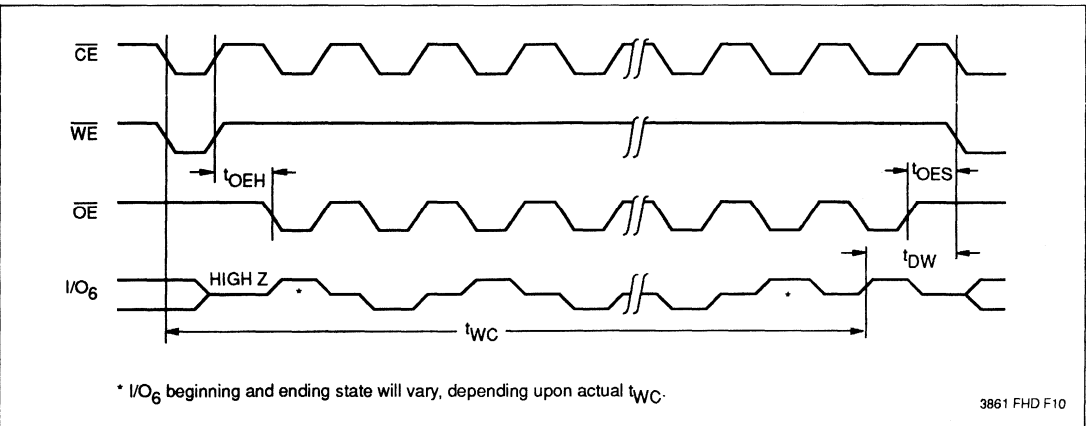
- Notes:** (7) Between successive byte writes within a page write operation,  $\overline{\text{OE}}$  can be strobed LOW: e.g. this can be done with  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  HIGH to fetch data from another memory device within the system for the next write; or with  $\overline{\text{WE}}$  HIGH and  $\overline{\text{CE}}$  LOW effectively performing a polling operation.
- (8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  controlled write cycle timing.

# X28HC16

**DATA Polling Timing Diagram<sup>(9)</sup>**



**Toggle Bit Timing Diagram<sup>(9)</sup>**



**Note:** (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

## X28HC16

### DEVICE OPERATION

#### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

#### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The X28HC16 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 2 ms.

#### Page Write Operation

The page write feature of the X28HC16 allows the entire memory to be written in 0.25 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28HC16 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address ( $A_6$  through  $A_{10}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

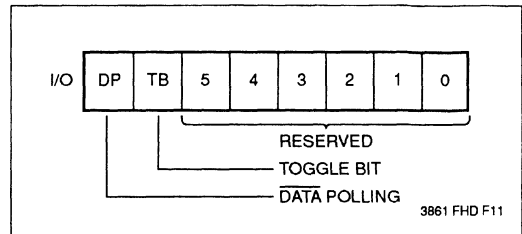
The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page

write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100  $\mu$ s.

#### Write Operation Status Bits

The X28HC16 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



#### DATA Polling ( $I/O_7$ )

The X28HC16 features  $\overline{DATA}$  Polling as a method to indicate to the host system that the byte write or page write cycle has completed.  $\overline{DATA}$  Polling allows a simple bit test operation to determine the status of the X28HC16, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on  $I/O_7$  (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete,  $I/O_7$  will reflect true data.

#### Toggle Bit ( $I/O_6$ )

The X28HC16 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle  $I/O_6$  will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

64K

X28C64

8K x 8 Bit

## 5 Volt, Byte Alterable E<sup>2</sup>PROM

### FEATURES

- 150 ns Access Time
- SIMPLE Byte and Page Write
  - Single 5 Volt Supply
  - No External High Voltages or  $V_{PP}$  Control Circuits
  - Self Timed
  - No Erase Before Write
  - No Complex Programming Algorithms
  - No Overerase Problem
- Low Power CMOS
  - 60 mA Active Current Max.
  - 200  $\mu$ A Standby Current Max.
- Fast Write Cycle Times
  - 64-Byte Page Write Operation
  - Byte or Page Write Cycle: 5 ms Typical
  - Complete Memory Rewrite: 0.625 Sec. Typical
  - Effective Byte Write Cycle Time: 78  $\mu$ s Typical
- Software Data Protection
- End of Write Detection
  - DATA Polling
  - Toggle Bit
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 100 Years
- JEDEC Approved Byte-Wide Pinout

### DESCRIPTION

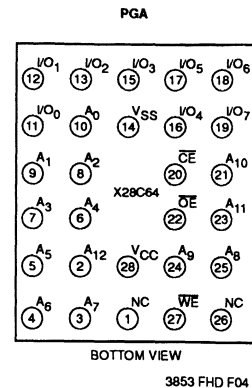
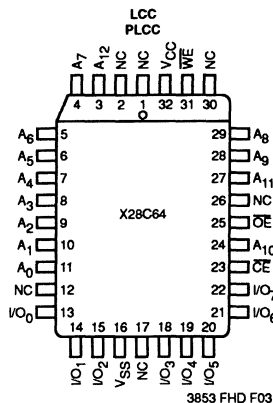
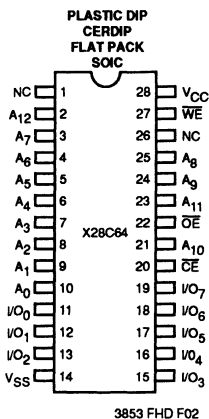
The X28C64 is an 8K x 8 E<sup>2</sup>PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C64 is a 5V only device. The X28C64 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C64 supports a 64-byte page write operation, effectively providing a 78  $\mu$ s/byte write cycle and enabling the entire memory to be typically written in 0.625 seconds. The X28C64 also features  $\overline{\text{DATA}}$  and Toggle Bit Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C64 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

3

### PIN CONFIGURATION





# X28C64

## PIN DESCRIPTIONS

### Addresses ( $A_0$ – $A_{12}$ )

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{CE}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH, power consumption is reduced.

### Output Enable ( $\overline{OE}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

### Data In/Data Out ( $I/O_0$ – $I/O_7$ )

Data is written to or read from the X28C64 through the I/O pins.

### Write Enable ( $\overline{WE}$ )

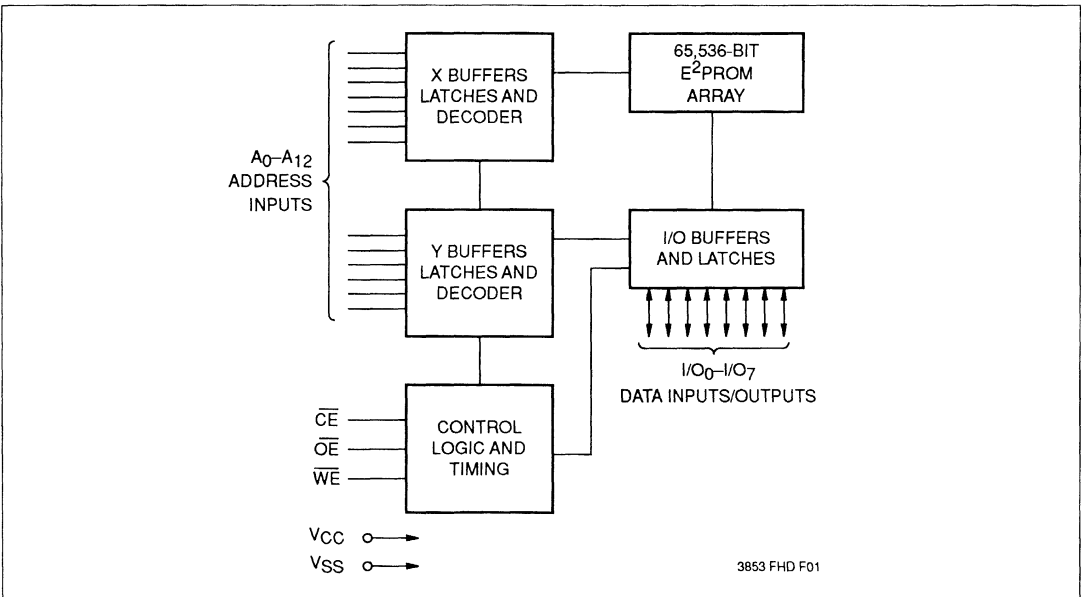
The Write Enable input controls the writing of data to the X28C64.

## PIN NAMES

Symbol	Description
$A_0$ – $A_{12}$	Address Inputs
$I/O_0$ – $I/O_7$	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$V_{CC}$	+5V
$V_{SS}$	Ground
NC	No Connect

3853 PGM T01

## FUNCTIONAL DIAGRAM



# X28C64

## DEVICE OPERATION

### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The X28C64 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

### Page Write Operation

The page write feature of the X28C64 allows the entire memory to be written in 0.625 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C64 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address ( $A_6$  through  $A_{12}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

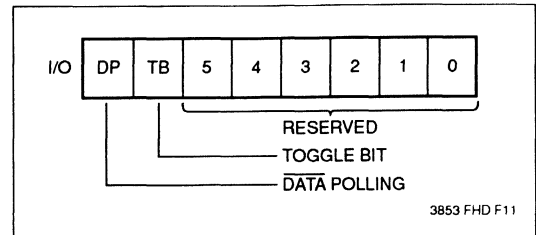
The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host

continues to access the device within the byte load cycle time of 100  $\mu$ s.

### Write Operation Status Bits

The X28C64 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



### DATA Polling (I/O<sub>7</sub>)

The X28C64 features  $\overline{DATA}$  Polling as a method to indicate to the host system that the byte write or page write cycle has completed.  $\overline{DATA}$  Polling allows a simple bit test operation to determine the status of the X28C64, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O<sub>7</sub> (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O<sub>7</sub> will reflect true data. Note: If the X28C64 is in the protected state and an illegal write operation is attempted  $\overline{DATA}$  Polling will not operate.

### Toggle Bit (I/O<sub>6</sub>)

The X28C64 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O<sub>6</sub> will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

# X28C64

## DATA Polling I/O<sub>7</sub>

Figure 2. DATA Polling Bus Sequence

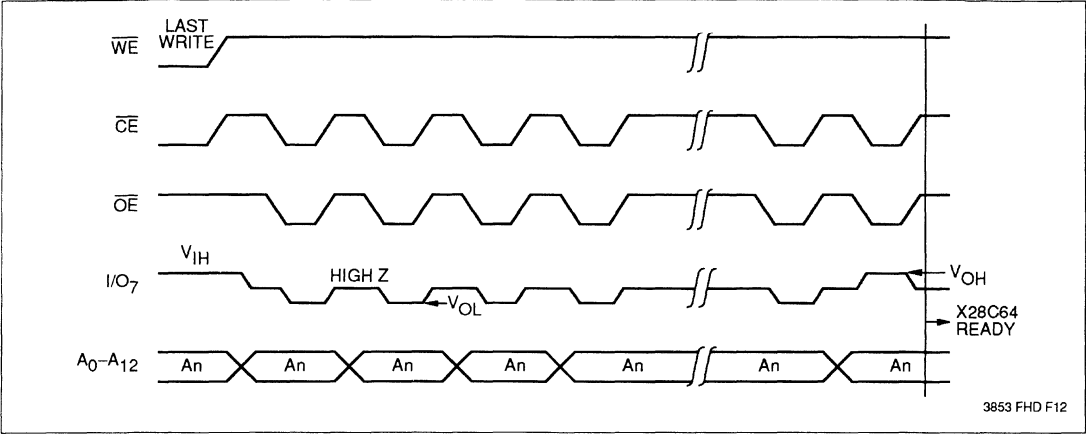
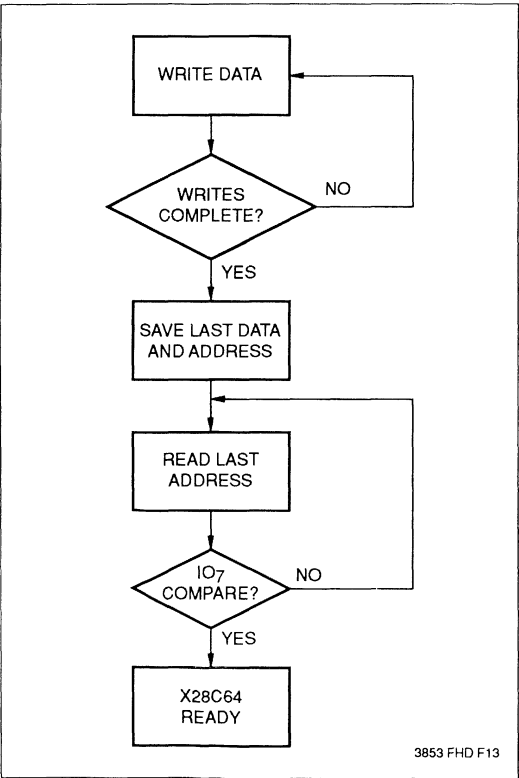


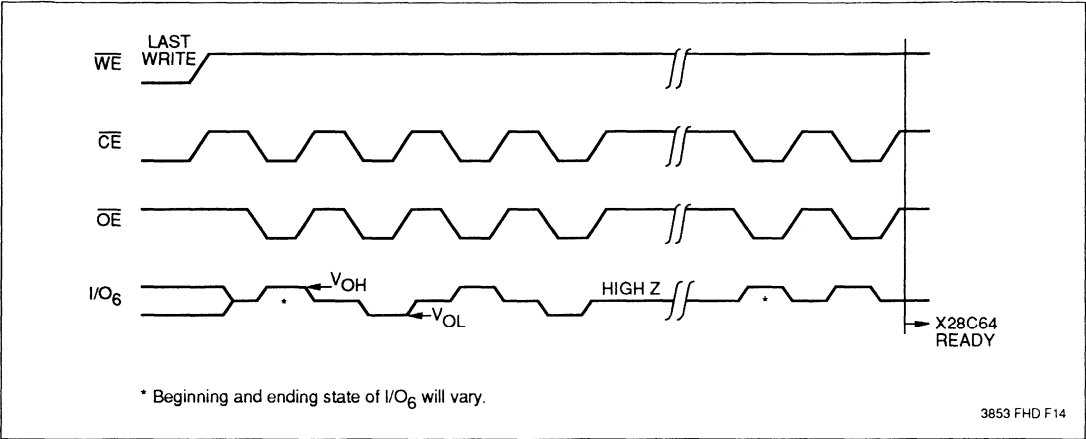
Figure 3. DATA Polling Software Flow



DATA Polling can effectively halve the time for writing to the X28C64. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

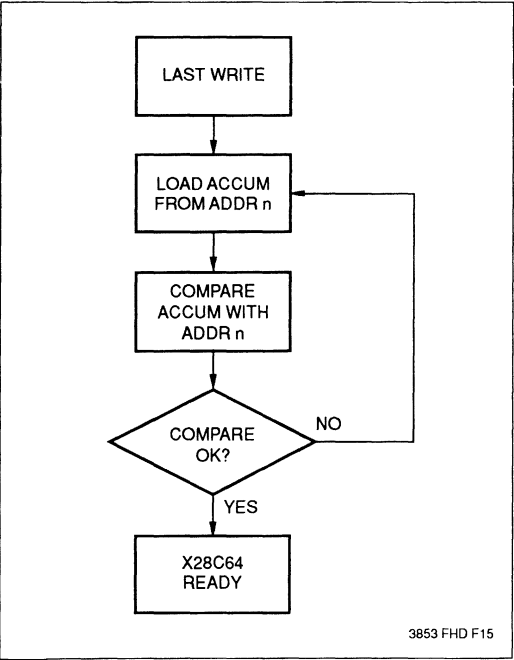
**X28C64**

**The Toggle Bit I/O<sub>6</sub>**  
**Figure 4. Toggle Bit Bus Sequence**



**3**

**Figure 5. Toggle Bit Software Flow**



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28C64 memories that is frequently updated. Toggle Bit testing can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

### HARDWARE DATA PROTECTION

The X28C64 provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A  $\overline{WE}$  pulse typically less than 20 ns will not initiate a write cycle.
- Default  $V_{CC}$  Sense—All write functions are inhibited when  $V_{CC}$  is  $\leq 3V$  typically.
- Write Inhibit—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH, or  $\overline{CE}$  HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

### SOFTWARE DATA PROTECTION

The X28C64 offers a software controlled data protection feature. The X28C64 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once  $V_{CC}$  was stable.

The X28C64 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C64 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

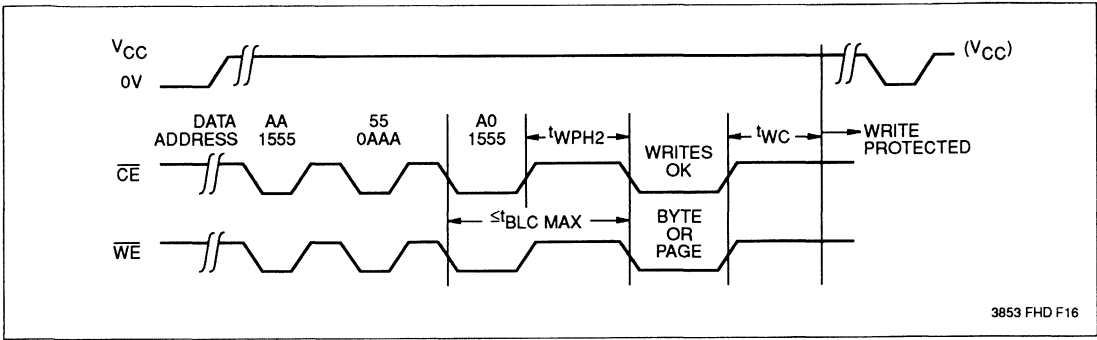
### SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data\*. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

*Note: \*Once the three byte sequence is issued it must be followed by a valid byte or page write operation.*

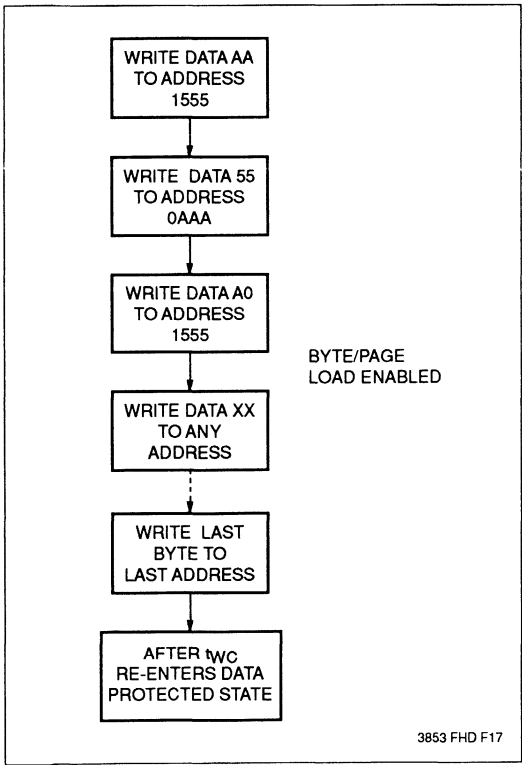
X28C64

Software Data Protection  
Figure 6. Timing Sequence—Byte or Page Write



3

Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C64 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C64 will be write protected during power-down and after any subsequent power-up.

*Note: Once initiated, the sequence of write operations should not be interrupted.*

# X28C64

Resetting Software Data Protection  
Figure 8. Reset Software Data Protection Timing Sequence

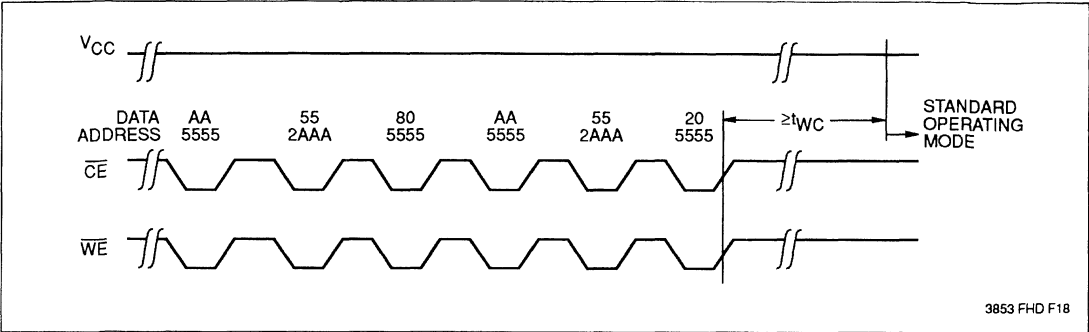
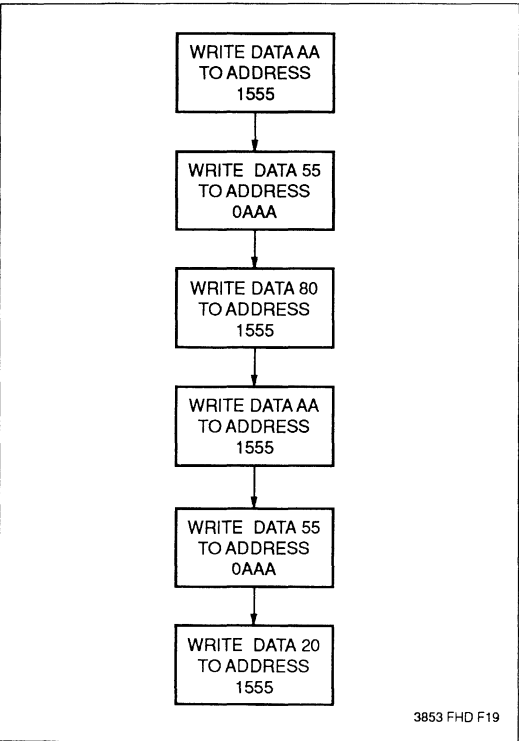


Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E<sup>2</sup>PROM programmer, the following six step algorithm will reset the internal protection circuit. After  $t_{WC}$ , the X28C64 will be in standard operating mode.

*Note: Once initiated, the sequence of write operations should not be interrupted.*

*It should also be noted, the Reset SDP operation performs a device "program" operation; whereby all bytes are written to 00[H].*

## X28C64

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### SYSTEM CONSIDERATIONS

Because the X28C64 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C64 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu\text{F}$  high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7  $\mu\text{F}$  electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.



# X28C64

### ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X28C64	−10°C to +85°C
X28C64I, X28C64M	−65°C to +135°C
Storage Temperature	−65°C to +150°C
Voltage on any Pin with	
Respect to Ground	−1.0V to +7.0V
D.C. Output Current	5 mA
Lead Temperature	
(Soldering, 10 Seconds)	300°C

### \*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

Supply Voltage	Limits
X28C64	5V ± 10%

### D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Current (Active) (TTL Inputs)		30	60	mA	$\overline{CE} = \overline{OE} = V_{IL}$ , $\overline{WE} = V_{IH}$ , All I/O's = Open, Address Inputs = 0.4V/2.4V Levels @ f = 5MHz
I <sub>SB1</sub>	V <sub>CC</sub> Current (Standby) (TTL Inputs)		1	2	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V <sub>IH</sub>
I <sub>SB2</sub>	V <sub>CC</sub> Current (Standby) (CMOS Inputs)		100	200	μA	$\overline{CE} = \overline{WE} = V_{CC} - 0.3V$ All I/O's = Open, Other Inputs = Don't Care
I <sub>LI</sub>	Input Leakage Current			10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current			10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , $\overline{CE} = V_{IH}$
V <sub>IL</sub> (2)	Input Low Voltage	−1.0		0.8	V	
V <sub>IH</sub> (2)	Input High Voltage	2.0		V <sub>CC</sub> + 1.0	V	
V <sub>OL</sub>	Output Low Voltage			0.4	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = −400 μA

3853 PGM T02

Notes: (1) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage and are not tested.  
(2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.

X28C64

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Minimum Endurance	100,000	Cycles/Byte
Data Retention	100	Years

3853 PGM T03

POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
tPUR(3)	Power-up to Read Operation	100	μs
tPUW(3)	Power-up to Write Operation	5	ms

3853 PGM T04

CAPACITANCE TA = 25°C, f = 1.0 MHz, VCC = 5V

Symbol	Parameter	Max.	Units	Test Conditions
CIO(3)	Input/Output Capacitance	10	pF	VIO = 0V
CIN(3)	Input Capacitance	6	pF	VIN = 0V

3853 PGM T05

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V

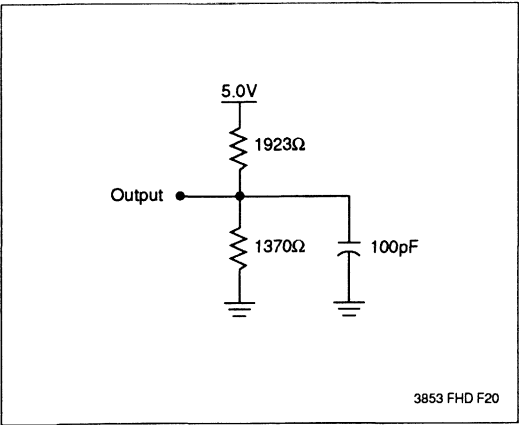
3853 PGM T06

MODE SELECTION

CE	OE	WE	Mode	I/O	Power
L	L	H	Read	DOUT	Active
L	H	L	Write	DIN	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3853 PGM T07

EQUIVALENT A.C. LOAD CIRCUIT



3853 FHD F20

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (3) This parameter is periodically sampled and not 100% tested.

# X28C64

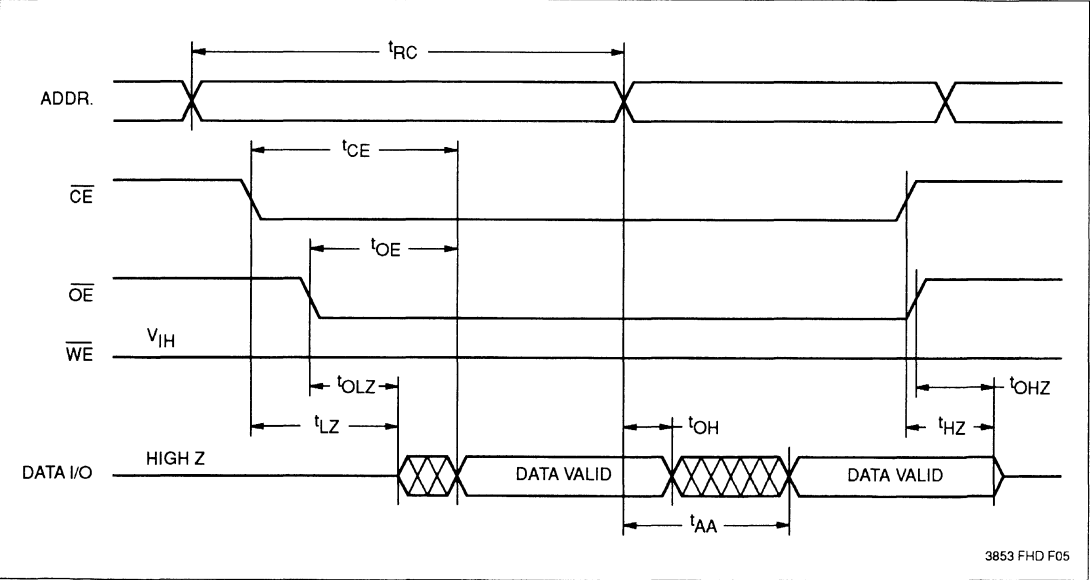
## A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified.)

### Read Cycle Limits

Symbol	Parameter	X28C64-15		X28C64-20		X28C64-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	150		200		250		ns
$t_{CE}$	Chip Enable Access Time		150		200		250	ns
$t_{AA}$	Address Access Time		150		200		250	ns
$t_{OE}$	Output Enable Access Time		70		80		100	ns
$t_{LZ}^{(4)}$	CE Low to Active Output	0		0		0		ns
$t_{OLZ}^{(4)}$	OE Low to Active Output	0		0		0		ns
$t_{HZ}^{(4)}$	CE High to High Z Output		50		50		50	ns
$t_{OHZ}^{(4)}$	OE High to High Z Output		50		50		50	ns
$t_{OH}$	Output Hold from Address Change	0		0		0		ns

3856 PGM T08

### Read Cycle



3853 FHD F05

**Notes:** (4)  $t_{LZ}$  min.,  $t_{HZ}$ ,  $t_{OLZ}$  min., and  $t_{OHZ}$  are periodically sampled and not 100% tested.  $t_{HZ}$  max. and  $t_{OHZ}$  max. are measured, with  $C_L = 5pF$ , from the point when  $\overline{CE}$  or  $\overline{OE}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

X28C64

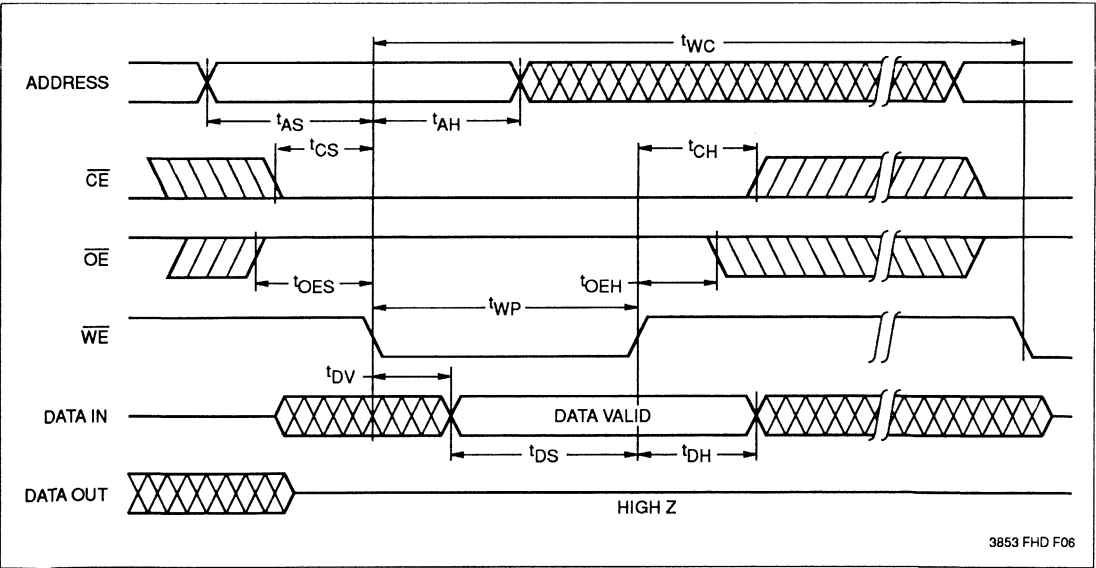
3

WRITE CYCLE LIMITS

Symbol	Parameter	Min. <sup>(7)</sup>	Typ. <sup>(1)</sup>	Max.	Units
t <sub>WC</sub> <sup>(5)</sup>	Write Cycle Time		5	10	ms
t <sub>AS</sub>	Address Setup Time	0			ns
t <sub>AH</sub>	Address Hold Time	100			ns
t <sub>CS</sub>	Write Setup Time	0			ns
t <sub>CH</sub>	Write Hold Time	0			ns
t <sub>CW</sub>	CE Pulse Width	100			ns
t <sub>OES</sub>	OE High Setup Time	10			ns
t <sub>OEH</sub>	OE High Hold Time	10			ns
t <sub>WP</sub>	WE Pulse Width	100			ns
t <sub>WPH</sub>	WE High Recovery	200			ns
t <sub>WPH2</sub> <sup>(6)</sup>	SDP We Recovery	1			μs
t <sub>DV</sub>	Data Valid			1	μs
t <sub>DS</sub>	Data Setup	50			ns
t <sub>DH</sub>	Data Hold	10			ns
t <sub>DW</sub>	Delay to Next Write	10			μs
t <sub>BLC</sub> <sup>(7)</sup>	Byte Load Cycle	1		100	μs

3853 PGM T09

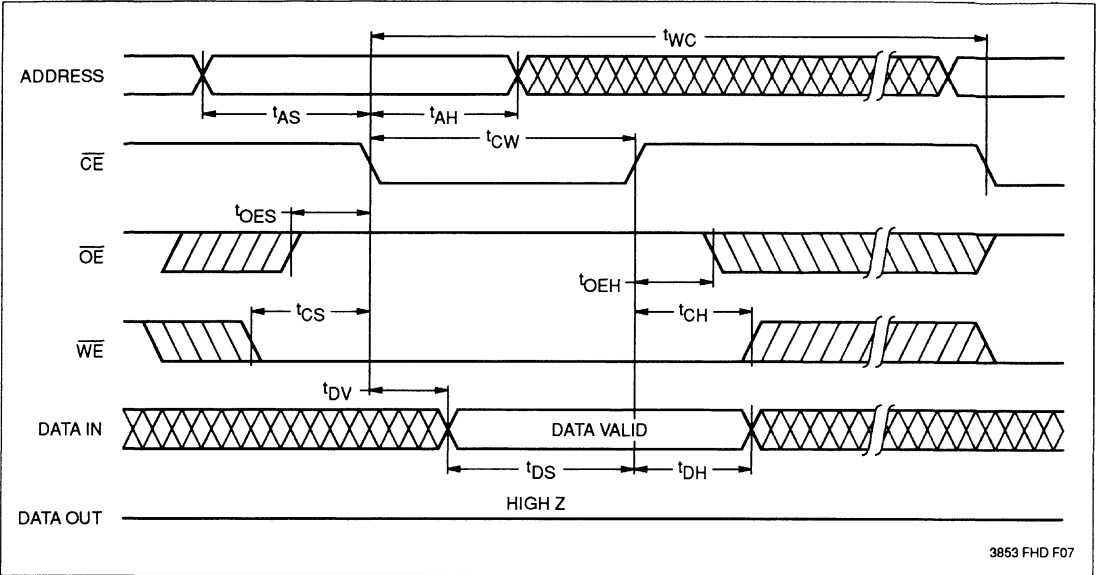
WE Controlled Write Cycle



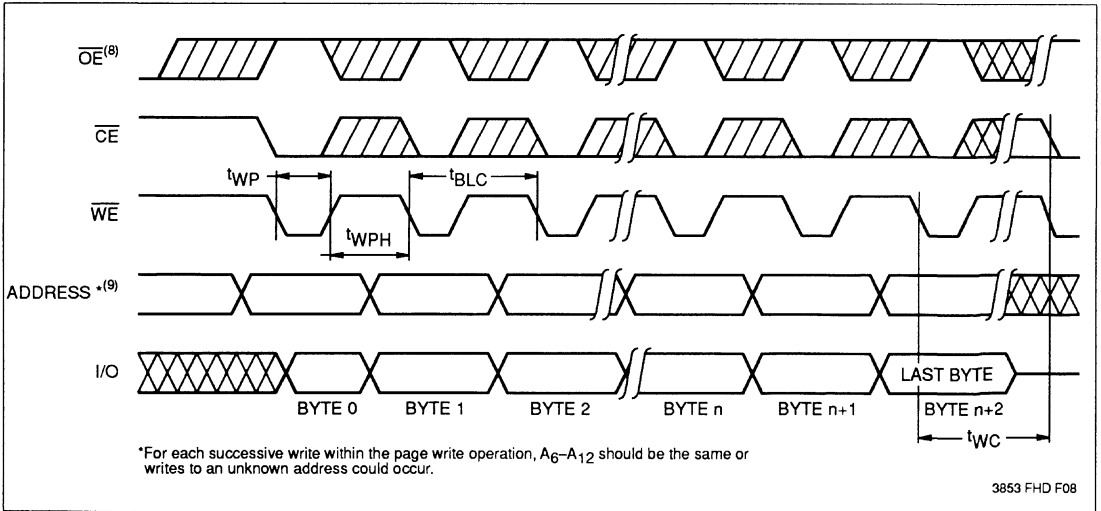
- Notes:** (5)  $t_{WC}$  is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.
- (6)  $t_{WPH}$  is the normal page write operation WE recovery time.  $t_{WPH2}$  is the WE recovery time needed only after the end of issuing the three byte SDP command sequence and before writing the first byte of data to the array. Refer to Figure 6 which illustrates the  $t_{WPH2}$  requirement.
- (7) For Faster  $t_{WC}$  and  $t_{BLC}$  times, refer to X28HC64.

# X28C64

## $\overline{\text{CE}}$ Controlled Write Cycle



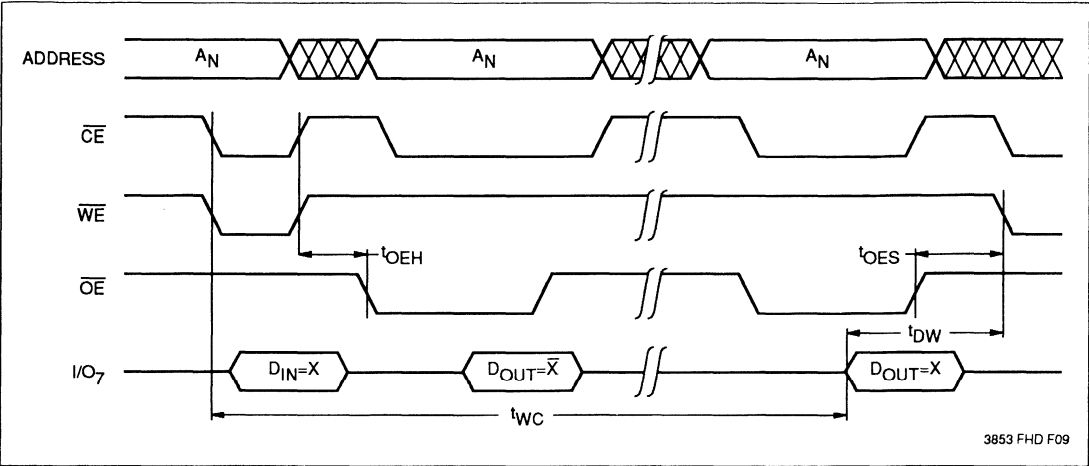
## Page Write Cycle



- Notes:** (8) Between successive byte writes within a page write operation,  $\overline{\text{OE}}$  can be strobed LOW: e.g. this can be done with  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  HIGH to fetch data from another memory device within the system for the next write; or with  $\overline{\text{WE}}$  HIGH and  $\overline{\text{CE}}$  LOW effectively performing a polling operation.
- (9) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  controlled write cycle timing.

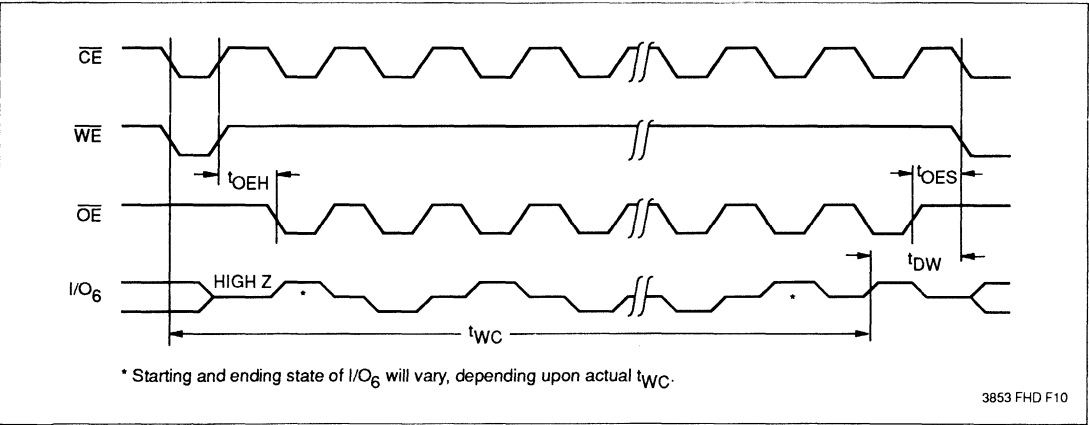
X28C64

DATA Polling Timing Diagram<sup>(10)</sup>



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Toggle Bit Timing Diagram<sup>(10)</sup>



**Note:** (10) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

X28C64

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NOTES



64K

X28HC64

8K x 8 Bit

## 5 Volt, Byte Alterable E<sup>2</sup>PROM

### FEATURES

- 55 ns Access Time
- SIMPLE Byte and Page Write
  - Single 5 Volt Supply
  - No External High Voltages or V<sub>PP</sub> Control Circuits
  - Self Timed
  - No Erase Before Write
  - No Complex Programming Algorithms
  - No Overerase Problem
- Low Power CMOS
  - 40 mA Active Current Max.
  - 200  $\mu$ A Standby Current Max.
- Fast Write Cycle Times
  - 64-Byte Page Write Operation
  - Byte or Page Write Cycle: 2 ms Typical
  - Complete Memory Rewrite: 0.25 Sec. Typical
  - Effective Byte Write Cycle Time: 32  $\mu$ s Typical
- Software Data Protection
- End of Write Detection
  - DATA Polling
  - Toggle Bit
- High Reliability
  - Endurance: 10,000 Cycles
  - Data Retention: 100 Years
- JEDEC Approved Byte-Wide Pinout

### DESCRIPTION

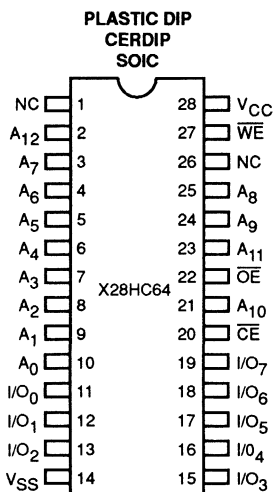
The X28HC64 is an 8K x 8 E<sup>2</sup>PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28HC64 is a 5V only device. The X28HC64 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28HC64 supports a 64-byte page write operation, effectively providing a 32  $\mu$ s/byte write cycle and enabling the entire memory to be typically written in 0.25 seconds. The X28HC64 also features DATA Polling and Toggle Bit Polling, two methods providing early end of write detection. In addition, the X28HC64 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

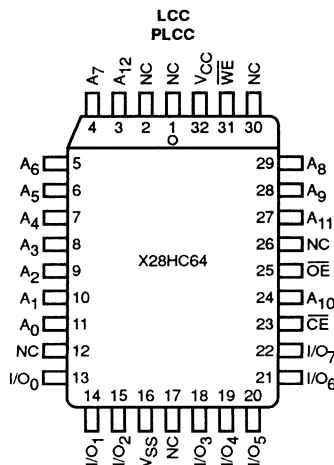
Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

3

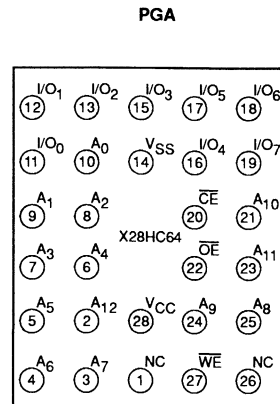
### PIN CONFIGURATION



3857 FHD F02



3857 FHD F03



BOTTOM VIEW

3857 FHD F04



# X28HC64

## PIN DESCRIPTIONS

### Addresses ( $A_0$ – $A_{12}$ )

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{CE}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH, power consumption is reduced.

### Output Enable ( $\overline{OE}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

### Data In/Data Out ( $I/O_0$ – $I/O_7$ )

Data is written to or read from the X28HC64 through the I/O pins.

### Write Enable ( $\overline{WE}$ )

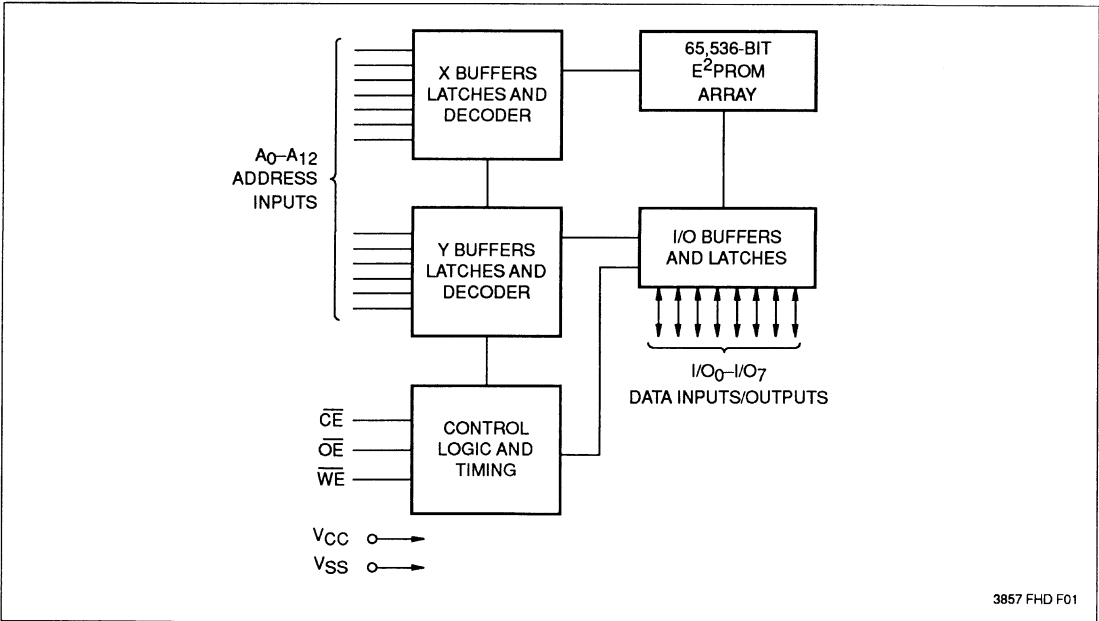
The Write Enable input controls the writing of data to the X28HC64.

## PIN NAMES

Symbol	Description
$A_0$ – $A_{12}$	Address Inputs
$I/O_0$ – $I/O_7$	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$V_{CC}$	+5V
$V_{SS}$	Ground
NC	No Connect

3857 PGM T01

## FUNCTIONAL DIAGRAM



3857 FHD F01

# X28HC64

## DEVICE OPERATION

### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The X28HC64 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 2 ms.

### Page Write Operation

The page write feature of the X28HC64 allows the entire memory to be written in 0.25 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28HC64 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address ( $A_6$  through  $A_{12}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

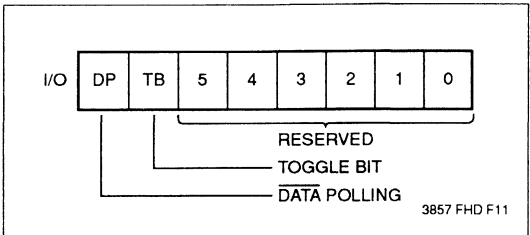
The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page

write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100  $\mu$ s.

### Write Operation Status Bits

The X28HC64 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



### DATA Polling (I/O<sub>7</sub>)

The X28HC64 features  $\overline{DATA}$  Polling as a method to indicate to the host system that the byte write or page write cycle has completed.  $\overline{DATA}$  Polling allows a simple bit test operation to determine the status of the X28HC64, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O<sub>7</sub> (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O<sub>7</sub> will reflect true data.

### Toggle Bit (I/O<sub>6</sub>)

The X28HC64 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O<sub>6</sub> will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

# X28HC64

## DATA POLLING I/O<sub>7</sub>

Figure 2. DATA Polling Bus Sequence

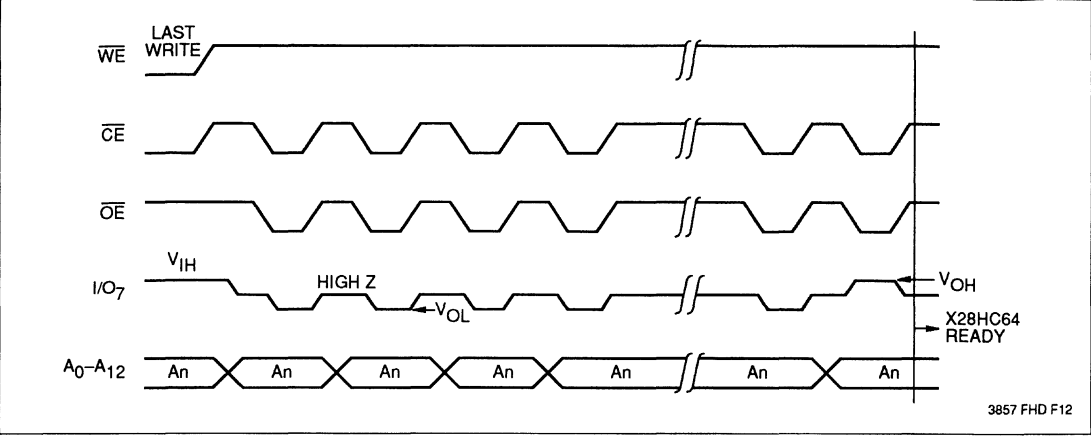
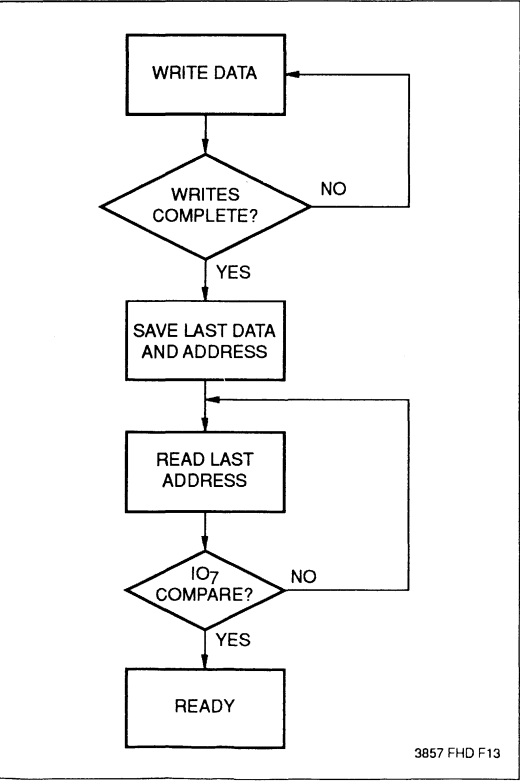


Figure 3. DATA Polling Software Flow



DATA Polling can effectively reduce the time for writing to the X28HC64. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

X28HC64

THE TOGGLE BIT I/O<sub>6</sub>  
Figure 4. Toggle Bit Bus Sequence

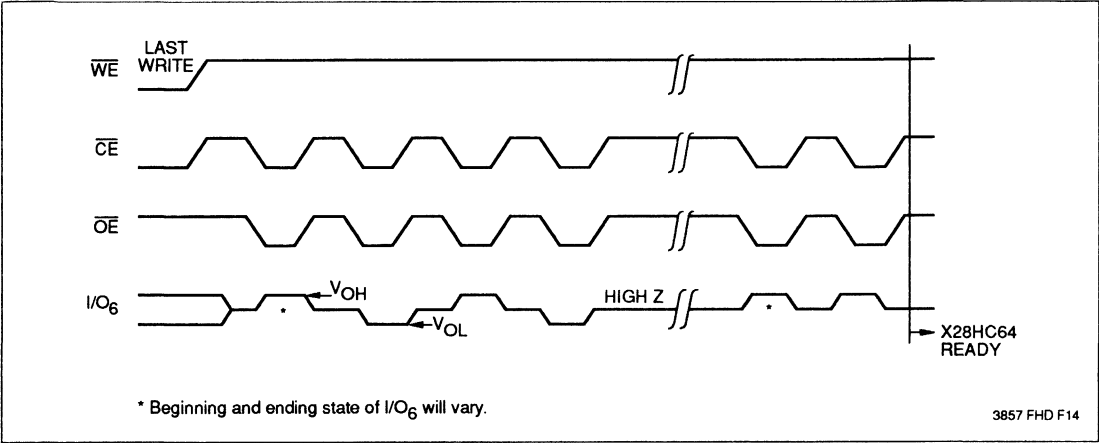
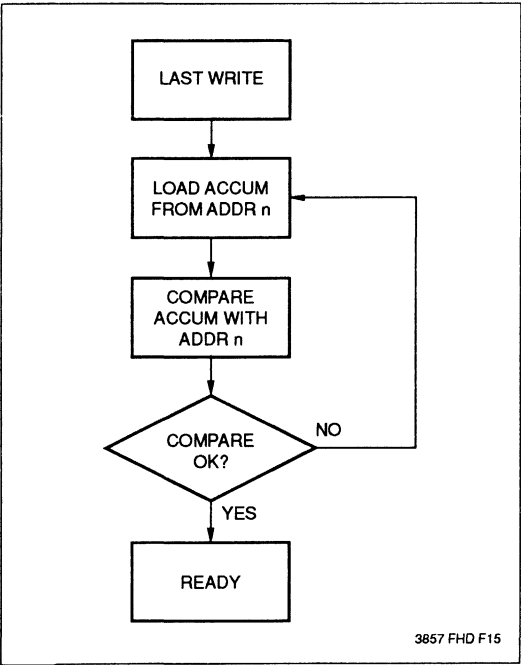


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28HC64 memories that is frequently updated. Toggle Bit testing can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

## X28HC64

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### HARDWARE DATA PROTECTION

The X28HC64 provides two hardware features that protect nonvolatile data from inadvertent writes.

- **Default V<sub>CC</sub> Sense**—All write functions are inhibited when V<sub>CC</sub> is ≤3V typically.
- **Write Inhibit**—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH, or  $\overline{CE}$  HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

### SOFTWARE DATA PROTECTION

The X28HC64 offers a software controlled data protection feature. The X28HC64 is shipped from Xicor with the software data protection **NCT ENABLED**; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V<sub>CC</sub> was stable.

The X28HC64 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection fea-

ture. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28HC64 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

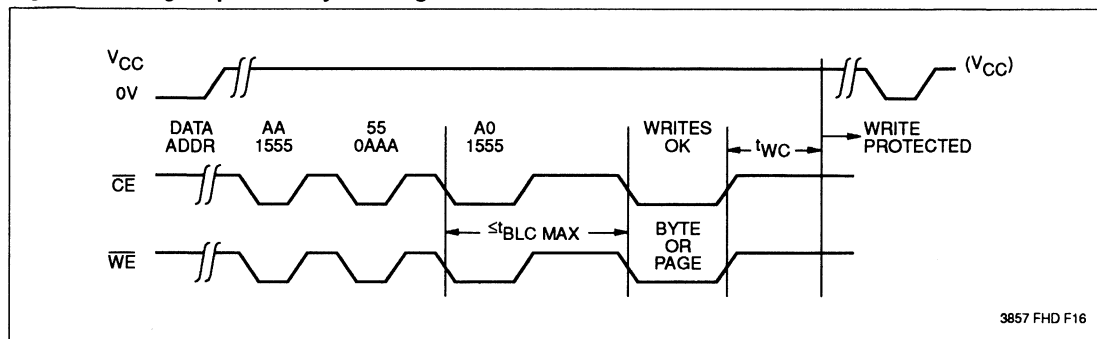
### SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

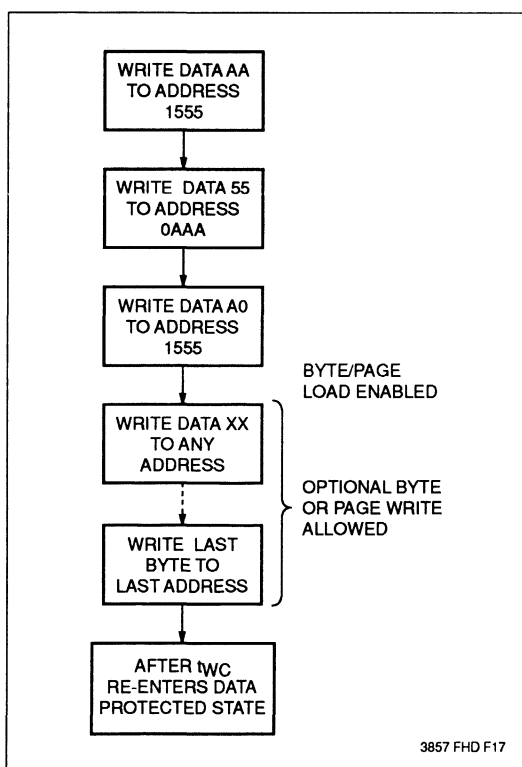
# X28HC64

## SOFTWARE DATA PROTECTION

**Figure 6. Timing Sequence—Byte or Page Write**



### Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used, the X28HC64 will automatically disable further writes unless another command is issued to deactivate it. If no further commands are issued the X28HC64 will be write protected during power-down and after any subsequent power-up.

**Note:** Once initiated, the sequence of write operations should not be interrupted.

X28HC64

RESETTING SOFTWARE DATA PROTECTION  
Figure 8. Reset Software Data Protection Timing Sequence

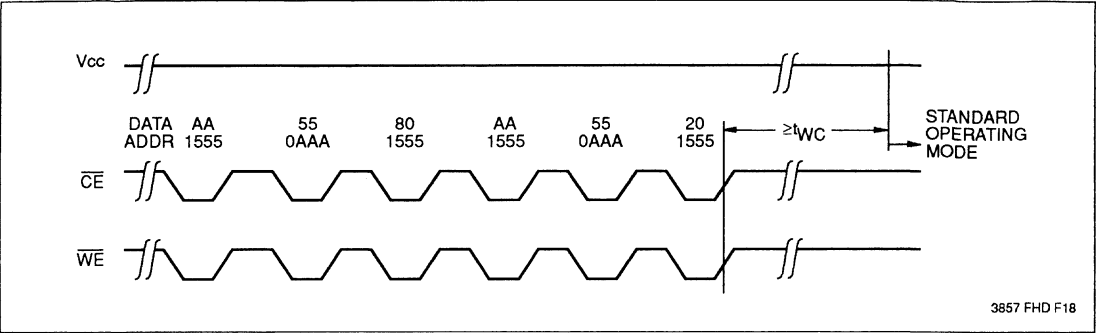
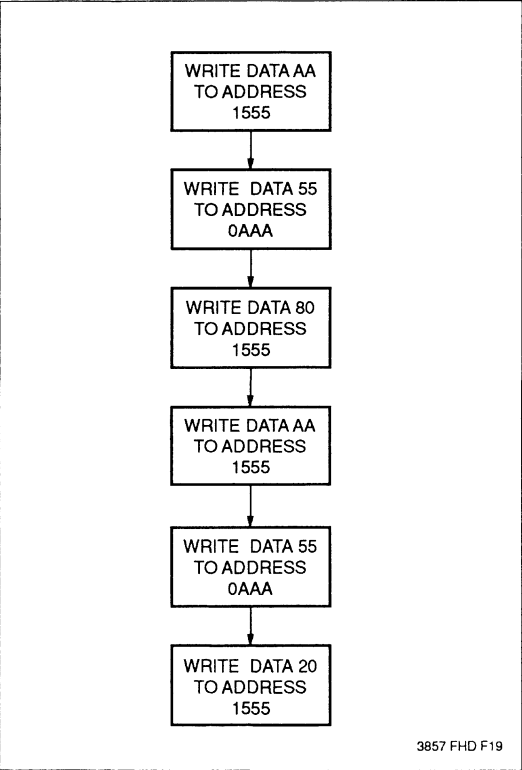


Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E<sup>2</sup>PROM programmer, the following six step algorithm will reset the internal protection circuit. After t<sub>wc</sub>, the X28HC64 will be in standard operating mode.

*Note:* Once initiated, the sequence of write operations should not be interrupted.

*It should also be noted, the Reset SDP operation performs a device "program" operation; whereby **all** bytes are written to 00[H].*

# X28HC64

## SYSTEM CONSIDERATIONS

Because the X28HC64 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

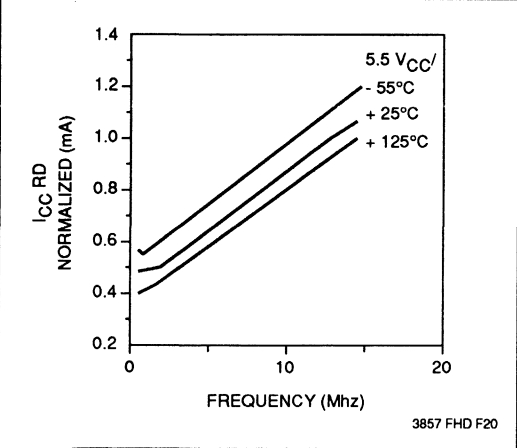
Because the X28HC64 has two power modes, standby and active, proper decoupling of the memory array is of

prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu$ F high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

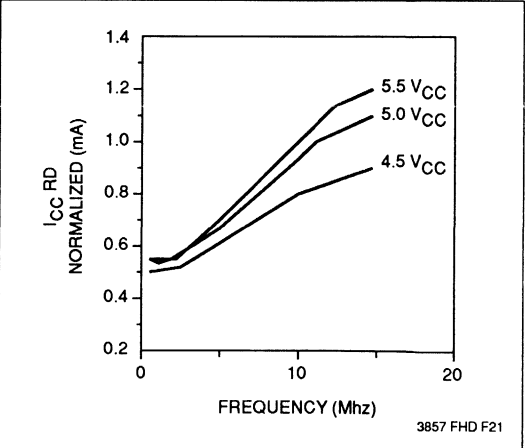
In addition, it is recommended that a 4.7  $\mu$ F electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

3

Normalized  $I_{CCRD}$  by Temperature Over Frequency



Normalized  $I_{CCRD}$  @ 25% Over the  $V_{CC}$  Range and Frequency





X28HC64

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X28HC64	−10°C to +85°C
X28HC64I, X28HC64M	−65°C to +135°C
Storage Temperature	
	−65°C to +150°C
Voltage on any Pin with	
Respect to Ground	−1.0V to +7.0V
D.C. Output Current	
	5 mA
Lead Temperature	
(Soldering, 10 Seconds)	300°C

\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

3857 PGM T02

Supply Voltage	Limits
X28HC64	5V ± 10%

3857 PGM T03

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Current (Active) (TTL Inputs)		15	40	mA	CE = OE = V <sub>IL</sub> , WE = V <sub>IH</sub> , All I/O's = Open, Address Inputs = TTL Levels @ f = 10 MHz
I <sub>SB1</sub>	V <sub>CC</sub> Current (Standby) (TTL Inputs)		1	2	mA	CE = V <sub>IH</sub> , OE = V <sub>IL</sub> All I/O's = Open, Other Inputs = V <sub>IH</sub>
I <sub>SB2</sub>	V <sub>CC</sub> Current (Standby) (CMOS Inputs)		100	200	μA	CE = V <sub>CC</sub> − 0.3V, OE = GND All I/O's = Open, Other Inputs = V <sub>CC</sub> − 0.3V
I <sub>LI</sub>	Input Leakage Current			±10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current			±10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , CE = V <sub>IH</sub>
V <sub>IL</sub> (2)	Input Low Voltage	−1.0		0.8	V	
V <sub>IH</sub> (2)	Input High Voltage	2.0		V <sub>CC</sub> + 1.0	V	
V <sub>OL</sub>	Output Low Voltage			0.4	V	I <sub>OL</sub> = 5 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = −5 mA

3857 PGM T04

Notes: (1) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage  
(2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.

X28HC64

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Unit
Minimum Endurance	10,000		Cycles/Byte
Data Retention	100		Years

3857 PGM T05

POWER-UP TIMING

Symbol	Parameter	Typ. (1)	Units
tPUR(3)	Power-up to Read Operation	100	μs
tPUW(3)	Power-up to Write Operation	5	ms

3857 PGM T06

CAPACITANCE TA = 25°C, f = 1.0 MHz, VCC = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C <sub>I/O</sub> (3)	Input/Output Capacitance	10	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (3)	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

3857 PGM T07

3

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	1.5V

3857 PGM T08

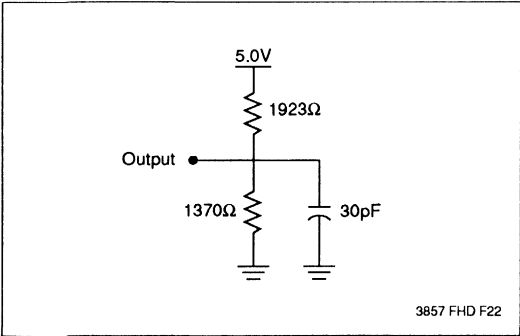
MODE SELECTION

CE	OE	WE	Mode	I/O	Power
L	L	H	Read	D <sub>OUT</sub>	Active
L	H	L	Write	D <sub>IN</sub>	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3857 PGM T09

Note: (3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUITS



3857 FHD F22

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

# X28HC64

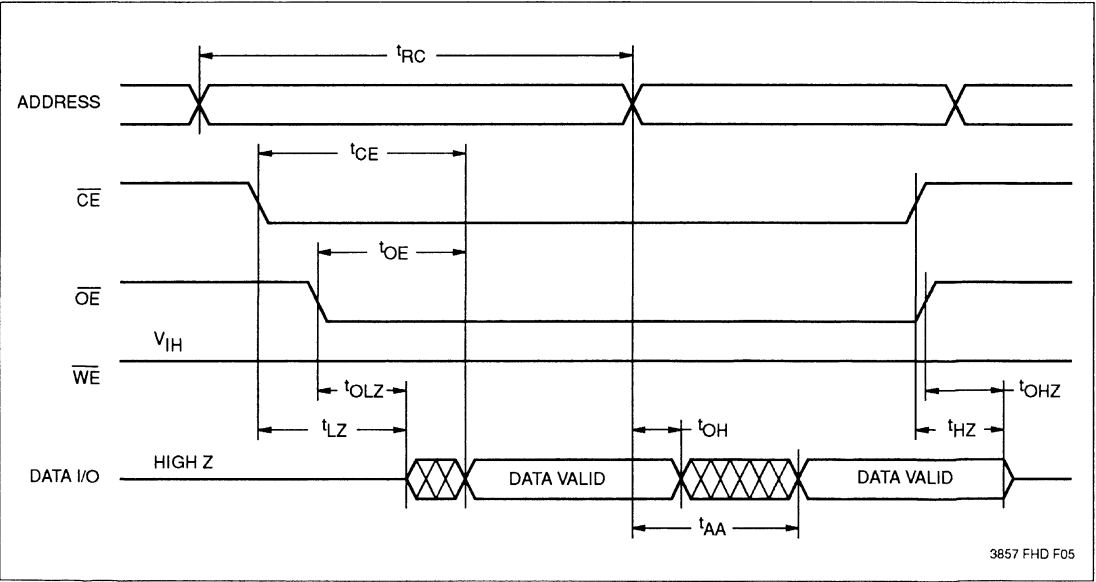
## A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

### Read Cycle Limits

Symbol	Parameter	X28HC64-55		X28HC64-70		X28HC64-90		X28HC64-12		Units
		-40°C to +85°C		-55°C to +125°C		-55°C to +125°C		-55°C to +125°C		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	55		70		90		120		ns
t <sub>CE</sub>	Chip Enable Access Time		55		70		90		120	ns
t <sub>AA</sub>	Address Access Time		55		70		90		120	ns
t <sub>OE</sub>	Output Enable Access Time		30		35		40		50	ns
t <sub>LZ</sub> <sup>(4)</sup>	CE Low to Active Output	0		0		0		0		ns
t <sub>OLZ</sub> <sup>(4)</sup>	OE Low to Active Output	0		0		0		0		ns
t <sub>HZ</sub> <sup>(4)</sup>	CE High to High Z Output		30		30		30		30	ns
t <sub>OHZ</sub> <sup>(4)</sup>	OE High to High Z Output		30		30		30		30	ns
t <sub>OH</sub>	Output Hold from Address Change	0		0		0		0		ns

3856 PGM T10

### Read Cycle



3857 FHD F05

**Notes:** (4)  $t_{LZ}$  min.,  $t_{HZ}$ ,  $t_{OLZ}$  min., and  $t_{OHZ}$  are periodically sampled and not 100% tested.  $t_{HZ}$  max. and  $t_{OHZ}$  max. are measured from the point when  $\overline{CE}$  or  $\overline{OE}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

X28HC64

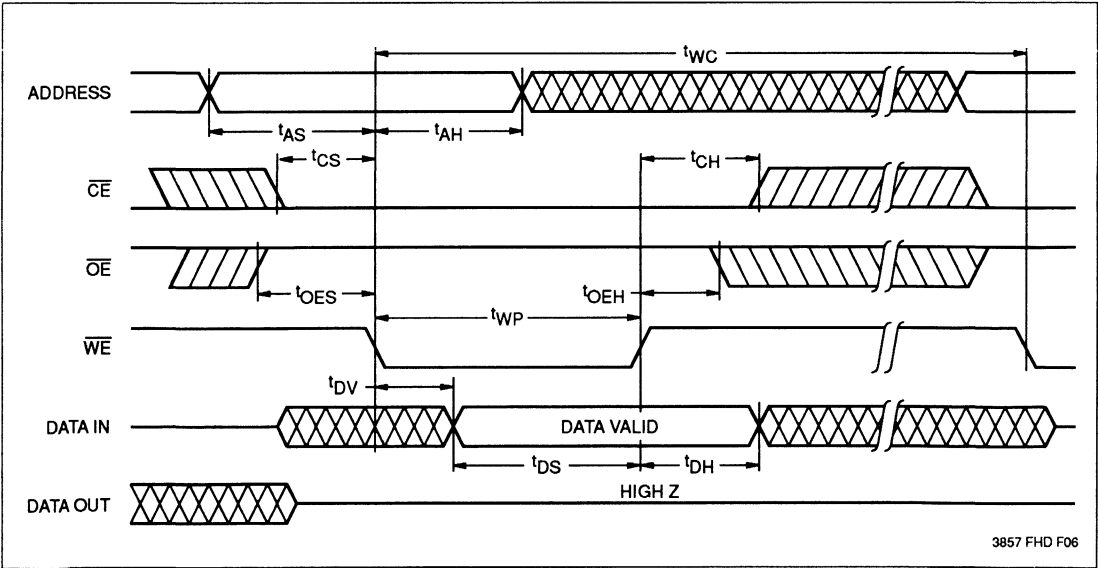
WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Typ. <sup>(1)</sup>	Max.	Units
t <sub>WC</sub> <sup>(5)</sup>	Write Cycle Time		2	5	ms
t <sub>AS</sub>	Address Setup Time	0			ns
t <sub>AH</sub>	Address Hold Time	50			ns
t <sub>CS</sub>	Write Setup Time	0			ns
t <sub>CH</sub>	Write Hold Time	0			ns
t <sub>CW</sub>	CE Pulse Width	50			ns
t <sub>OES</sub>	OE High Setup Time	0			ns
t <sub>OEH</sub>	OE High Hold Time	0			ns
t <sub>WP</sub>	WE Pulse Width	50			ns
t <sub>WPH</sub> <sup>(6)</sup>	WE High Recovery	50			ns
t <sub>DV</sub> <sup>(6)</sup>	Data Valid			1	μs
t <sub>DS</sub>	Data Setup	50			ns
t <sub>DH</sub>	Data Hold	0			ns
t <sub>DW</sub> <sup>(6)</sup>	Delay to Next Write	10			μs
t <sub>BLC</sub>	Byte Load Cycle	0.150		100	μs

3857 PGM T11

3

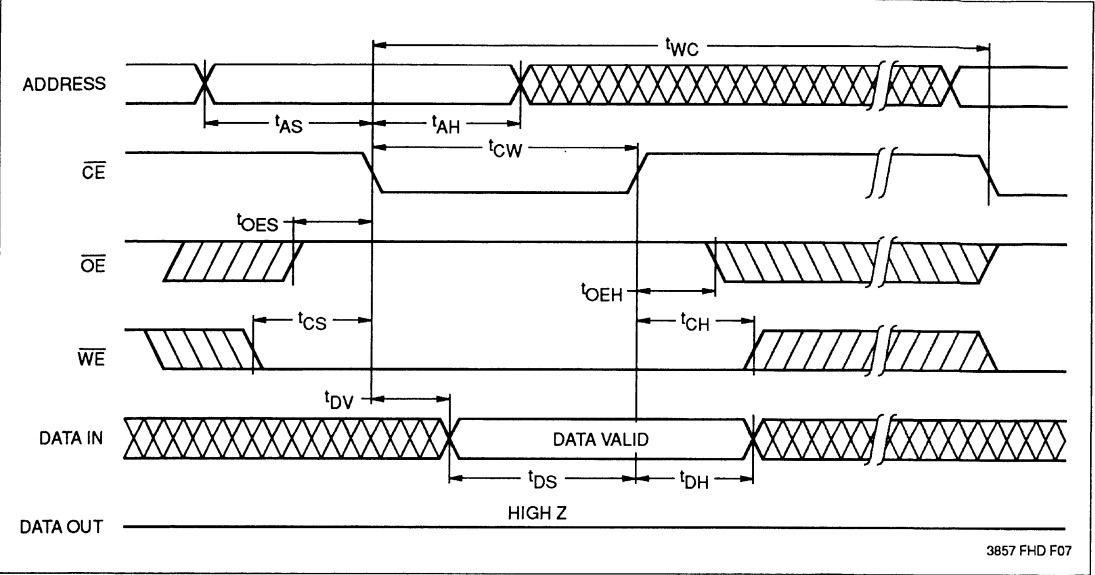
WE Controlled Write Cycle



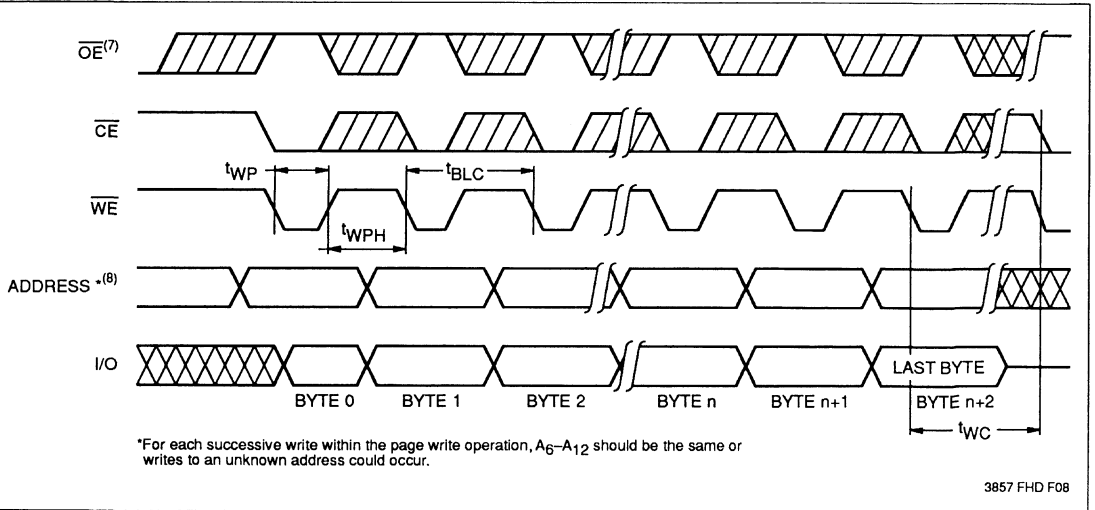
Notes: (5)  $t_{WC}$  is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.  
(6)  $t_{WPH}$  and  $t_{DW}$  are periodically sampled and not 100% tested.

# X28HC64

## $\overline{\text{CE}}$ Controlled Write Cycle



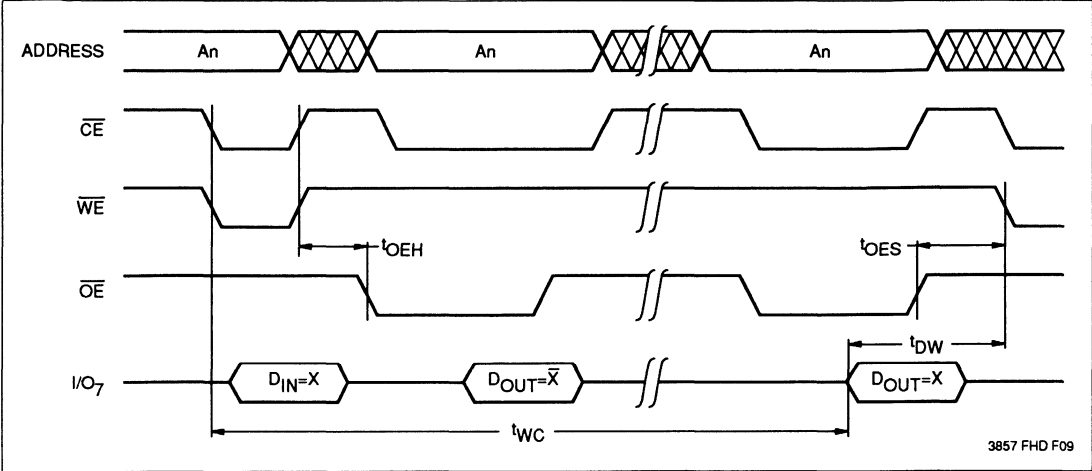
## Page Write Cycle



- Notes:** (7) Between successive byte writes within a page write operation,  $\overline{\text{OE}}$  can be strobed LOW: e.g. this can be done with  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  HIGH to fetch data from another memory device within the system for the next write; or with  $\overline{\text{WE}}$  HIGH and  $\overline{\text{CE}}$  LOW effectively performing a polling operation.
- (8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  controlled write cycle timing.

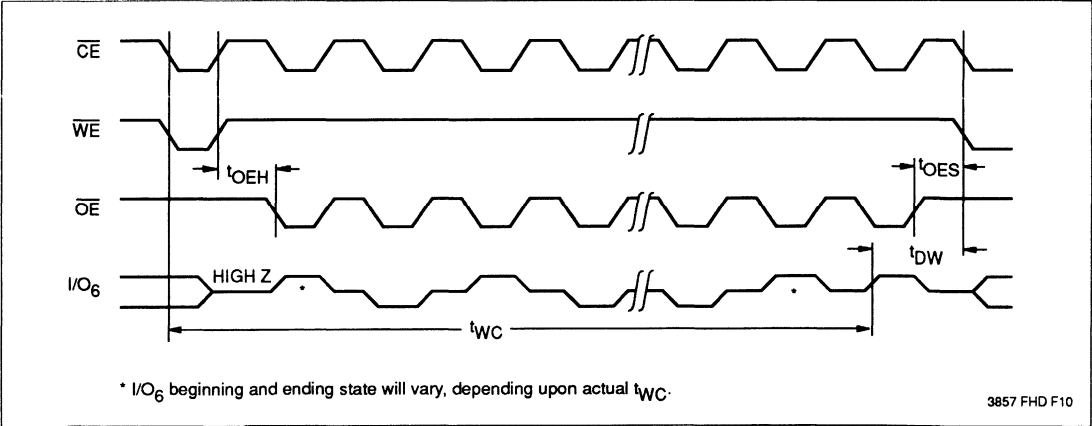
X28HC64

DATA Polling Timing Diagram<sup>(9)</sup>



3

Toggle Bit Timing Diagram<sup>(9)</sup>



**Note:** (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

**X28HC64**

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**NOTES**



256K

X28C256

32K x 8 Bit

## 5 Volt, Byte Alterable E<sup>2</sup>PROM

### FEATURES

- Access Time: 150ns
- SIMPLE Byte and Page Write
  - Single 5 Volt Supply
  - No External High Voltages or V<sub>pp</sub> Control Circuits
  - Self Timed
  - No Erase Before Write
  - No Complex Programming Algorithms
  - No Overerase Problem
- Low Power CMOS:
  - Active: 60mA
  - Standby: 200 $\mu$ A
- Software Data Protection
  - Protects Data Against System Level Inadvertent Writes
- High Speed Page Write Capability
- Highly Reliable Direct Write™ Cell
  - Endurance: 100,000 Write Cycles
  - Data Retention: 100 Years
- Early End of Write Detection
  - DATA Polling
  - Toggle Bit Polling

### DESCRIPTION

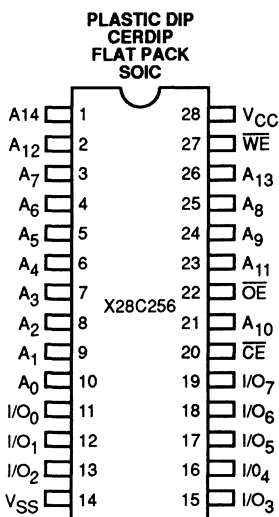
The X28C256 is an 32K x 8 E<sup>2</sup>PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C256 is a 5V only device. The X28C256 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C256 supports a 64-byte page write operation, effectively providing a 78  $\mu$ s/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C256 also features  $\overline{\text{DATA}}$  and Toggle Bit Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C256 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

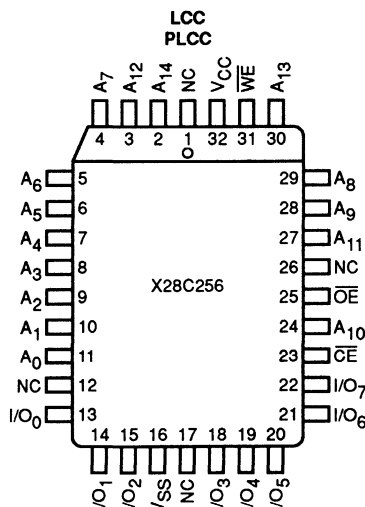
Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

3

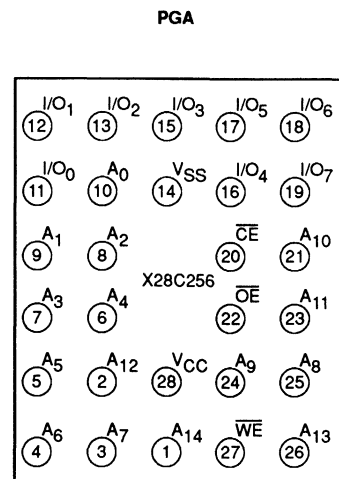
### PIN CONFIGURATION



3855 FHD F02



3855 FHD F03



BOTTOM VIEW

3855 FHD F04



# X28C256

## PIN DESCRIPTIONS

### Addresses (A<sub>0</sub>–A<sub>14</sub>)

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{\text{CE}}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{\text{CE}}$  is HIGH, power consumption is reduced.

### Output Enable ( $\overline{\text{OE}}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

### Data In/Data Out (I/O<sub>0</sub>–I/O<sub>7</sub>)

Data is written to or read from the X28C256 through the I/O pins.

### Write Enable ( $\overline{\text{WE}}$ )

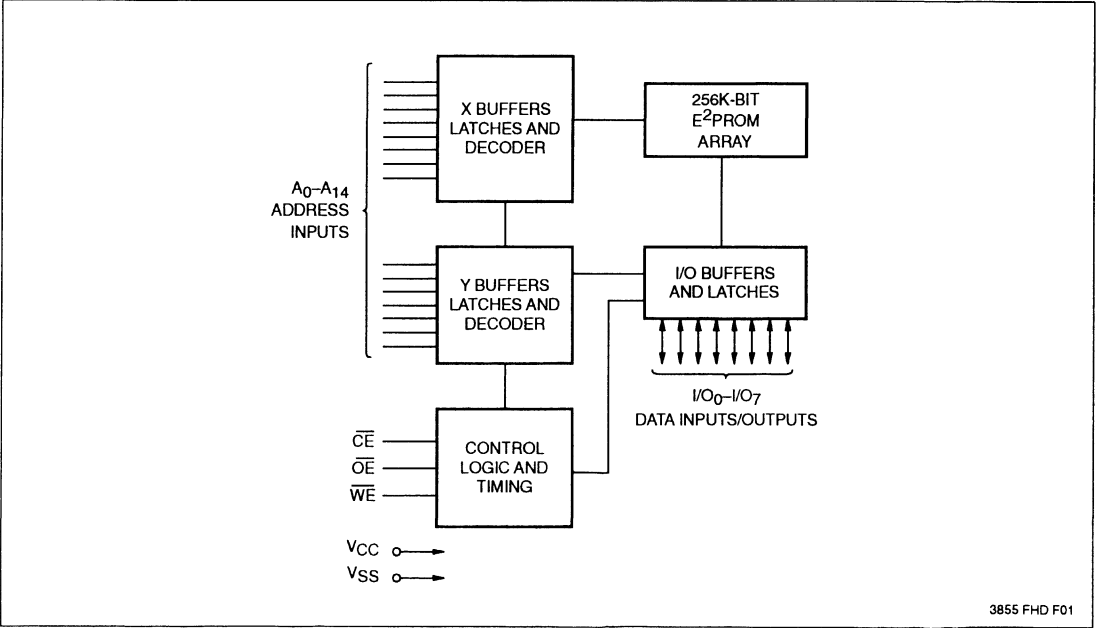
The Write Enable input controls the writing of data to the X28C256.

## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>14</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

3855 PGM T01

## FUNCTIONAL DIAGRAM



3855 FHD F01

# X28C256

## DEVICE OPERATION

### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The X28C256 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

### Page Write Operation

The page write feature of the X28C256 allows the entire memory to be written in 2.5 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C256 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address ( $A_6$  through  $A_{14}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

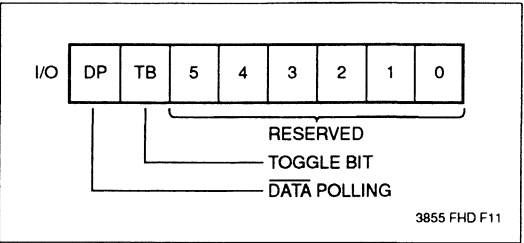
The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host

continues to access the device within the byte load cycle time of 100  $\mu$ s.

### Write Operation Status Bits

The X28C256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



3

### $\overline{DATA}$ Polling ( $I/O_7$ )

The X28C256 features  $\overline{DATA}$  Polling as a method to indicate to the host system that the byte write or page write cycle has completed.  $\overline{DATA}$  Polling allows a simple bit test operation to determine the status of the X28C256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on  $I/O_7$  (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete,  $I/O_7$  will reflect true data. Note: If the X28C256 is in the protected state and an illegal write operation is attempted  $\overline{DATA}$  Polling will not operate.

### Toggle Bit ( $I/O_6$ )

The X28C256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle  $I/O_6$  will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

# X28C256

## DATA POLLING I/O<sub>7</sub>

Figure 2. DATA Polling Bus Sequence

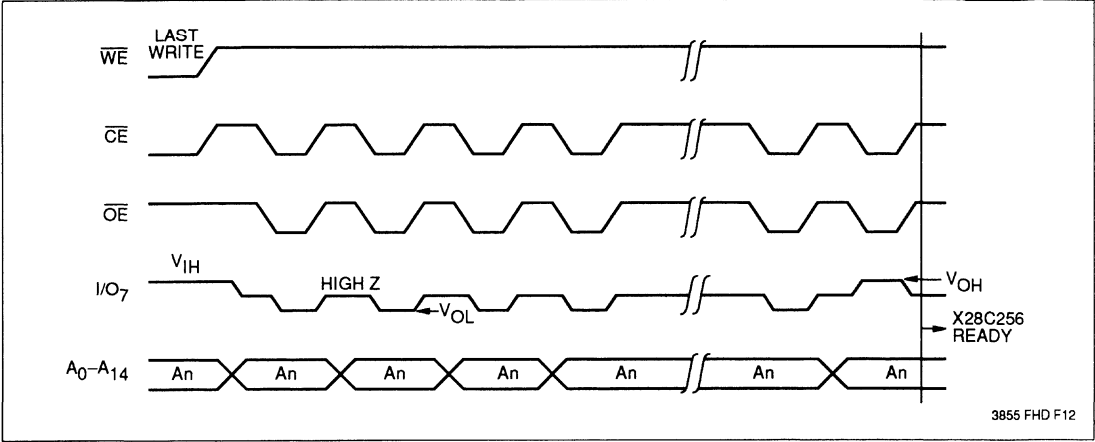
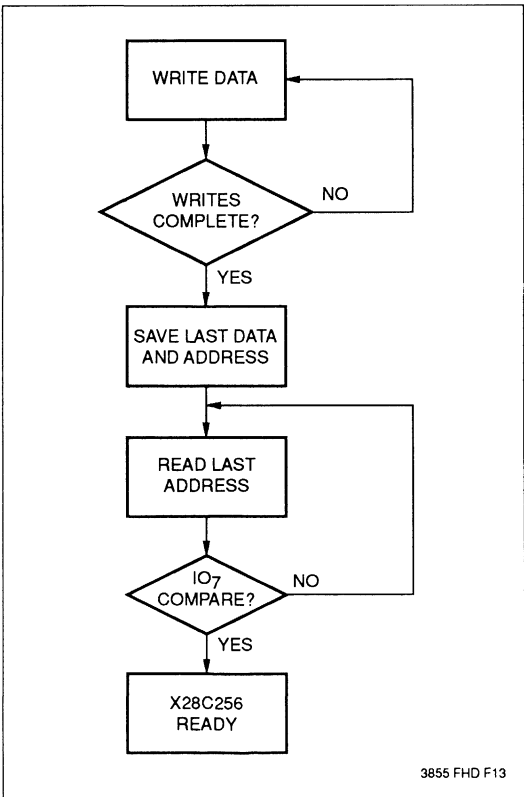


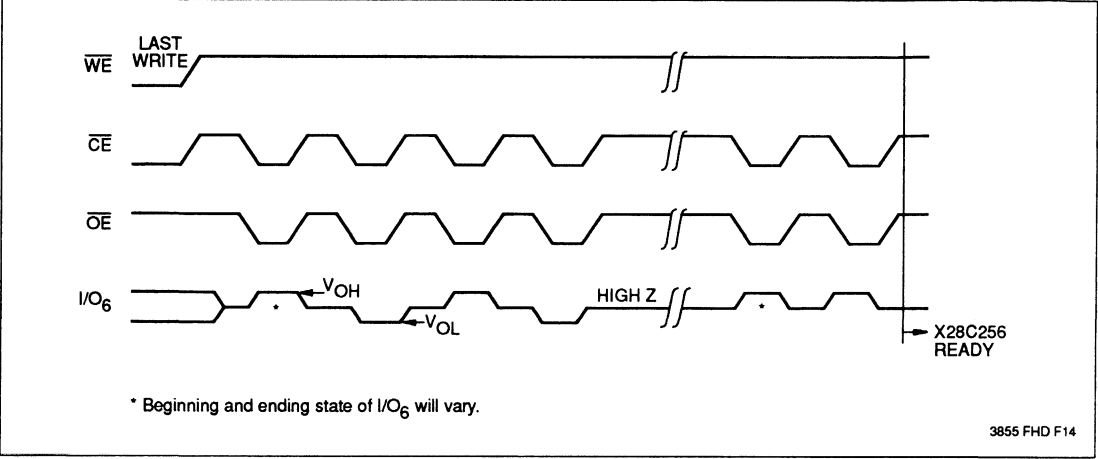
Figure 3. DATA Polling Software Flow



DATA Polling can effectively halve the time for writing to the X28C256. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

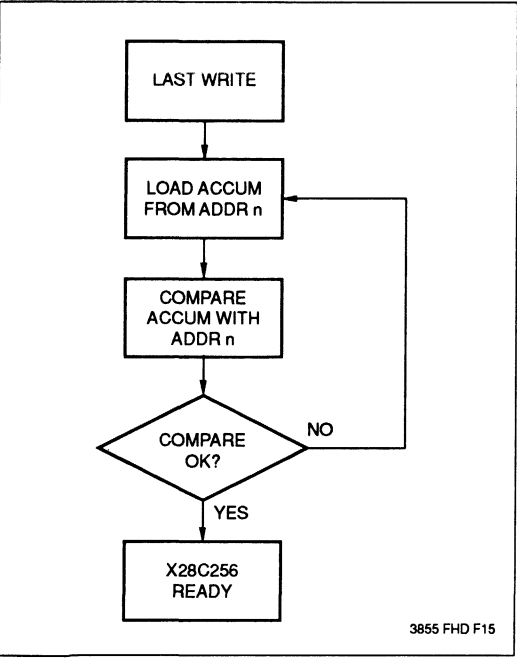
X28C256

THE TOGGLE BIT I/O<sub>6</sub>  
Figure 4. Toggle Bit Bus Sequence



3

Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28C256 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

## X28C256

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### HARDWARE DATA PROTECTION

The X28C256 provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A  $\overline{WE}$  pulse typically less than 20 ns will not initiate a write cycle.
- Default  $V_{CC}$  Sense—All write functions are inhibited when  $V_{CC}$  is  $\leq 3.5V$  typically.
- Write Inhibit—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH, or  $\overline{CE}$  HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

### SOFTWARE DATA PROTECTION

The X28C256 offers a software controlled data protection feature. The X28C256 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once  $V_{CC}$  was stable.

The X28C256 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C256 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

#### Software Algorithm

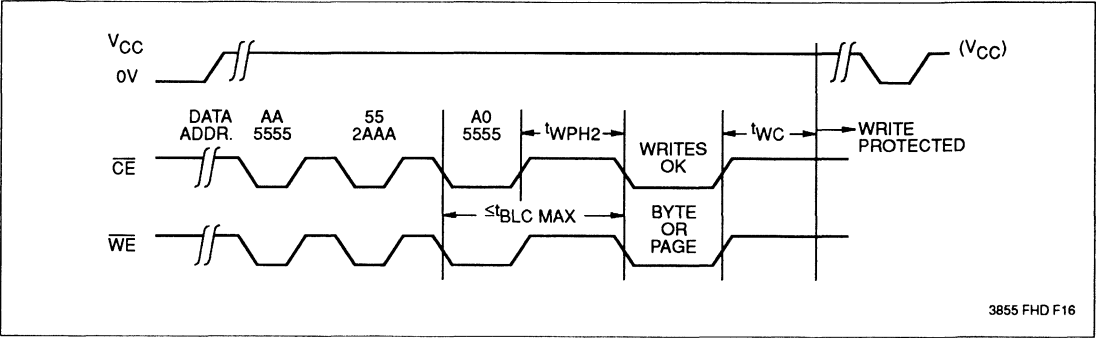
Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data.\* Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

**\*NOTE:** Once the three byte sequence is issued it must be followed by a valid byte or page write operation.

X28C256

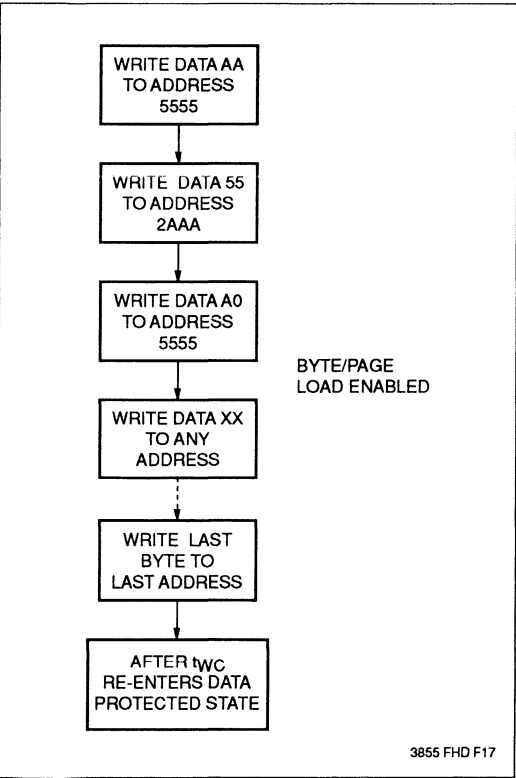
SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write



3

Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C256 will be write protected during power-down and after any subsequent power-up.

*Note: Once initiated, the sequence of write operations should not be interrupted.*

# X28C256

## RESETTING SOFTWARE DATA PROTECTION

Figure 8. Reset Software Data Protection Timing Sequence

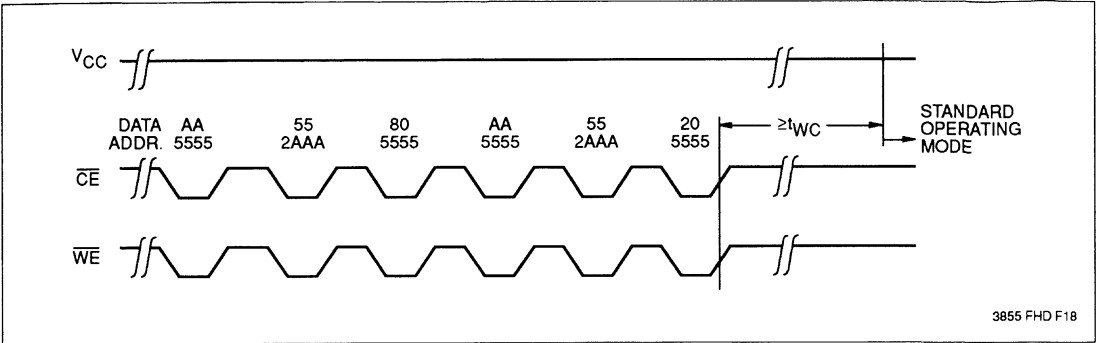
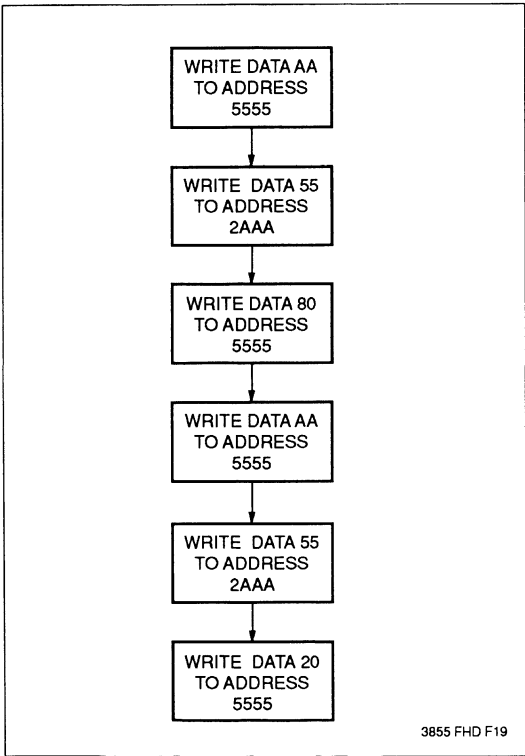


Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E<sup>2</sup>PROM programmer, the following six step algorithm will reset the internal protection circuit. After  $t_{WC}$ , the X28C256 will be in standard operating mode.

*Note: Once initiated, the sequence of write operations should not be interrupted.*

X28C256

SYSTEM CONSIDERATIONS

Because the X28C256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

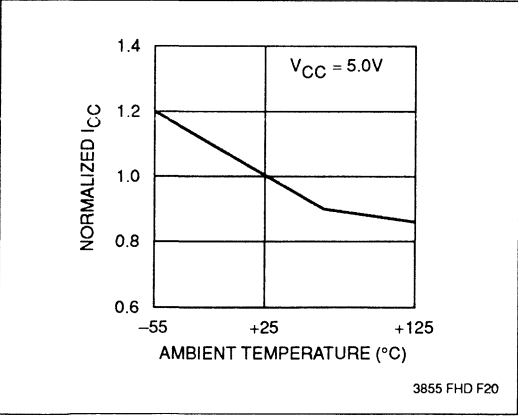
Because the X28C256 has two power modes, standby and active, proper decoupling of the memory array is of

prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu F$  high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

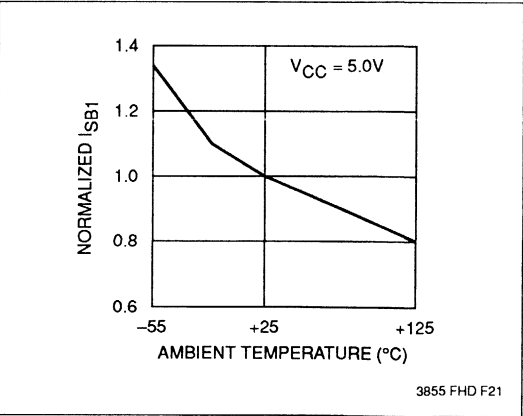
In addition, it is recommended that a 4.7  $\mu F$  electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

3

Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature





## X28C256

### ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias

X28C256 ..... -10°C to +85°C

X28C256I, X28C256M ..... -65°C to +135°C

Storage Temperature ..... -65°C to +150°C

Voltage on any Pin with

Respect to Ground ..... -1.0V to +7.0V

D.C. Output Current ..... 5 mA

Lead Temperature

(Soldering, 10 Seconds) ..... 300°C

### \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

3855 PGM T01

Supply Voltage	Limits
X28C256	5V ± 10%

3855 PGM T02

### D.C. OPERATING CHARACTERISTICS (over recommended operating conditions, unless otherwise specified)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Current (Active) (TTL Inputs)			60	mA	CE = OE = V <sub>IL</sub> , WE = V <sub>IH</sub> , All I/O's = Open, Address Inputs = .4V/2.4V @ f = 5MHz
I <sub>SB1</sub>	V <sub>CC</sub> Current (Standby) (TTL Inputs)			2	mA	CE = V <sub>IH</sub> , OE = V <sub>IL</sub> All I/O's = Open, Other Inputs = V <sub>IH</sub>
I <sub>SB2</sub> (2)	V <sub>CC</sub> Current (Standby) (CMOS Inputs)		200	500	μA	CE = V <sub>CC</sub> - 0.3V, OE = V <sub>IL</sub> All I/O's = Open, Other Inputs = V <sub>CC</sub> - 0.3V
I <sub>LI</sub>	Input Leakage Current			10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current			10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , CE = V <sub>IH</sub>
V <sub>IL</sub> (3)	Input Low Voltage	-1.0		0.8	V	
V <sub>IH</sub> (3)	Input High Voltage	2.0		V <sub>CC</sub> + 1.0	V	
V <sub>OL</sub>	Output Low Voltage			0.4	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = -400 μA

**Notes:** (1) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage and are not tested

(2) I<sub>SB2</sub> Max of 200 μA available from Xicor. Contact local sales office and reference X28C256 C7125.

(3) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.

X28C256

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	10,000	Cycles/Byte
Data Retention	100	Years

3855 PGM T03

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t <sub>PUR</sub> (4)	Power-up to Read Operation	100	μs
t <sub>PW</sub> (4)	Power-up to Write Operation	5	ms

3855 PGM T04

CAPACITANCE T<sub>A</sub> = 25°C, f = 1.0 MHz, V<sub>CC</sub> = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C <sub>I/O</sub> (4)	Input/Output Capacitance	10	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (4)	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

3855 PGM T05

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V

3855 PGM T06

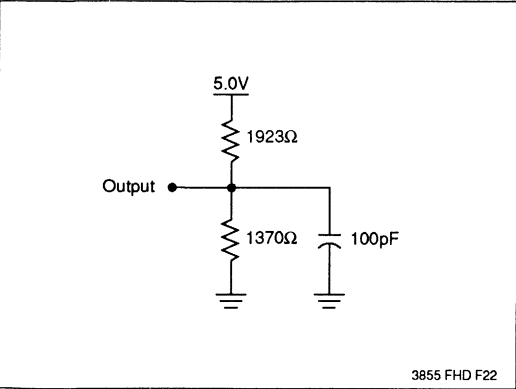
MODE SELECTION

CE	OE	WE	Mode	I/O	Power
L	L	H	Read	D <sub>OUT</sub>	Active
L	H	L	Write	D <sub>IN</sub>	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3855 PGM T07

Note: (4) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



3855 FHD F22

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

# X28C256

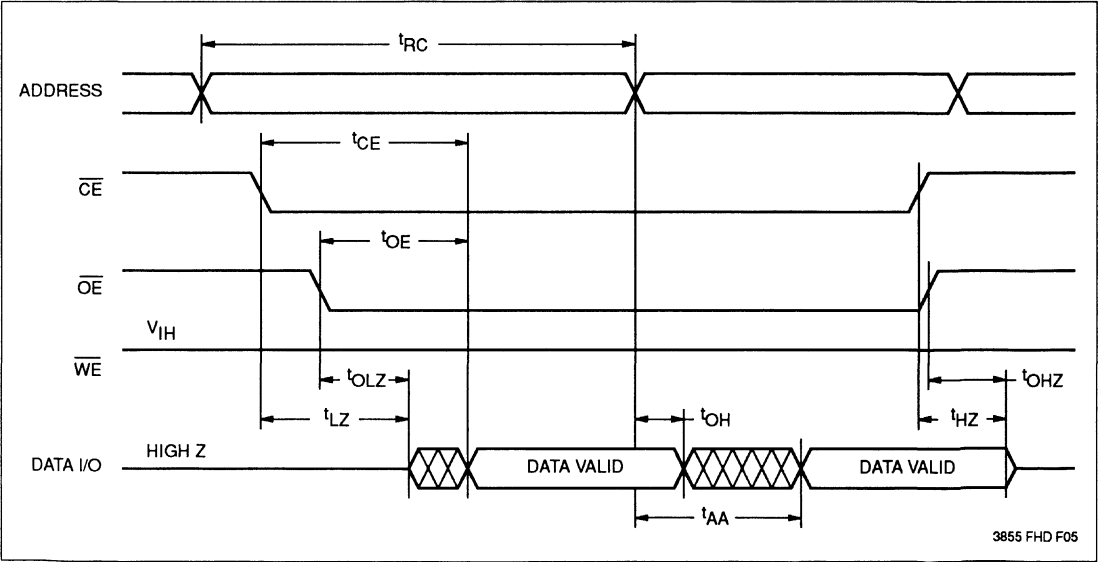
## A.C. CHARACTERISTICS (over recommended operating conditions, unless otherwise specified)

### Read Cycle Limits

Symbol	Parameter	X28C256-15		X28C256-20		X28C256-25		X28C256		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	150		200		250		300		ns
$t_{CE}$	Chip Enable Access Time		150		200		250		300	ns
$t_{AA}$	Address Access Time		150		200		250		300	ns
$t_{OE}$	Output Enable Access Time		50		80		100		100	ns
$t_{LZ}^{(5)}$	$\overline{CE}$ Low to Active Output	0		0		0		0		ns
$t_{OLZ}^{(5)}$	$\overline{OE}$ Low to Active Output	0		0		0		0		ns
$t_{HZ}^{(5)}$	$\overline{CE}$ High to High Z Output		50		50		50		50	ns
$t_{OHZ}^{(5)}$	$\overline{OE}$ High to High Z Output		50		50		50		50	ns
$t_{OH}$	Output Hold from Address Change	0		0		0		0		ns

3853 PGM T08

### Read Cycle



3855 FHD F05

**Note:** (5)  $t_{LZ}$  min.,  $t_{HZ}$ ,  $t_{OLZ}$  min., and  $t_{OHZ}$  are periodically sampled and not 100% tested.  $t_{HZ}$  and  $t_{OHZ}$  are measured, with  $C_L = 5\text{pF}$ , from the point when  $\overline{CE}$  or  $\overline{OE}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

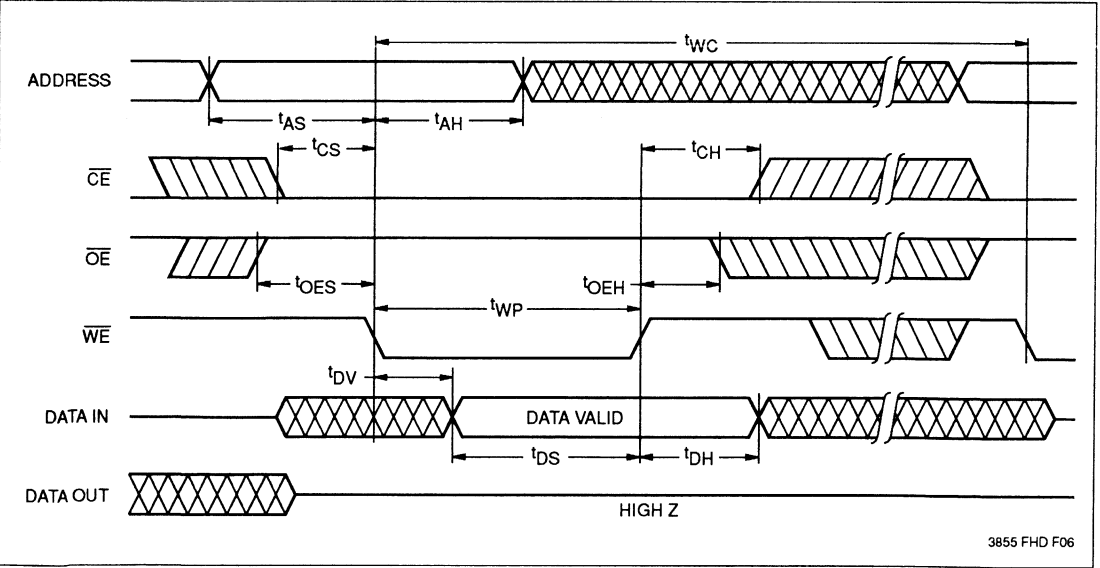
X28C256

WRITE CYCLE LIMITS

Symbol	Parameter	Min.(9)	Typ.(6)	Max.	Units
t <sub>WC</sub> (7)	Write Cycle Time		5	10	ms
t <sub>AS</sub>	Address Setup Time	0			ns
t <sub>AH</sub>	Address Hold Time	150			ns
t <sub>CS</sub>	Write Setup Time	0			ns
t <sub>CH</sub>	Write Hold Time	0			ns
t <sub>CW</sub>	CE Pulse Width	100			ns
t <sub>OES</sub>	OE High Setup Time	10			ns
t <sub>OEH</sub>	OE High Hold Time	10			ns
t <sub>WP</sub>	WE Pulse Width	100			ns
t <sub>WPH</sub>	WE High Recovery	50			ns
t <sub>WPH2</sub> (8)	SDP We Recovery	1			μs
t <sub>DV</sub>	Data Valid			1	μs
t <sub>DS</sub>	Data Setup	50			ns
t <sub>DH</sub>	Data Hold	10			ns
t <sub>DW</sub>	Delay to Next Write	10			μs
t <sub>BLC</sub> (9)	Byte Load Cycle	1		100	μs

3855 PGM T09

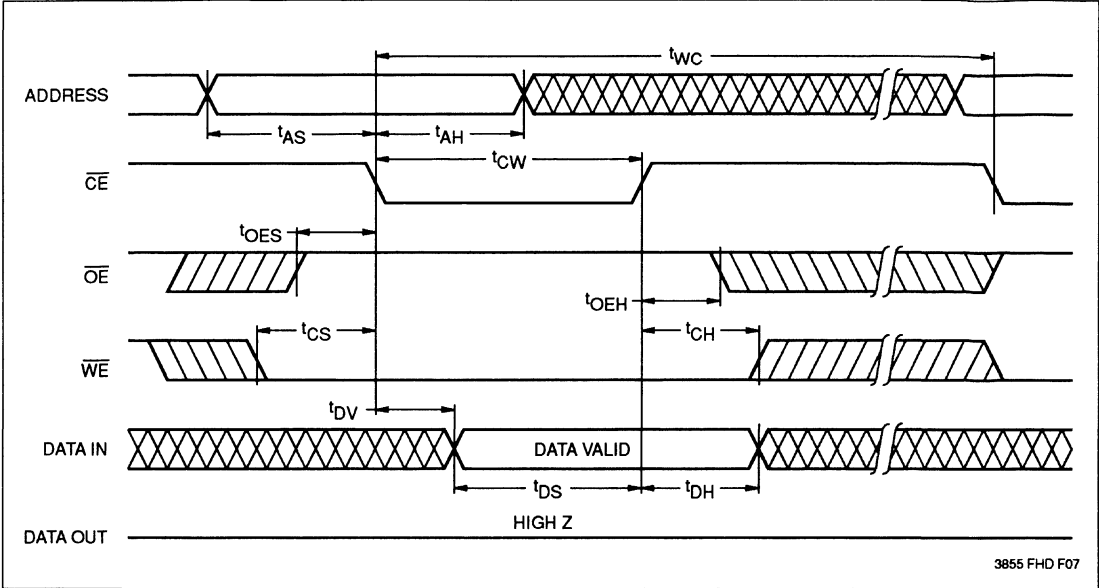
WE Controlled Write Cycle



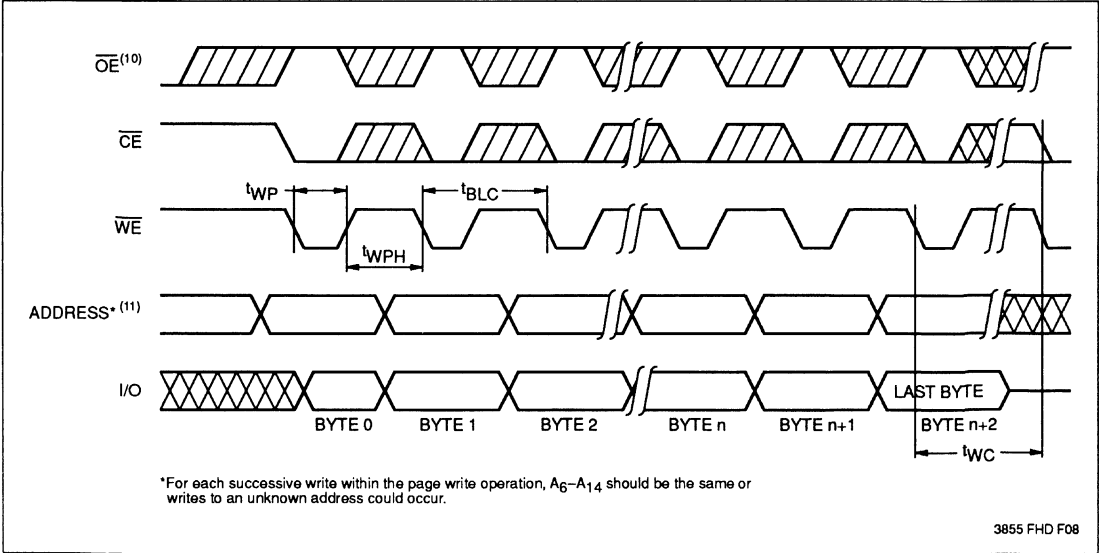
- Notes:** (6) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage.  
(7) t<sub>WC</sub> is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.  
(8) t<sub>WPH</sub> is the normal page write operation WE recovery time. t<sub>WPH2</sub> is the WE recovery time needed only after the end of issuing the three byte SDP command sequence and before writing the first byte of data to the array. Refer to Figure 6 which illustrates the t<sub>WPH2</sub> requirement.  
(9) For faster t<sub>WC</sub> and t<sub>BLC</sub>, refer to X28HC256 or X28VC256.

# X28C256

## CE Controlled Write Cycle



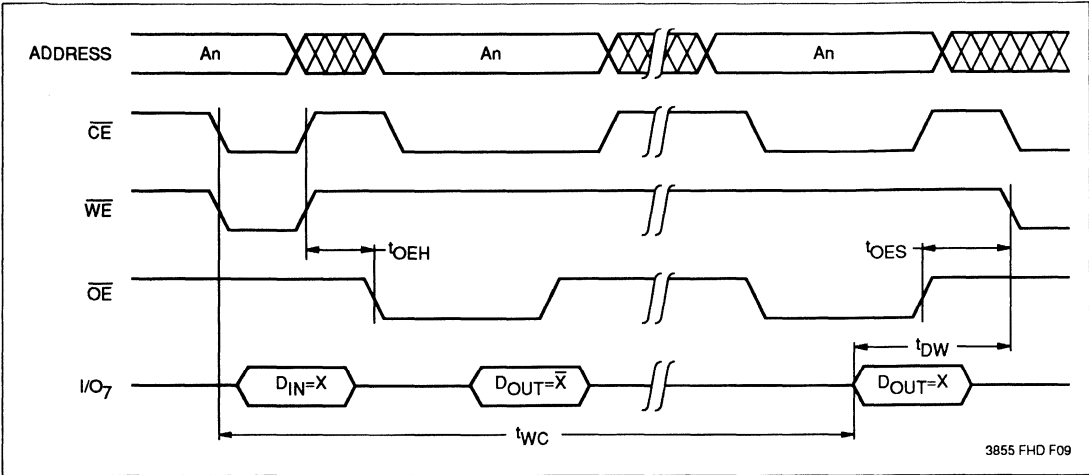
## Page Write Cycle



- Notes:**
- (10) Between successive byte writes within a page write operation,  $\overline{OE}$  can be strobed LOW: e.g. this can be done with  $\overline{CE}$  and  $\overline{WE}$  HIGH to fetch data from another memory device within the system for the next write; or with  $\overline{WE}$  HIGH and  $\overline{CE}$  LOW effectively performing a polling operation.
  - (11) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the  $\overline{CE}$  or  $\overline{WE}$  controlled write cycle timing.

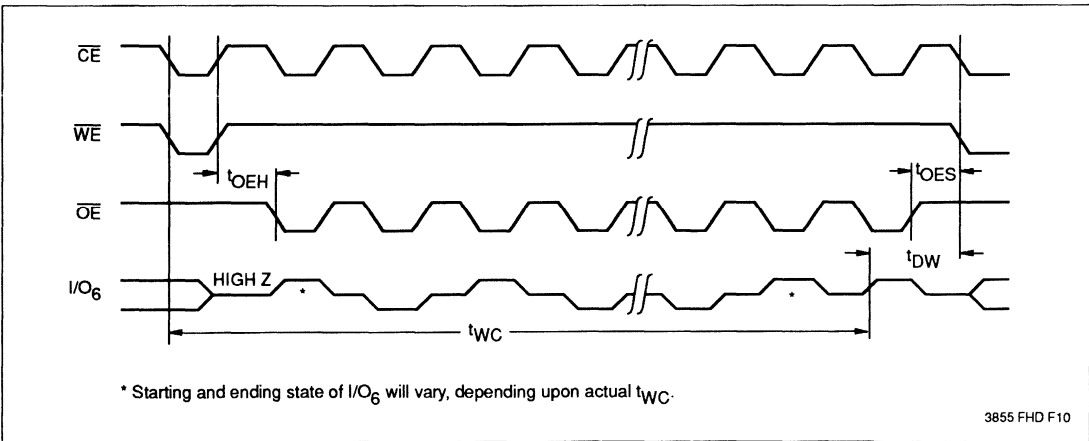
# X28C256

DATA Polling Timing Diagram<sup>(12)</sup>



3

Toggle Bit Timing Diagram<sup>(12)</sup>



**Note:** (12) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

**X28C256**

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**NOTES**

256K

**X28HC256**

32K x 8 Bit

**5 Volt, Byte Alterable E<sup>2</sup>PROM**

**FEATURES**

- Access Time: 70 ns
- SIMPLE Byte and Page Write
  - Single 5 Volt Supply
  - No External High Voltages or V<sub>pp</sub> Control Circuits
  - Self Timed
  - No Erase Before Write
  - No Complex Programming Algorithms
  - No Overerase Problem
- Low Power CMOS:
  - Active: 60mA
  - Standby: 500μA
- Software Data Protection
  - Protects Data Against System Level Inadvertent Writes
- High Speed Page Write Capability
- Highly Reliable Direct Write™ Cell
  - Endurance: 10,000 Write Cycles
  - Data Retention: 100 Years
- Early End of Write Detection
  - DATA Polling
  - Toggle Bit Polling

**DESCRIPTION**

The X28HC256 is a second generation high performance CMOS 32K x 8 E<sup>2</sup>PROM. It is fabricated with Xicor's proprietary, textured poly floating gate technology, providing a highly reliable 5 Volt only nonvolatile memory.

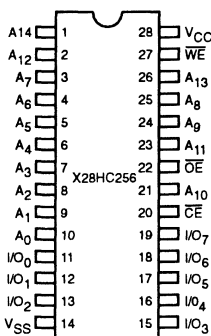
The X28HC256 supports a 128-byte page write operation, effectively providing a 24μs/byte write cycle and enabling the entire memory to be typically rewritten in less than 0.8 seconds. The X28HC256 also features DATA Polling and Toggle Bit polling, two methods of providing early end of write detection. The X28HC256 also supports the JEDEC standard Software Data Protection feature for protecting against inadvertent writes during power-up and power-down.

Endurance for the X28HC256 is specified as a minimum 10,000 write cycles per byte and an inherent data retention of 100 years.

3

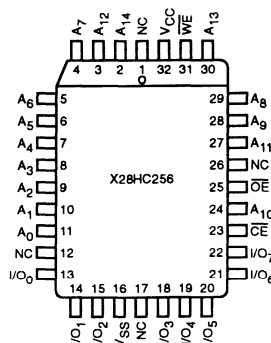
**PIN CONFIGURATION**

PLASTIC DIP  
CERDIP  
FLAT PACK  
SOIC



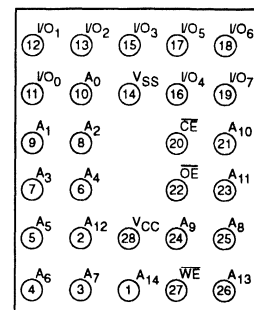
3859 FHD F02

LCC  
PLCC



3859 FHD F03

PGA



X28HC256  
(BOTTOM VIEW)

3859 FHD F04



# X28HC256

## PIN DESCRIPTIONS

### Addresses ( $A_0$ – $A_{14}$ )

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{CE}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH, power consumption is reduced.

### Output Enable ( $\overline{OE}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

### Data In/Data Out ( $I/O_0$ – $I/O_7$ )

Data is written to or read from the X28HC256 through the I/O pins.

### Write Enable ( $\overline{WE}$ )

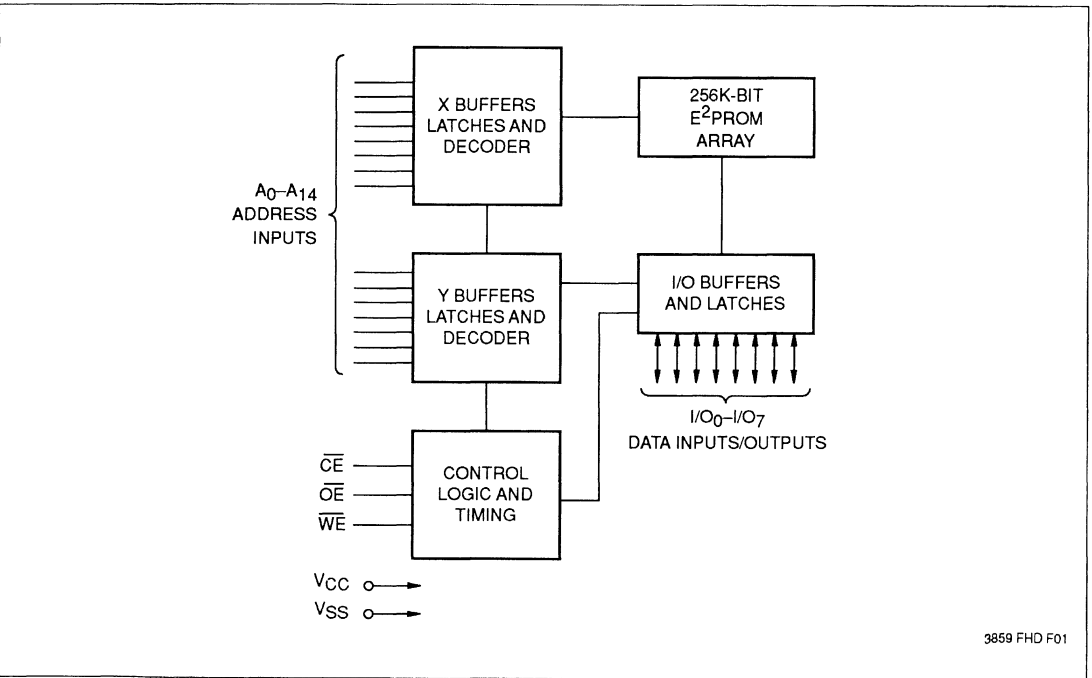
The Write Enable input controls the writing of data to the X28HC256.

## PIN NAMES

Symbol	Description
$A_0$ – $A_{14}$	Address Inputs
$I/O_0$ – $I/O_7$	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VCC	+5V
VSS	Ground
NC	No Connect

3859 PGM T01

## FUNCTIONAL DIAGRAM



3859 FHD F01

## X28HC256

### DEVICE OPERATION

#### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

#### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The X28HC256 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3 ms.

#### Page Write Operation

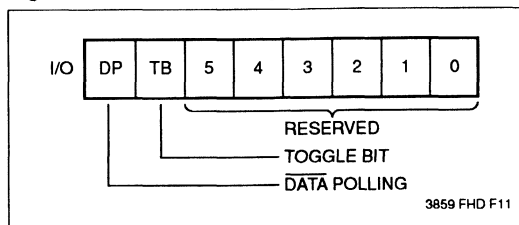
The page write feature of the X28HC256 allows the entire memory to be written in typically 0.8 seconds. Page write allows up to one hundred twenty-eight bytes of data to be consecutively written to the X28HC256 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address ( $A_7$  through  $A_{14}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twenty-seven bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100  $\mu$ s.

#### Write Operation Status Bits

The X28HC256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



#### DATA Polling (I/O<sub>7</sub>)

The X28HC256 features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X28HC256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O<sub>7</sub> (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O<sub>7</sub> will reflect true data.

#### Toggle Bit (I/O<sub>6</sub>)

The X28HC256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O<sub>6</sub> will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read and write operations.

# X28HC256

## DATA POLLING I/O<sub>7</sub>

Figure 2. DATA Polling Bus Sequence

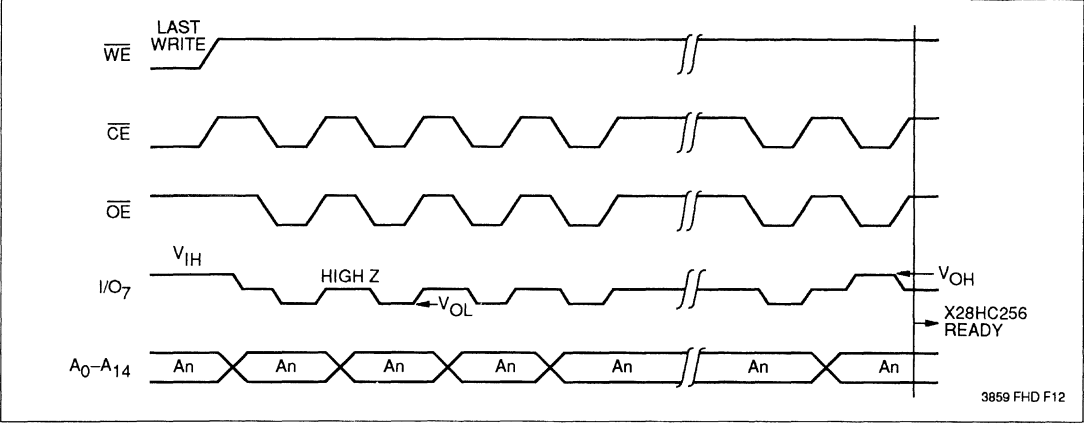
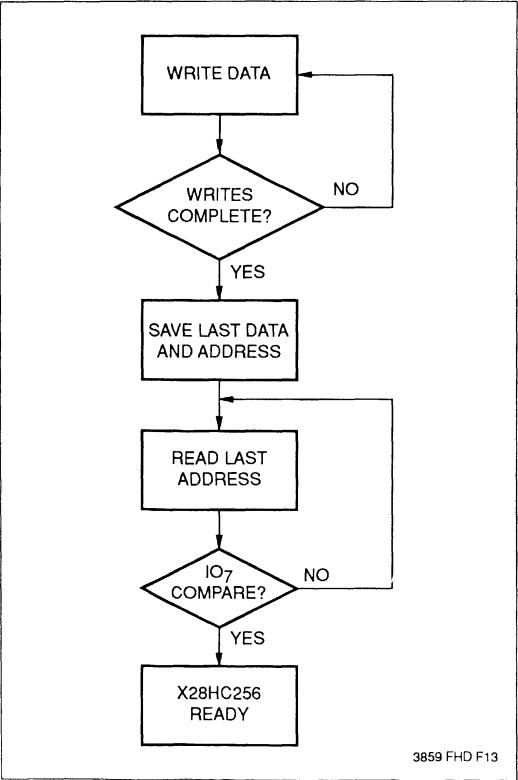


Figure 3. DATA Polling Software Flow

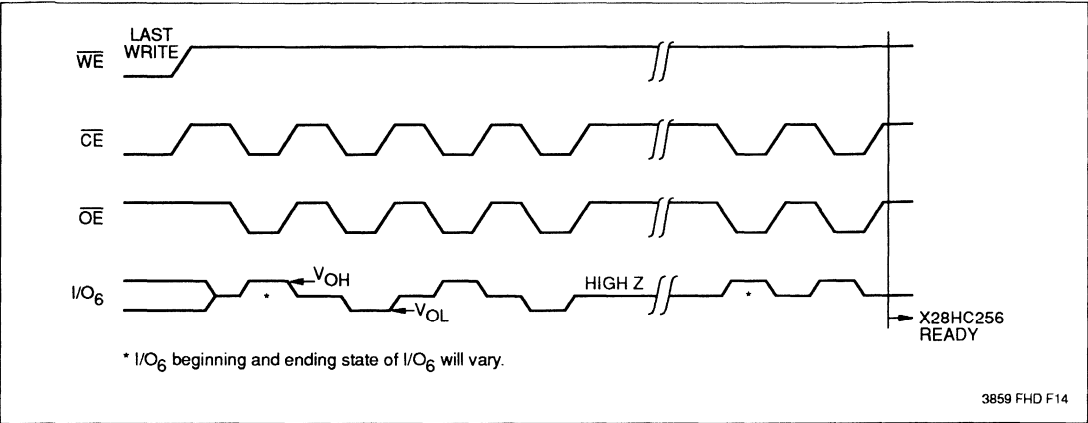


DATA Polling can effectively halve the time for writing to the X28HC256. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

X28HC256

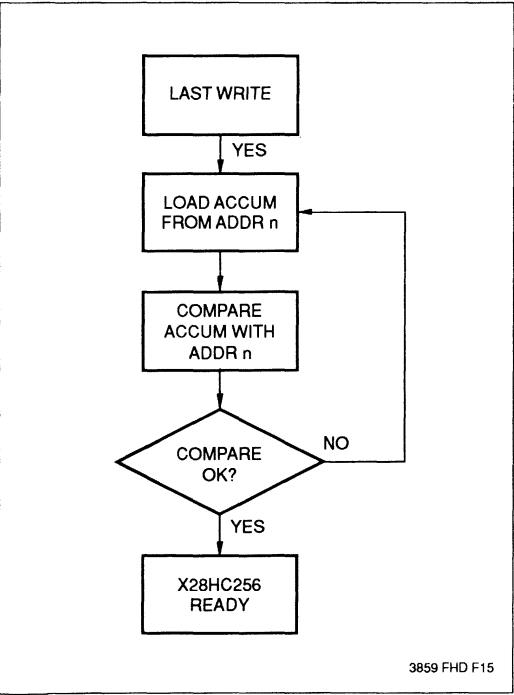
THE TOGGLE BIT I/O<sub>6</sub>

Figure 4. Toggle Bit Bus Sequence



3

Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28HC256 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

## X28HC256

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### HARDWARE DATA PROTECTION

The X28HC256 provides two hardware features that protect nonvolatile data from inadvertent writes.

- Default  $V_{CC}$  Sense—All write functions are inhibited when  $V_{CC}$  is  $\leq 3.5V$  Typically.
- Write Inhibit—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH, or  $\overline{CE}$  HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

### SOFTWARE DATA PROTECTION

The X28HC256 offers a software controlled data protection feature. The X28HC256 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/down operations through the use of external circuits. The host would then have open read and write access of the device once  $V_{CC}$  was stable.

The X28HC256 can be automatically protected during power-up and power-down without the need for external

circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28HC256 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

### SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three byte sequence opens the page write window enabling the host to write from one to one hundred twenty-eight bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

X28HC256

SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write

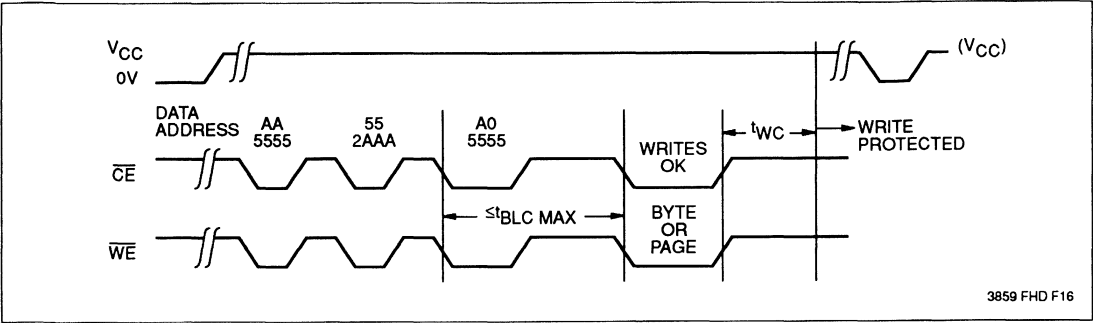
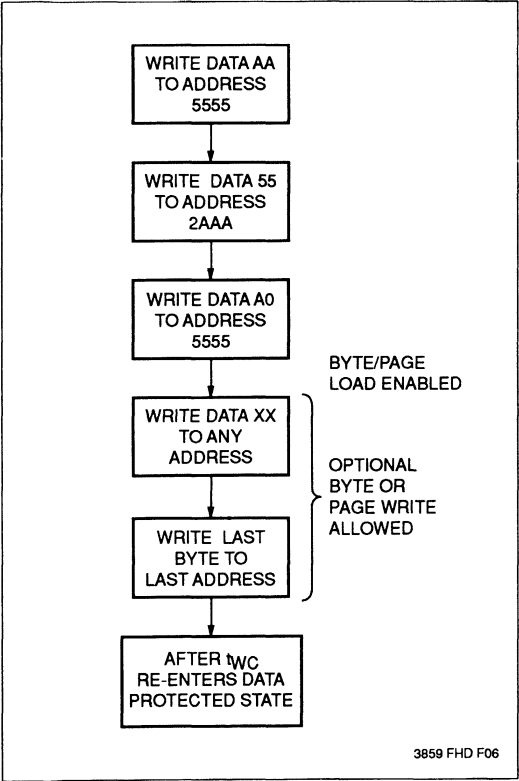


Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28HC256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28HC256 will be write protected during power-down and after any subsequent power-up.

*Note: Once initiated, the sequence of write operations should not be interrupted.*

# X28HC256

## RESETTING SOFTWARE DATA PROTECTION

Figure 8. Reset Software Data Protection Timing Sequence

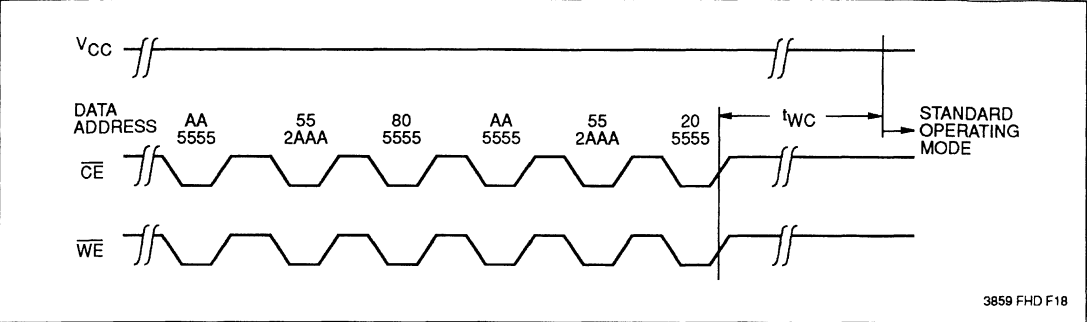
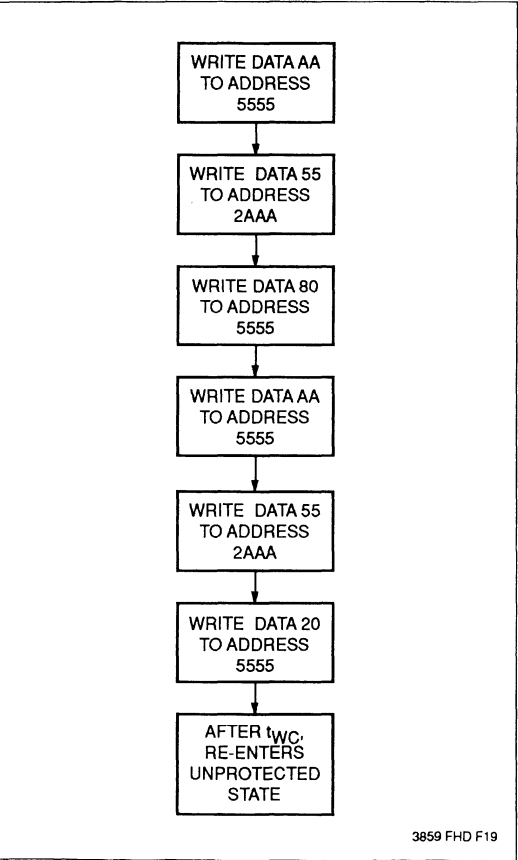


Figure 9. Write Sequence for resetting Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E<sup>2</sup>PROM programmer, the following six step algorithm will reset the internal protection circuit. After t<sub>WC</sub>, the X28HC256 will be in standard operating mode.

*Note: Once initiated, the sequence of write operations should not be interrupted.*

## X28HC256

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### SYSTEM CONSIDERATIONS

Because the X28HC256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28HC256 has two power modes, standby and active, proper decoupling of the memory array is of

prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu\text{F}$  high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7  $\mu\text{F}$  electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.



X28HC256

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X28HC256 .....	−10°C to +85°C
X28HC256I, X28HC256M .....	−65°C to +135°C
Storage Temperature .....	
−65°C to +150°C	
Voltage on any Pin with	
Respect to VSS .....	−1.0V to +7V
D.C. Output Current .....	10 mA
Lead Temperature (Soldering, 10 Seconds) .....	
300°C	

\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

3859 PGM T02

Supply Voltage	Limits
X28HC256	5V ± 10%

3859 PGM T03

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(7)	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Active Current (TTL Inputs)		30	80	mA	$\overline{CE} = \overline{OE} = V_{IL}$ , $\overline{WE} = V_{IH}$ , All I/O's = Open, Address Inputs = .4V/2.4V Levels @ f = 10MHz
I <sub>SB1</sub>	V <sub>CC</sub> Standby Current (TTL Inputs)		1	2	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ , All I/O's = Open, Other Inputs = $V_{IH}$
I <sub>SB2</sub>	V <sub>CC</sub> Standby Current (CMOS Inputs)		200	500	μA	$\overline{CE} = V_{CC} - 0.3V$ , $\overline{OE} = GND$ , All I/Os = Open, Other Inputs = $V_{CC} - 0.3V$
I <sub>LI</sub>	Input Leakage Current			10	μA	$V_{IN} = GND$ to $V_{CC}$
I <sub>LO</sub>	Output Leakage Current			10	μA	$V_{OUT} = GND$ to $V_{CC}$ , $\overline{CE} = V_{IH}$
V <sub>IL</sub> (2)	Input Low Voltage	−1.0		0.8	V	
V <sub>IH</sub> (2)	Input High Voltage	2.0		$V_{CC} + 1.0$	V	
V <sub>OL</sub>	Output Low Voltage			0.4	V	I <sub>OL</sub> = 6mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = −4mA

3859 PGM T04

Notes: (1) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage.  
(2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.

X28HC256

POWER-UP TIMING

Symbol	Parameter	Max.	Units
tPUR <sup>(3)</sup>	Power-Up to Read	100	μs
tPUW <sup>(3)</sup>	Power-Up to Write	5	ms

3859 PGM T05

CAPACITANCE T<sub>A</sub> = 25°C, F = 1.0MHZ, V<sub>CC</sub> = 5V.

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> <sup>(9)</sup>	Input/Output Capacitance	10	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> <sup>(9)</sup>	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

3859 PGM T06

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	10,000		Cycles per Byte
Data Retention	100		Years

3859 PGM T07

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

3859 PGM T08

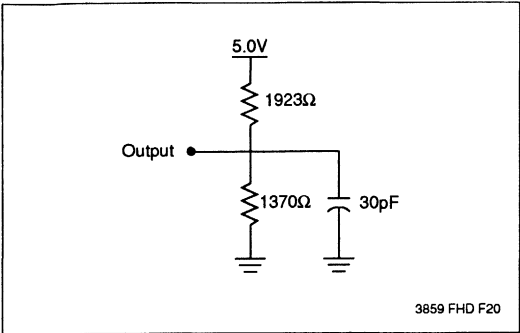
MODE SELECTION

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	I/O	Power
L	L	H	Read	D <sub>OUT</sub>	Active
L	H	L	Write	D <sub>IN</sub>	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3859 PGM T09

Note: (3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



3859 FHD F20

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

# X28HC256

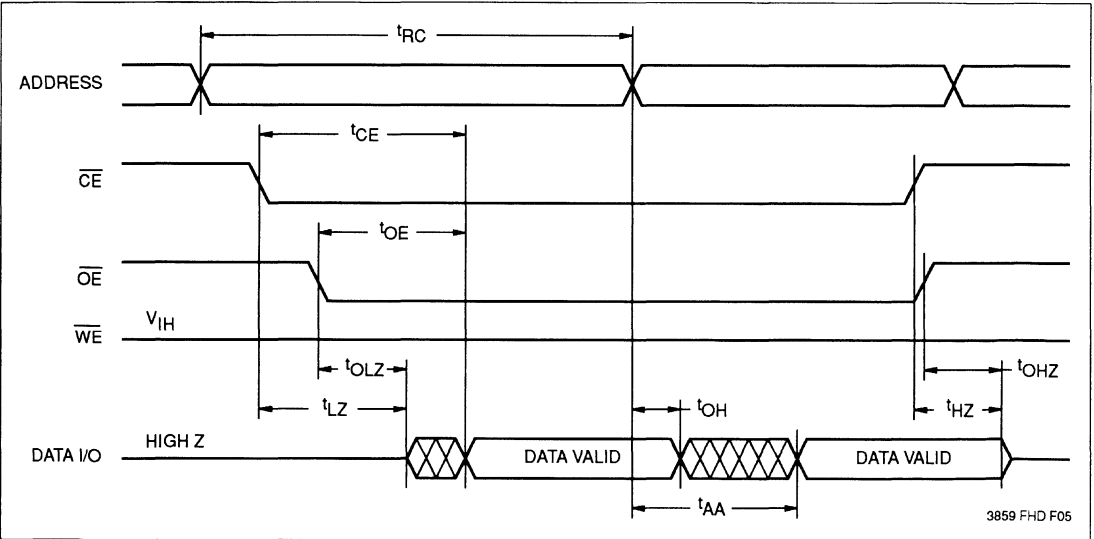
## A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

### Read Cycle Limits

Symbol	Parameter	X28HC256-70		X28HC256-90		X28HC256-12		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}^{(5)}$	Read Cycle Time	70		90		120		ns
$t_{CE}^{(5)}$	Chip Enable Access Time		70		90		120	ns
$t_{AA}^{(5)}$	Address Access Time		70		90		120	ns
$t_{OE}$	Output Enable Access Time		35		40		50	ns
$t_{LZ}^{(4)}$	$\overline{CE}$ Low to Active Output	0		0		0		ns
$t_{OLZ}^{(4)}$	$\overline{OE}$ Low to Active Output	0		0		0		ns
$t_{HZ}^{(4)}$	$\overline{CE}$ High to High Z Output		35		40		50	ns
$t_{OHZ}^{(4)}$	$\overline{OE}$ High to High Z Output		35		40		50	ns
$t_{OH}$	Output Hold From Address Change	0		0		0		ns

3859 PGM T10

### Read Cycle



3859 FHD F05

- Notes:** (4)  $t_{LZ}$  min.,  $t_{HZ}$ ,  $t_{OLZ}$  min. and  $t_{OHZ}$  are periodically sampled and not 100% tested,  $t_{HZ}$  and  $t_{OHZ}$  are measured, with  $CL = 5pF$ , from the point when  $\overline{CE}$ ,  $\overline{OE}$  return high (whichever occurs first) to the time when the outputs are no longer driven.  
(5) For faster 256k products, refer to X28VC256 product line.

X28HC256

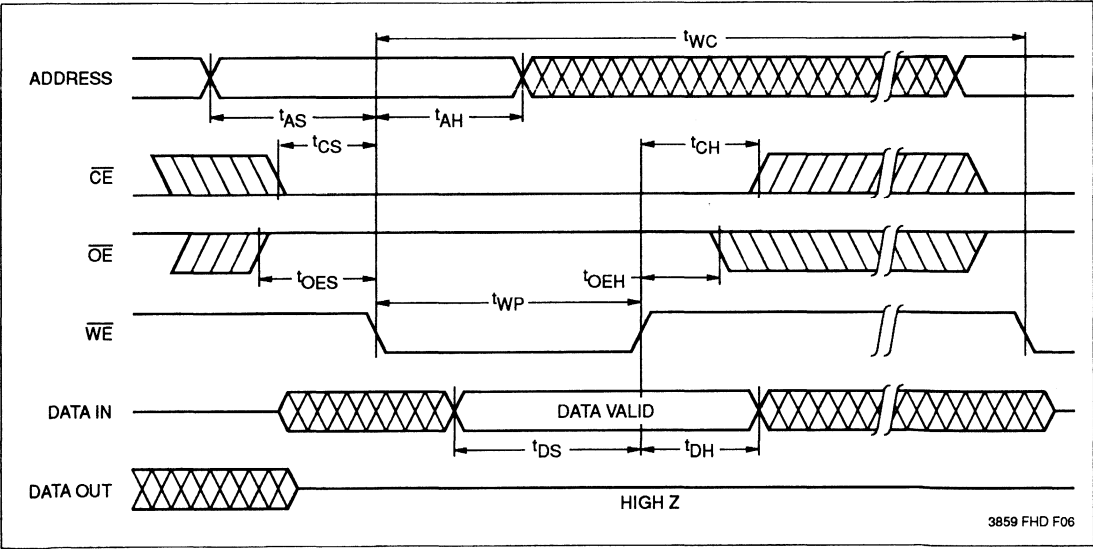
3

Write Cycle Limits

Symbol	Parameter	Min.	Typ. <sup>(6)</sup>	Max.	Units
t <sub>wc</sub> <sup>(7)</sup>	Write Cycle Time		3	5	ms
t <sub>AS</sub>	Address Setup Time	0			ns
t <sub>AH</sub>	Address Hold Time	50			ns
t <sub>CS</sub>	Write Setup Time	0			ns
t <sub>CH</sub>	Write Hold Time	0			ns
t <sub>CW</sub>	CE Pulse Width	50			ns
t <sub>OES</sub>	OE High Setup Time	0			ns
t <sub>OEH</sub>	OE High Hold Time	0			ns
t <sub>WP</sub>	WE Pulse Width	50			ns
t <sub>WPH</sub> <sup>(8)</sup>	WE High Recovery (page write only)	50			ns
t <sub>DS</sub>	Data Setup	50			ns
t <sub>DH</sub>	Data Hold	0			ns
t <sub>DW</sub> <sup>(8)</sup>	Delay to Next Write after polling is true	10			μs
t <sub>BLC</sub>	Byte Load Cycle	0.150		100	μs

3859 PGM T11

WE Controlled Write Cycle

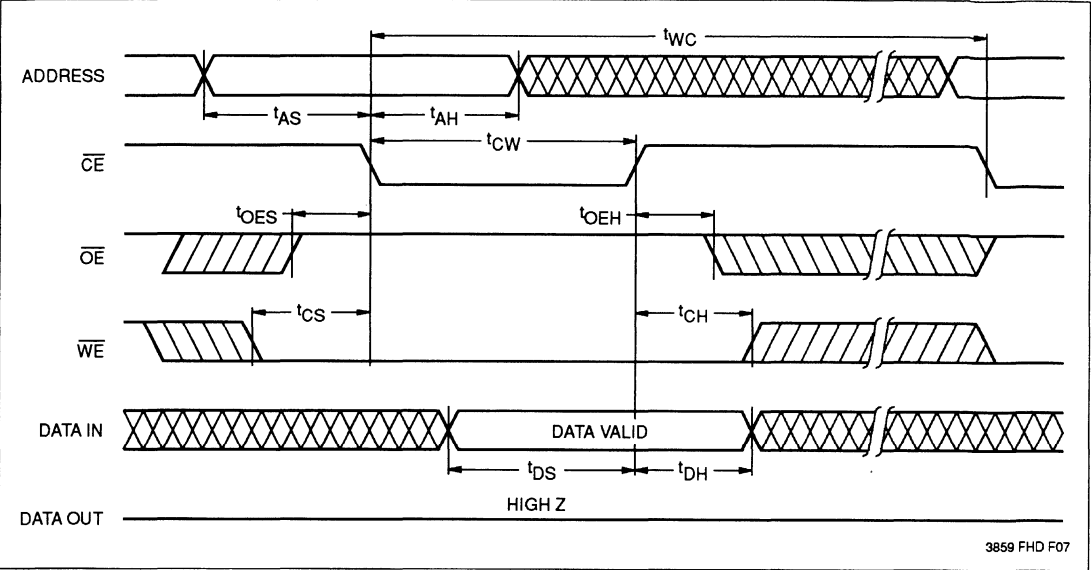


3859 FHD F06

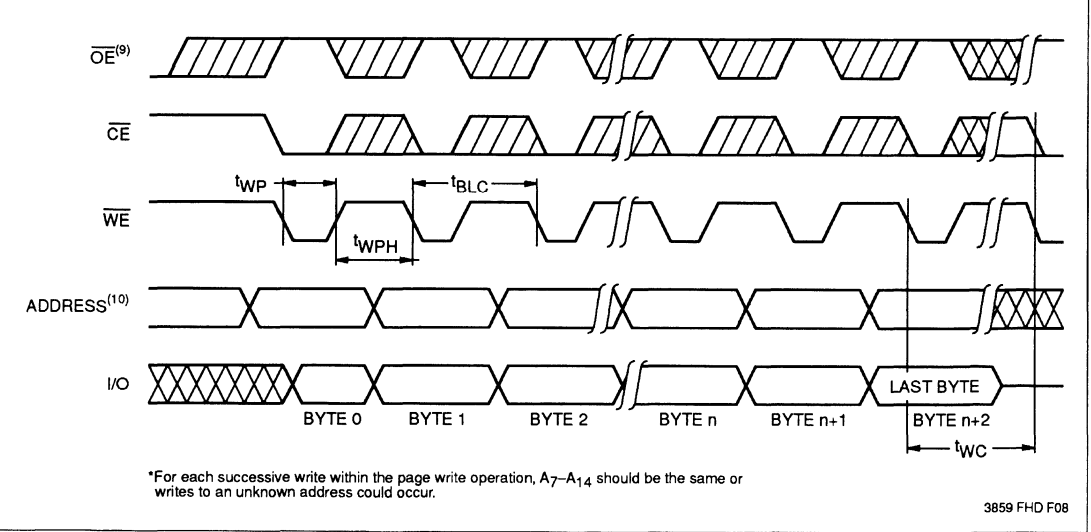
- Notes:** (6) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.  
(7)  $t_{wc}$  is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.  
(8)  $t_{WPH}$  and  $t_{DW}$  are periodically sampled and not 100% tested.

# X28HC256

## CE Controlled Write Cycle



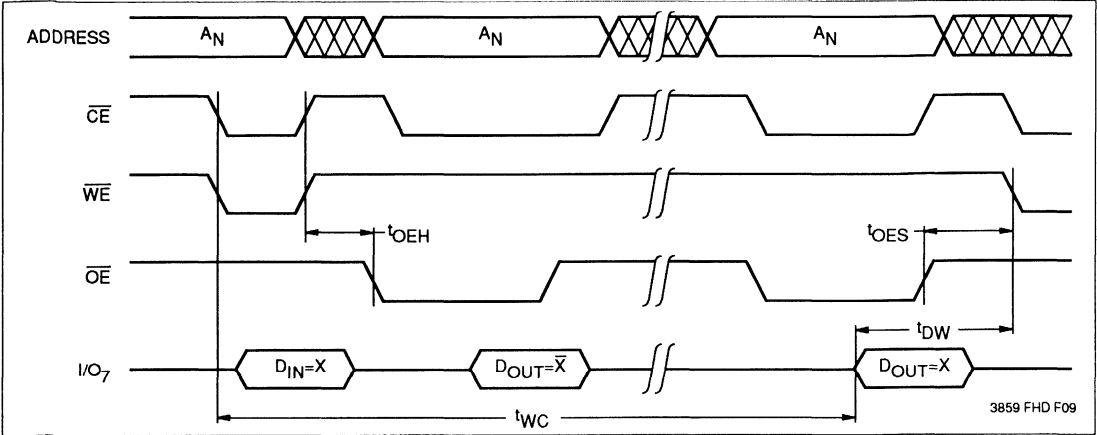
## Page Write Cycle



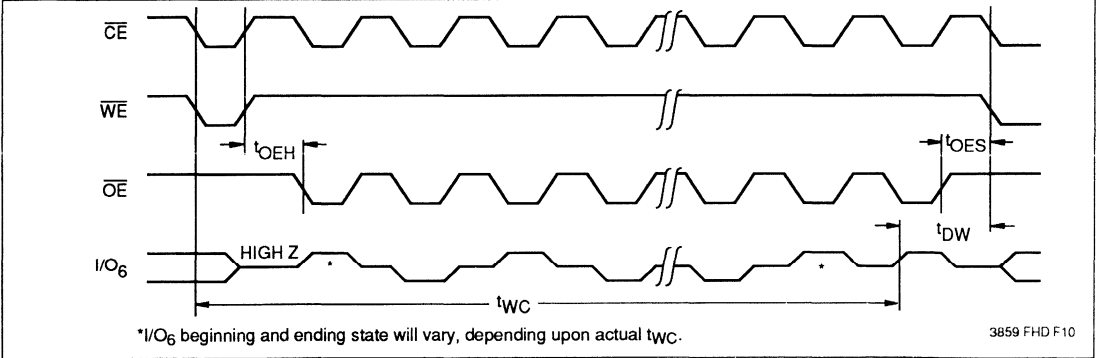
- Notes:**
- (9) Between successive byte writes within a page write operation,  $\overline{OE}$  can be strobed LOW: e.g. this can be done with  $\overline{CE}$  and  $\overline{WE}$  HIGH to fetch data from another memory device within the system for the next write; or with  $\overline{WE}$  HIGH and  $\overline{CE}$  LOW effectively performing a polling operation.
  - (10) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the  $\overline{CE}$  or  $\overline{WE}$  controlled write cycle timing.

X28HC256

DATA Polling Timing Diagram<sup>(11)</sup>



Toggle Bit Timing Diagram<sup>(11)</sup>



**Note:** (11) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

**X28HC256**

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**NOTES**



## Advance Information Very High Speed

256K

X28VC256

32K x 8 Bit

### 5 Volt, Byte Alterable E<sup>2</sup>PROM

#### FEATURES

- Access Time: 45 ns
- SIMPLE Byte and Page Write
  - Single 5 Volt Supply
  - No External High Voltages or V<sub>pp</sub> Control Circuits
  - Self Timed
    - No Erase Before Write
    - No Complex Programming Algorithms
    - No Overerase Problem
- Low Power CMOS:
  - Active: 80mA
  - Standby: 10mA
- Software Data Protection
  - Protects Data Against System Level Inadvertent Writes
- High Speed Page Write Capability
- Highly Reliable Direct Write™ Cell
  - Endurance: 10,000 Write Cycles
  - Data Retention: 100 Years
- Early End of Write Detection
  - DATA Polling
  - Toggle Bit Polling

#### DESCRIPTION

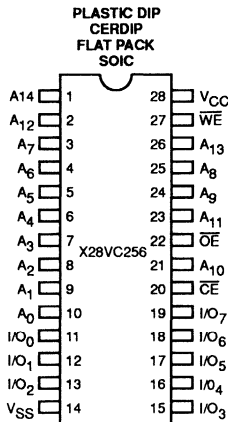
The X28VC256 is a second generation high performance CMOS 32K x 8 E<sup>2</sup>PROM. It is fabricated with Xicor's proprietary, textured poly floating gate technology, providing a highly reliable 5 Volt only nonvolatile memory.

The X28VC256 supports a 128-byte page write operation, effectively providing a 24μs/byte write cycle and enabling the entire memory to be typically rewritten in less than 0.8 seconds. The X28VC256 also features DATA Polling and Toggle Bit polling, two methods of providing early end of write detection. The X28VC256 also supports the JEDEC standard Software Data Protection feature for protecting against inadvertent writes during power-up and power-down.

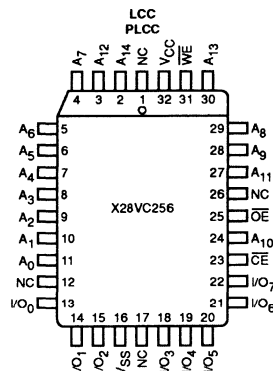
Endurance for the X28VC256 is specified as a minimum 10,000 write cycles per byte and an inherent data retention of 100 years.

3

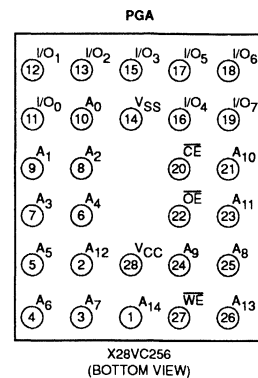
#### PIN CONFIGURATION



3869 FHD F02



3869 FHD F03



3869 FHD F04



# X28VC256

## PIN DESCRIPTIONS

### Addresses (A<sub>0</sub>–A<sub>14</sub>)

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{\text{CE}}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{\text{CE}}$  is HIGH, power consumption is reduced.

### Output Enable ( $\overline{\text{OE}}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

### Data In/Data Out (I/O<sub>0</sub>–I/O<sub>7</sub>)

Data is written to or read from the X28VC256 through the I/O pins.

### Write Enable ( $\overline{\text{WE}}$ )

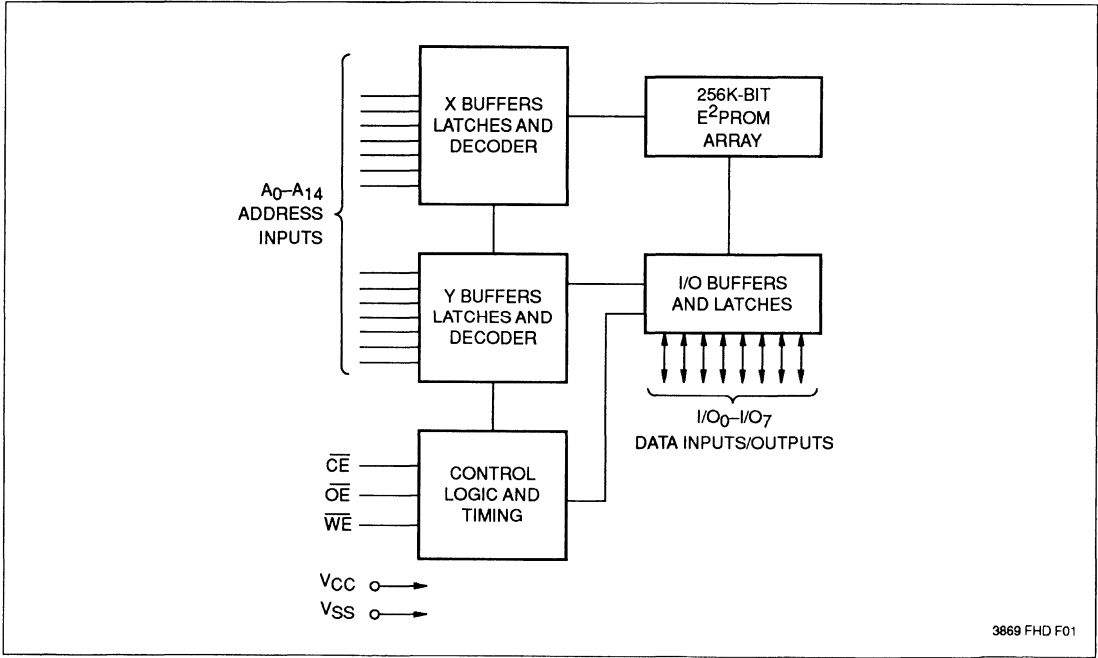
The Write Enable input controls the writing of data to the X28VC256.

## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>14</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

3869 PGM T01

## FUNCTIONAL DIAGRAM



3869 FHD F01

# X28VC256

## DEVICE OPERATION

### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The X28VC256 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3 ms.

### Page Write Operation

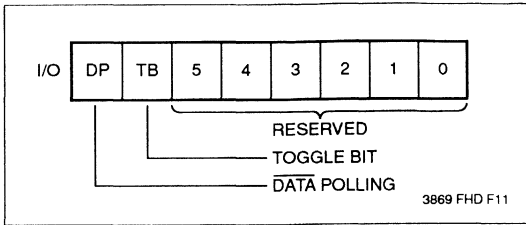
The page write feature of the X28VC256 allows the entire memory to be written in typically 0.8 seconds. Page write allows up to one hundred twenty-eight bytes of data to be consecutively written to the X28VC256 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address ( $A_7$  through  $A_{14}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twenty-seven bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100  $\mu$ s.

### Write Operation Status Bits

The X28VC256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



### DATA Polling (I/O<sub>7</sub>)

The X28VC256 features  $\overline{DATA}$  Polling as a method to indicate to the host system that the byte write or page write cycle has completed.  $\overline{DATA}$  Polling allows a simple bit test operation to determine the status of the X28VC256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O<sub>7</sub> (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O<sub>7</sub> will reflect true data.

### Toggle Bit (I/O<sub>6</sub>)

The X28VC256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O<sub>6</sub> will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read and write operations.

# X28VC256

## DATA POLLING I/O<sub>7</sub>

Figure 2. DATA Polling Bus Sequence

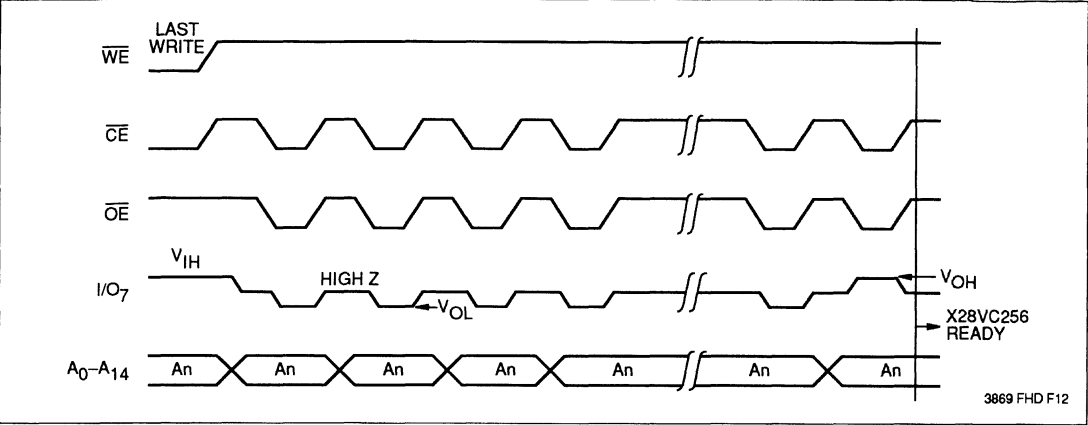
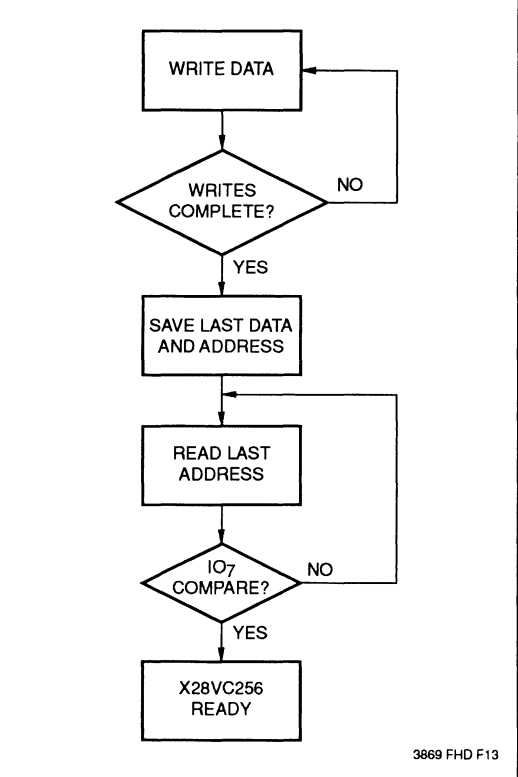


Figure 3. DATA Polling Software Flow



DATA Polling can effectively halve the time for writing to the X28VC256. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

X28VC256

THE TOGGLE BIT I/O<sub>6</sub>

Figure 4. Toggle Bit Bus Sequence

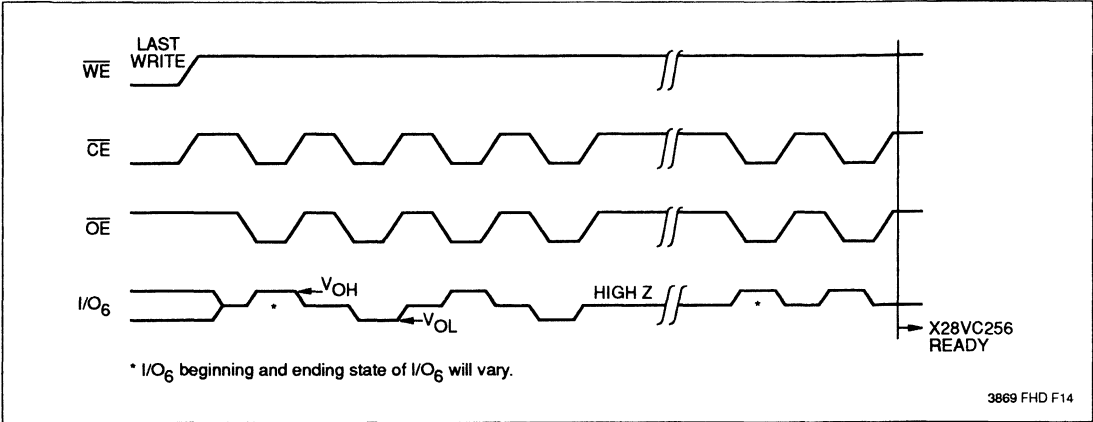
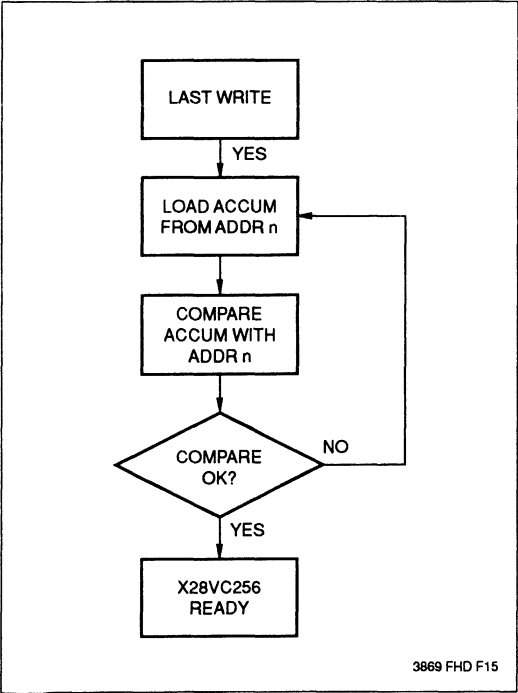


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28VC256 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

## X28VC256

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### HARDWARE DATA PROTECTION

The X28VC256 provides two hardware features that protect nonvolatile data from inadvertent writes.

- Default  $V_{CC}$  Sense—All write functions are inhibited when  $V_{CC}$  is  $\leq 3.5V$  typically.
- Write Inhibit—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH, or  $\overline{CE}$  HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

### SOFTWARE DATA PROTECTION

The X28VC256 offers a software controlled data protection feature. The X28VC256 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/down operations through the use of external circuits. The host would then have open read and write access of the device once  $V_{CC}$  was stable.

The X28VC256 can be automatically protected during power-up and power-down without the need for external

circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28VC256 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

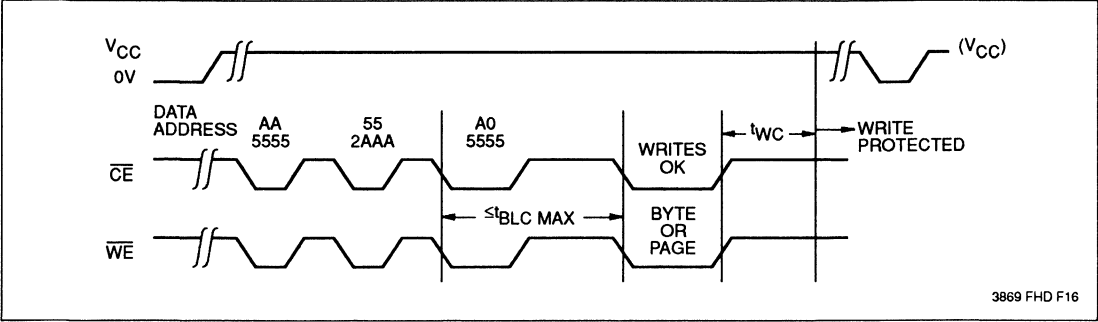
### SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three byte sequence opens the page write window enabling the host to write from one to one hundred twenty-eight bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

X28VC256

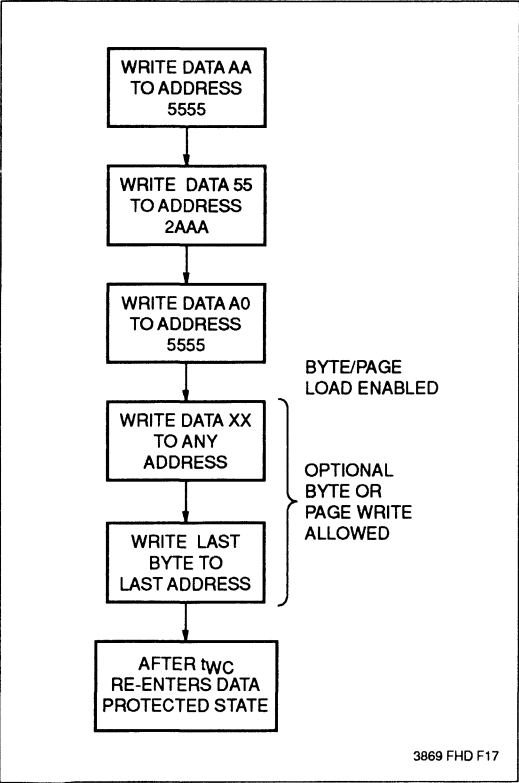
SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write



3

Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28VC256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28VC256 will be write protected during power-down and after any subsequent power-up.

*Note: Once initiated, the sequence of write operations should not be interrupted.*

X28VC256

RESETTING SOFTWARE DATA PROTECTION

Figure 8. Reset Software Data Protection Timing Sequence

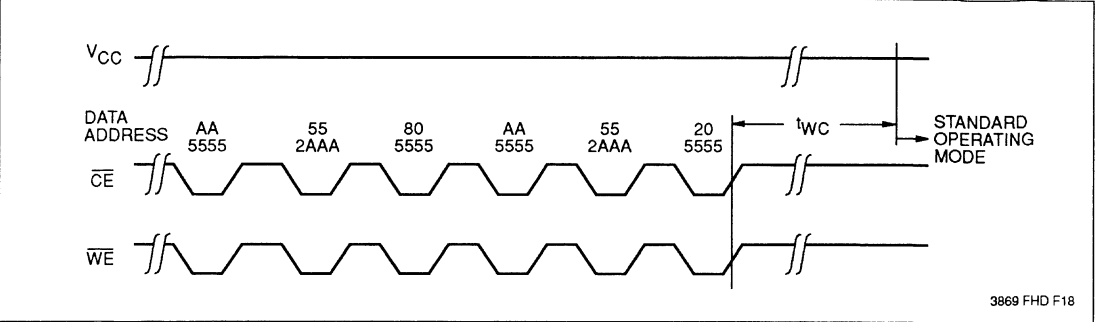
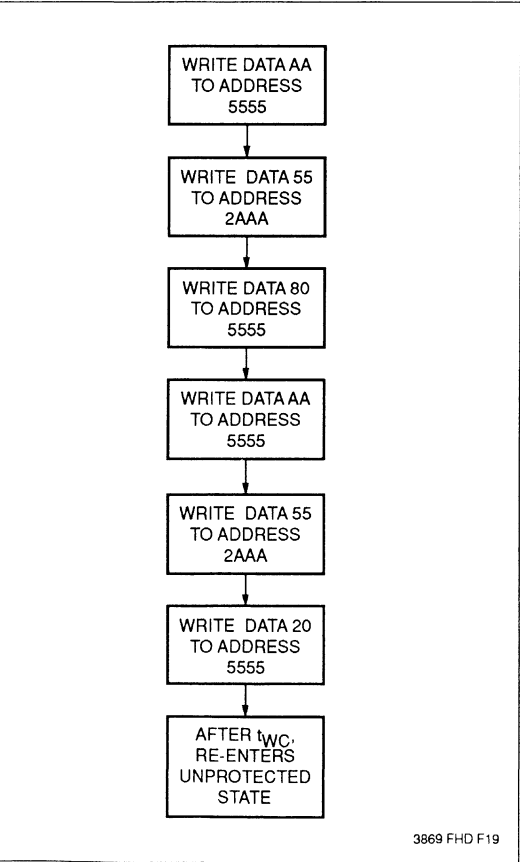


Figure 9. Write Sequence for Resetting Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E<sup>2</sup>PROM programmer, the following six step algorithm will reset the internal protection circuit. After  $t_{wc}$ , the X28VC256 will be in standard operating mode.

*Note:* Once initiated, the sequence of write operations should not be interrupted.

## X28VC256

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### SYSTEM CONSIDERATIONS

Because the X28VC256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28VC256 has two power modes, standby and active, proper decoupling of the memory array is of

prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu\text{F}$  high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7  $\mu\text{F}$  electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.



X28VC256

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias  
X28VC256 .....-10°C to +85°C  
X28VC256I, X28VC256M .....-65°C to +135°C  
Storage Temperature .....-65°C to +150°C  
Voltage on any Pin with  
Respect to V<sub>SS</sub> .....-1.0V to +7V  
D.C. Output Current ..... 10 mA  
Lead Temperature (Soldering, 10 Seconds) .....300°C

\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

3869 PGM T02

Supply Voltage	Limits
X28VC256	5V ± 10%

3869 PGM T03

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Active Current		30	80	mA	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ , All I/O's = Open, Address Inputs = 0.4V/2.4V Levels @ f = 10MHz
I <sub>SB</sub>	V <sub>CC</sub> Standby Current		10	25	mA	$\overline{CE} = V_{IH}, \overline{OE} = V_{IL}$ , All I/O's = Open, Other Inputs = V <sub>IH</sub>
I <sub>LI</sub>	Input Leakage Current			10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current			10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , $\overline{CE} = V_{IH}$
V <sub>IL</sub> (2)	Input Low Voltage	-1.0		0.8	V	
V <sub>IH</sub> (2)	Input High Voltage	2.0		V <sub>CC</sub> + 1.0	V	
V <sub>OL</sub>	Output Low Voltage			0.4	V	I <sub>OL</sub> = 6mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = -4mA

3869 PGM T04

Notes: (1) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage.  
(2) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.

# X28VC256

## POWER-UP TIMING

Symbol	Parameter	Max.	Units
t <sub>PUR</sub> (3)	Power-Up to Read	100	μs
t <sub>PUW</sub> (3)	Power-Up to Write	5	ms

3869 PGM T05

CAPACITANCE T<sub>A</sub> = 25°C, F = 1.0MHZ, V<sub>CC</sub> = 5V.

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (3)	Input/Output Capacitance	10	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (3)	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

3869 PGM T06

3

## ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	10,000		Cycles per Byte
Data Retention	100		Years

3869 PGM T07

## A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

3869 PGM T08

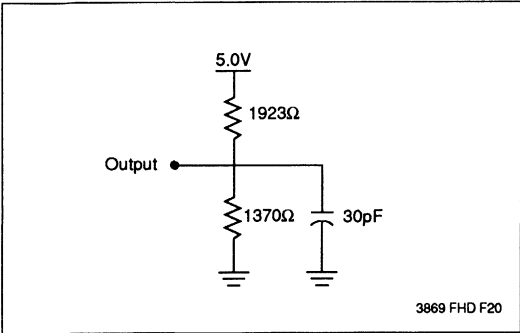
## MODE SELECTION

CE	OE	WE	Mode	I/O	Power
L	L	H	Read	DOUT	Active
L	H	L	Write	DIN	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3869 PGM T09

Note: (3) This parameter is periodically sampled and not 100% tested.

## EQUIVALENT A.C. LOAD CIRCUIT



## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

# X28VC256

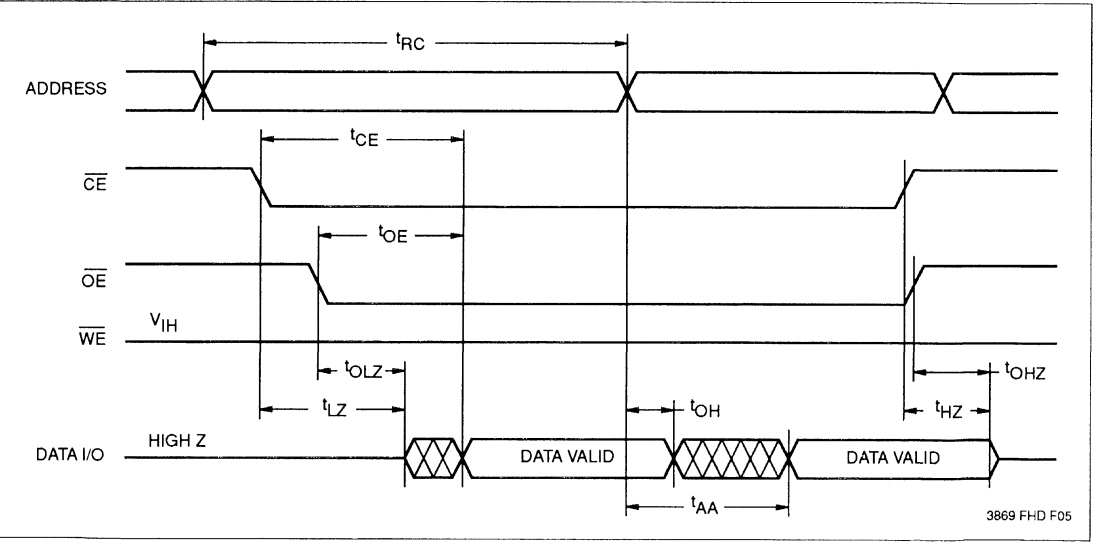
## A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

### Read Cycle Limits

Symbol	Parameter	X28VC256-45 -40°C to 85°C		X28VC256-55 -55°C to 125°C		X28VC256-70 -55°C to 125°C		X28VC256-90 -55°C to 125°C		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	45		55		70		90		ns
t <sub>CE</sub>	Chip Enable Access Time		45		55		70		90	ns
t <sub>AA</sub>	Address Access Time		45		55		70		90	ns
t <sub>OE</sub>	Output Enable Access Time		30		30		35		40	ns
t <sub>LZ</sub> (4)	$\overline{CE}$ Low to Active Output	0		0		0		0		ns
t <sub>OLZ</sub> (4)	$\overline{OE}$ Low to Active Output	0		0		0		0		ns
t <sub>HZ</sub> (4)	$\overline{CE}$ High to High Z Output		30		30		35		40	ns
t <sub>OHZ</sub> (4)	$\overline{OE}$ High to High Z Output		30		30		35		40	ns
t <sub>OH</sub>	Output Hold From Address Change	0		0		0		0		ns

3869 PGM T10

### Read Cycle



3869 FHD F05

**Notes:** (4)  $t_{LZ}$  min.,  $t_{HZ}$ ,  $t_{OLZ}$  min. and  $t_{OHZ}$  are periodically sampled and not 100% tested,  $t_{HZ}$  and  $t_{OHZ}$  are measured, with  $CL = 5pF$ , from the point when  $\overline{CE}$ ,  $\overline{OE}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

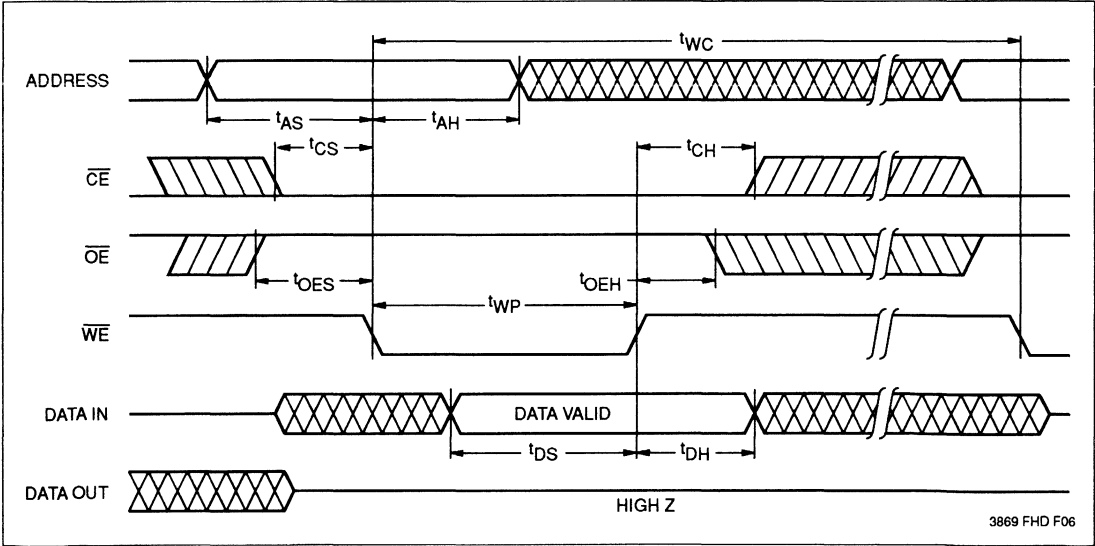
X28VC256

Write Cycle Limits

Symbol	Parameter	Min.	Typ. <sup>(5)</sup>	Max.	Units
t <sub>WC</sub> <sup>(6)</sup>	Write Cycle Time		3	5	ms
t <sub>AS</sub>	Address Setup Time	0			ns
t <sub>AH</sub>	Address Hold Time	50			ns
t <sub>CS</sub>	Write Setup Time	0			ns
t <sub>CH</sub>	Write Hold Time	0			ns
t <sub>CW</sub>	CE Pulse Width	50			ns
t <sub>OES</sub>	OE High Setup Time	0			ns
t <sub>OEH</sub>	OE High Hold Time	0			ns
t <sub>WP</sub>	WE Pulse Width	50			ns
t <sub>WPH</sub> <sup>(7)</sup>	WE High Recovery (page write only)	50			ns
t <sub>DS</sub>	Data Setup	50			ns
t <sub>DH</sub>	Data Hold	0			ns
t <sub>DW</sub> <sup>(7)</sup>	Delay to Next Write after polling is true	10			μs
t <sub>BLC</sub>	Byte Load Cycle	0.150		100	μs

3869 PGM T11

WE Controlled Write Cycle

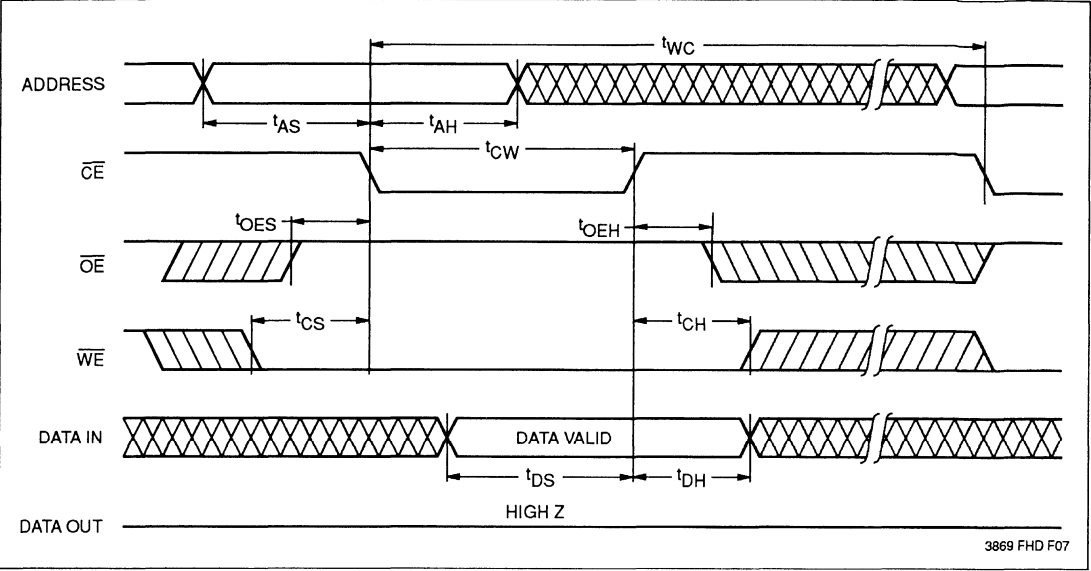


3869 FHD F06

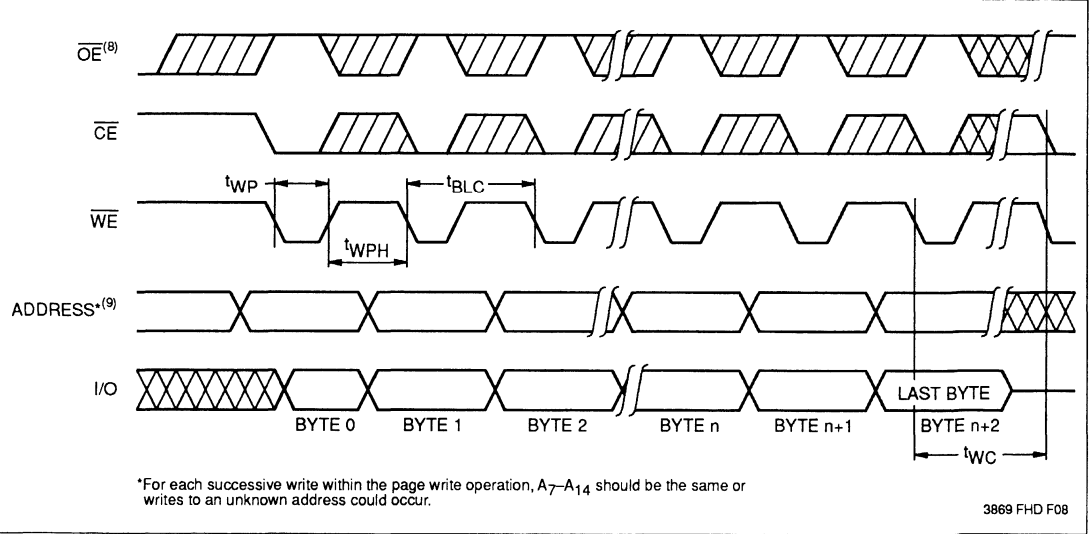
- Notes: (5) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.  
(6)  $t_{WC}$  is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.  
(7)  $t_{WPH}$  and  $t_{PW}$  are periodically sampled and not 100% tested.

# X28VC256

## CE Controlled Write Cycle



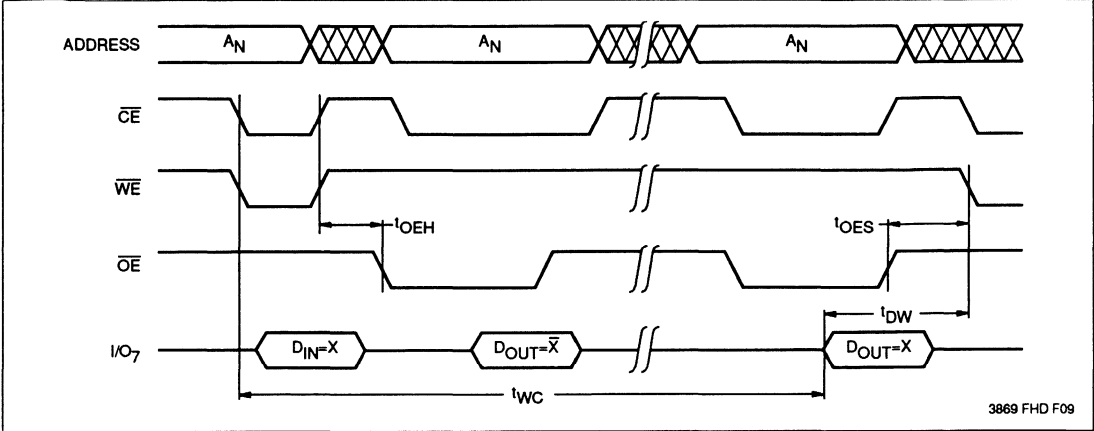
## Page Write Cycle



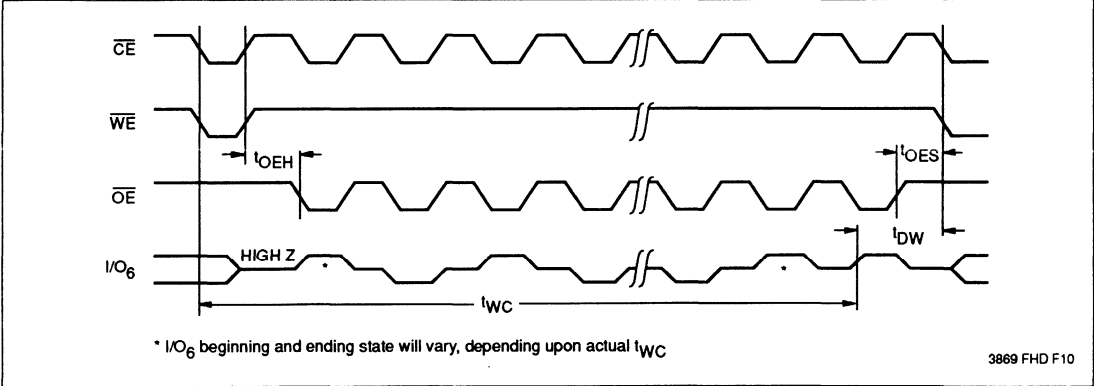
- Notes:** (8) Between successive byte writes within a page write operation,  $\overline{OE}$  can be strobed LOW: e.g. this can be done with  $\overline{CE}$  and  $\overline{WE}$  HIGH to fetch data from another memory device within the system for the next write; or with  $\overline{WE}$  HIGH and  $\overline{CE}$  LOW effectively performing a polling operation.
- (9) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the  $\overline{CE}$  or  $\overline{WE}$  controlled write cycle timing.

X28VC256

DATA Polling Timing Diagram<sup>(10)</sup>



Toggle Bit Timing Diagram<sup>(10)</sup>



**Note:** (10) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

**X28VC256**

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**NOTES**



## Fact Sheet

256K

X28TC256

32K x 8

## Fast Column Access E<sup>2</sup>PROM

### FEATURES

- 35ns Access Time
  - Within 64-Byte Page Boundaries
  - Page Crossing Status Output— $\overline{\text{WAIT}}$
- 5 Volt Byte and Page Alterable
  - Write From One to Sixty-Four Bytes
  - Write Time—5ms Max.
  - Complete Memory Rewrite: 2.5 Sec. Max.
- Early End of Write Detection
  - $\overline{\text{DATA}}$  Polling
  - Toggle Bit Polling
  - Minimize Memory Rewrite: 1.5 Sec. Typical
- Software Data Protection
- Highly Reliable Direct Write™ Cell
  - Endurance: 10,000 Cycles Per Byte
  - Data Retention: 100 years

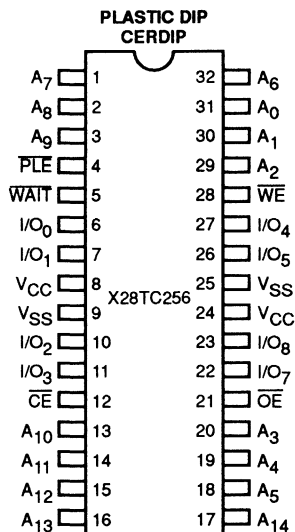
### DESCRIPTION

The X28TC256 is a high speed 32K x 8, 5 volt byte alterable nonvolatile memory. It is specially designed to support high speed microprocessors by providing a fast column access time of 35ns for each byte on a 64-byte page. The access time when changing pages will be 150ns maximum. The X28TC256 automatically generates a  $\overline{\text{WAIT}}$  signal when page boundaries are crossed.

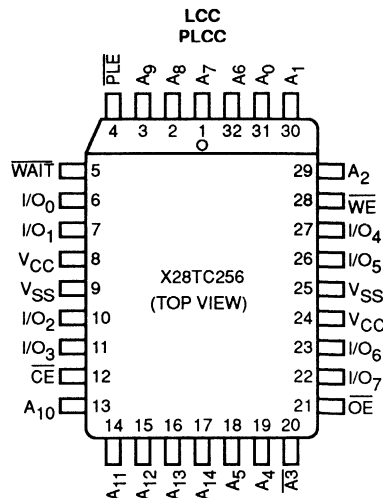
The X28TC256 also features  $\overline{\text{DATA}}$  Polling and toggle bit polling methods for detecting early end of write. Using either of these polling features, the entire memory can typically be rewritten in 1.5 seconds.

3

### PIN CONFIGURATION



3860 FHD F02

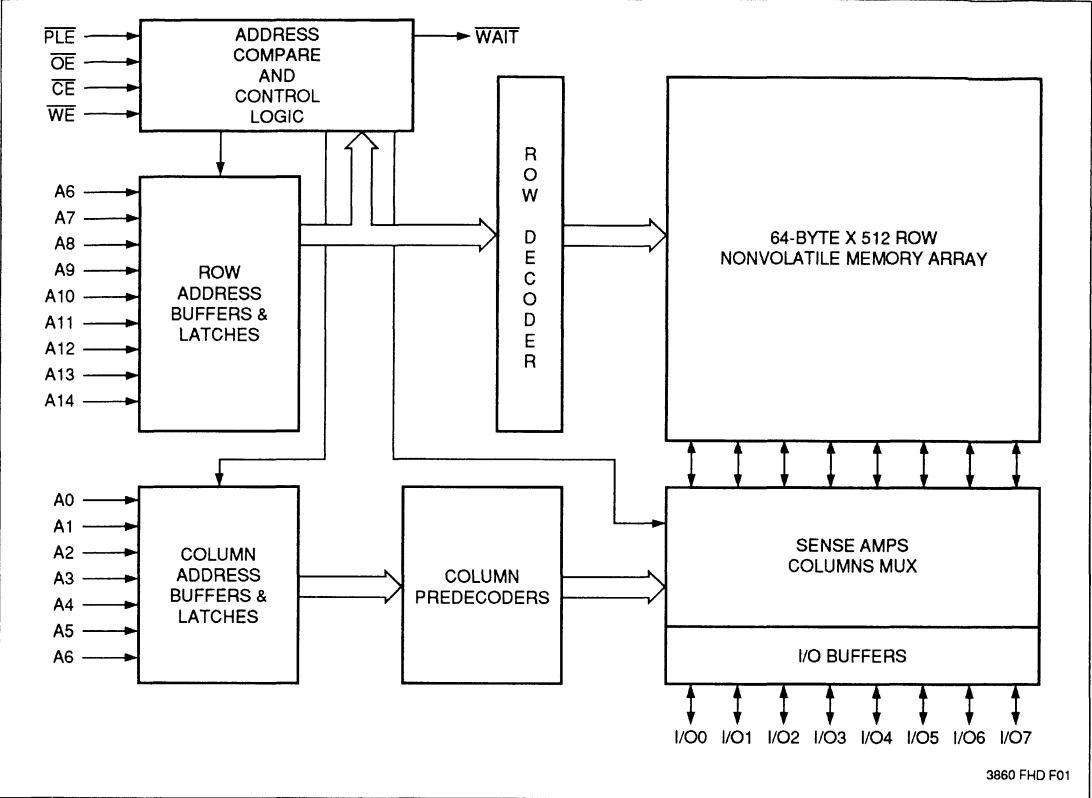


3860 FHD F03



X28TC256

FUNCTIONAL DIAGRAM





512K

X28C512

64K x 8 Bit

5 Volt, Byte Alterable E<sup>2</sup>PROM

## FEATURES

- Access Time: 120 ns
- SIMPLE Byte and Page Write
  - Single 5 Volt Supply
  - No External High Voltages or V<sub>PP</sub> Control Circuits
  - Self Timed
  - No Erase Before Write
  - No Complex Programming Algorithms
  - No Overerase Problem
- Low Power CMOS:
  - Active: 50mA
  - Standby: 500 $\mu$ A
- Software Data Protection
  - Protects Data Against System Level Inadvertent Writes
- High Speed Page Write Capability
- Highly Reliable Direct Write™ Cell
  - Endurance: 10,000 Write Cycles
  - Data Retention: 100 Years
- Early End of Write Detection
  - DATA Polling
  - Toggle Bit Polling

## • Two PLCC and LCC Pinouts

- X28C512
- X28C010 E<sup>2</sup>PROM Pin Compatible
- X28C513
- Compatible with Lower Density E<sup>2</sup>PROMs

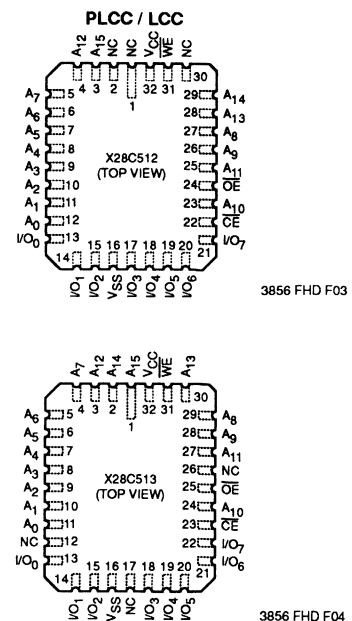
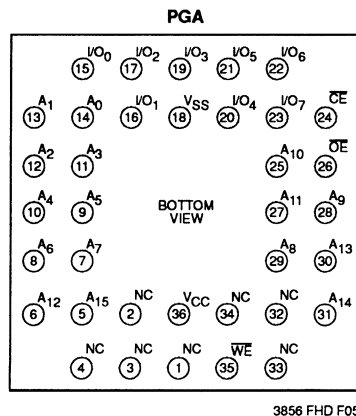
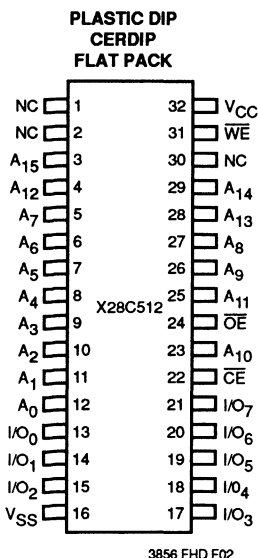
## DESCRIPTION

The X28C512 is an 64K x 8 E<sup>2</sup>PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C512 is a 5V only device. The X28C512 features the JEDEC approved pinout for bytewise memories, compatible with industry standard EPROMs.

The X28C512 supports a 128-byte page write operation, effectively providing a 39  $\mu$ s/byte write cycle and enabling the entire memory to be written in less than 2.5 seconds. The X28C512 also features DATA Polling and Toggle Bit testing, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28C512 supports the Software Data Protection option.

3

## PIN CONFIGURATION



# X28C512

## PIN DESCRIPTIONS

### Addresses (A<sub>0</sub>–A<sub>15</sub>)

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{\text{CE}}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{\text{CE}}$  is HIGH, power consumption is reduced.

### Output Enable ( $\overline{\text{OE}}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

### Data In/Data Out (I/O<sub>0</sub>–I/O<sub>7</sub>)

Data is written to or read from the X28C512 through the I/O pins.

### Write Enable ( $\overline{\text{WE}}$ )

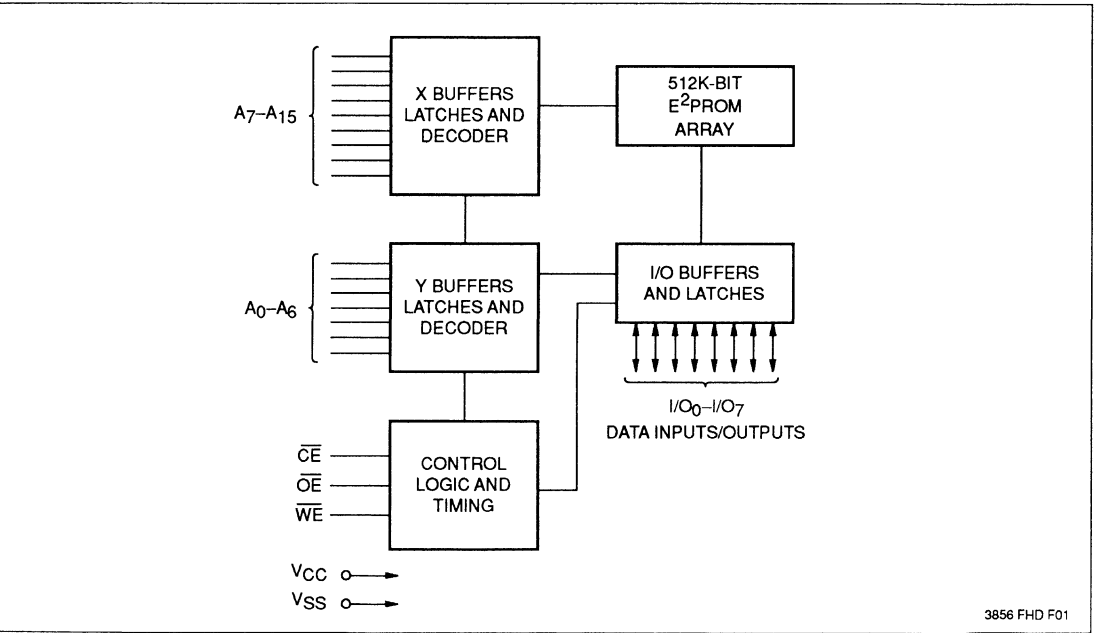
The Write Enable input controls the writing of data to the X28C512.

## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>15</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

3856 PGM T01

## FUNCTIONAL DIAGRAM



3856 FHD F01

# X28C512

## DEVICE OPERATION

### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The X28C512 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

### Page Write Operation

The page write feature of the X28C512 allows the entire memory to be written in 2.5 seconds. Page write allows two to one hundred twenty-eight bytes of data to be consecutively written to the X28C512 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address ( $A_7$  through  $A_{15}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

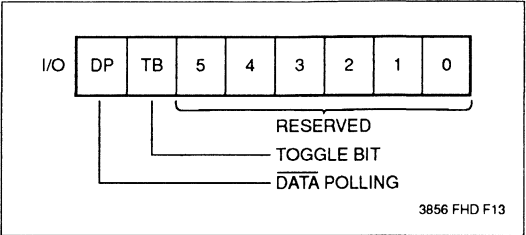
The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twenty-seven bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effec-

tively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100  $\mu$ s.

### Write Operation Status Bits

The X28C512 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



3

### DATA Polling (I/O<sub>7</sub>)

The X28C512 features  $\overline{DATA}$  Polling as a method to indicate to the host system that the byte write or page write cycle has completed.  $\overline{DATA}$  Polling allows a simple bit test operation to determine the status of the X28C512, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O<sub>7</sub> (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O<sub>7</sub> will reflect true data.

### Toggle Bit (I/O<sub>6</sub>)

The X28C512 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O<sub>6</sub> will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

# X28C512

## DATA Polling I/O<sub>7</sub>

Figure 2a. DATA Polling Bus Sequence

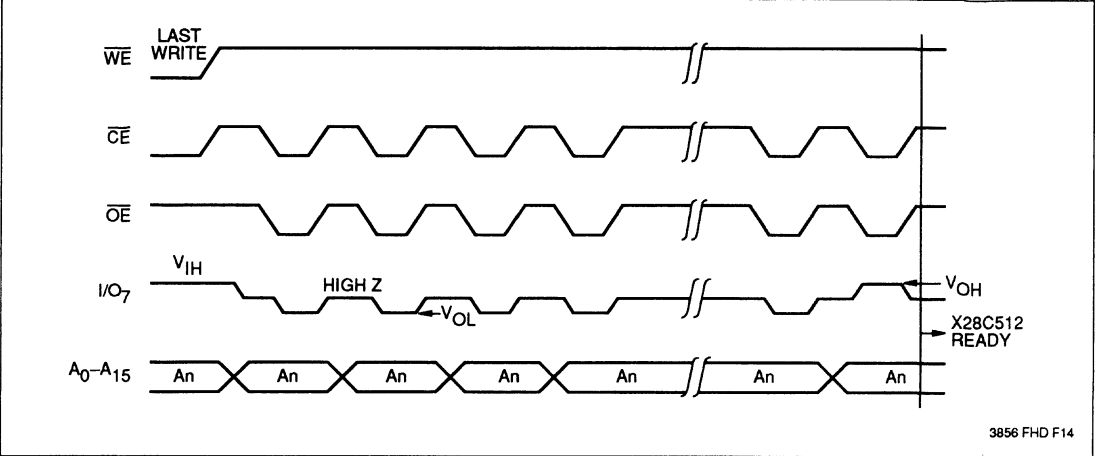
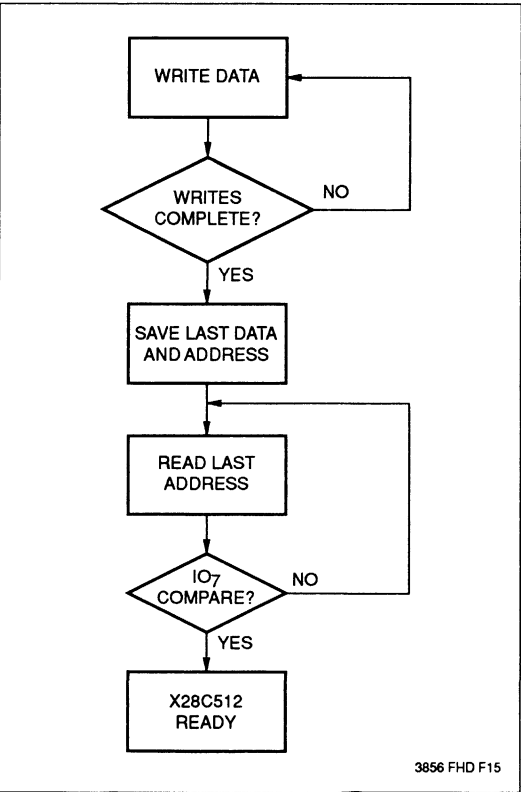


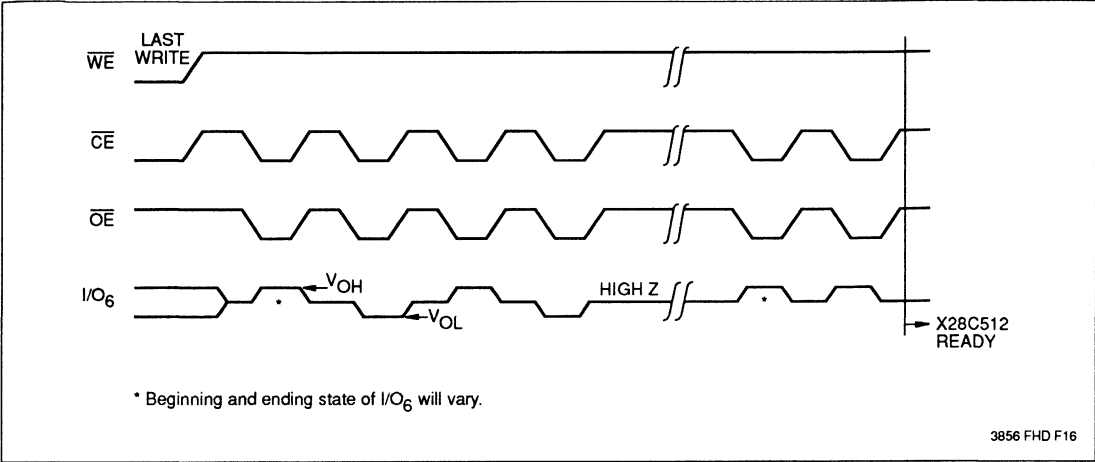
Figure 2b. DATA Polling Software Flow



DATA Polling can effectively halve the time for writing to the X28C512. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

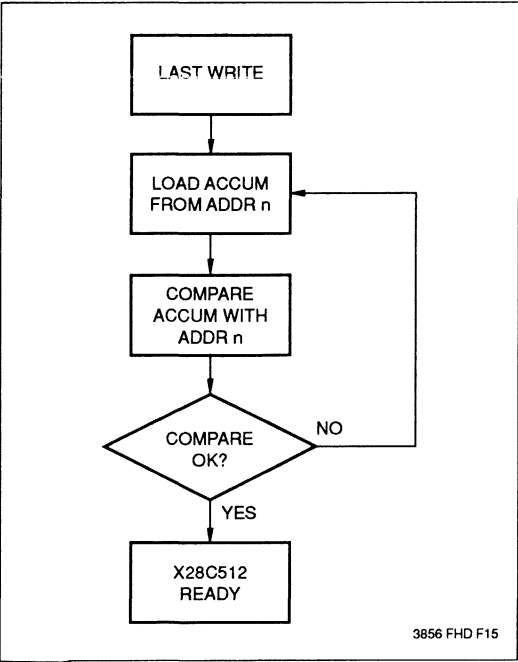
# X28C512

The Toggle Bit I/O<sub>6</sub>  
Figure 3a. Toggle Bit Bus Sequence



3

Figure 3b. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28C512 memories that is frequently updated. Toggle Bit testing can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.

## X28C512

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### HARDWARE DATA PROTECTION

The X28C512 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A  $\overline{WE}$  pulse typically less than 10 ns will not initiate a write cycle.
- Default  $V_{CC}$  Sense—All write functions are inhibited when  $V_{CC}$  is  $\leq 3.6V$ .
- Write Inhibit—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH, or  $\overline{CE}$  HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity. Write cycle timing specifications must be observed concurrently.

### SOFTWARE DATA PROTECTION

The X28C512 offers a software controlled data protection feature. The X28C512 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once  $V_{CC}$  was stable.

The X28C512 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C512 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device. Note: The data in the three byte enable sequence is not written to the memory array.

### SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to one hundred twenty-eight bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

X28C512

Software Data Protection

Figure 4a. Timing Sequence—Software Data Protect Enable Sequence followed by Byte or Page Write

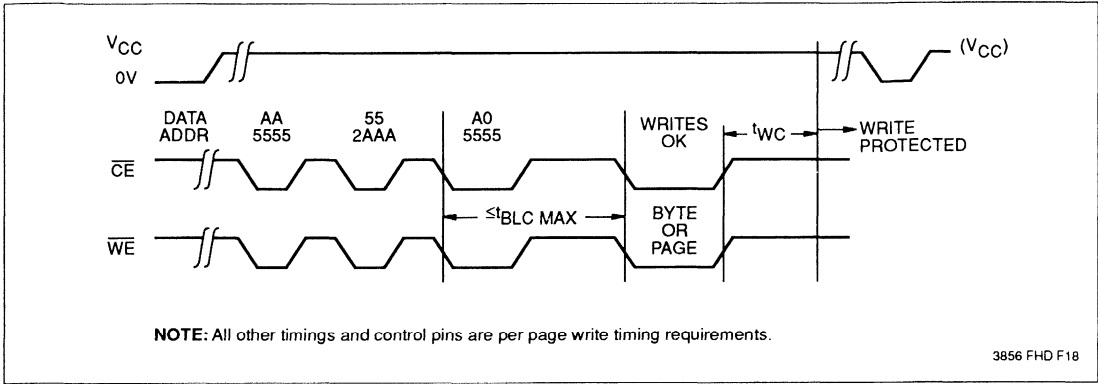
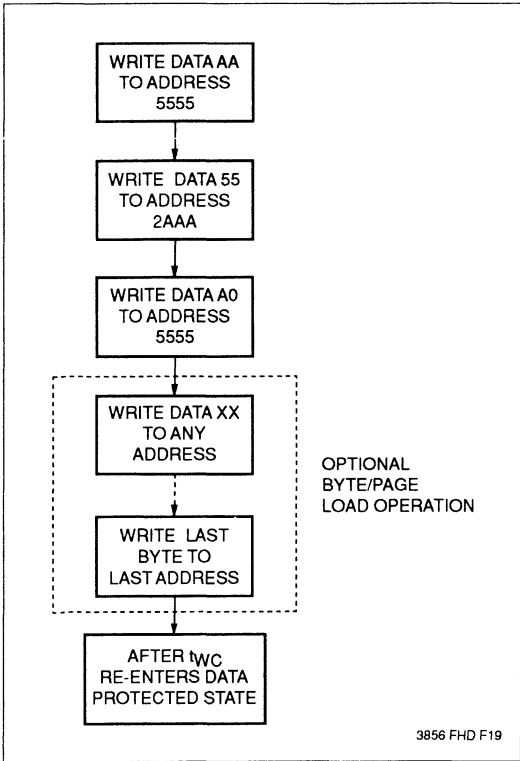


Figure 4b. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C512 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C512 will be write protected during power-down and after any subsequent power-up. The state of  $A_{15}$  while executing the algorithm is don't care.

*Note: Once initiated, the sequence of write operations should not be interrupted.*



# X28C512

Resetting Software Data Protection  
Figure 5a. Reset Software Data Protection Timing Sequence

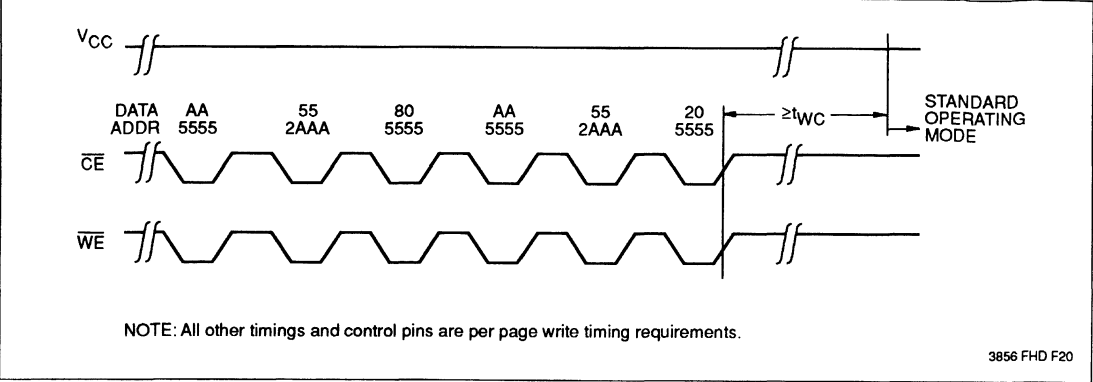
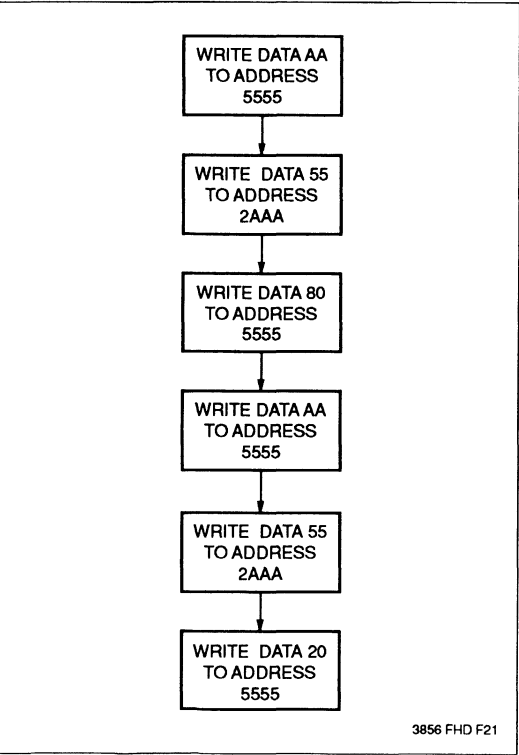


Figure 5b. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E2PROM programmer, the following six step algorithm will reset the internal protection circuit. After  $t_{WC}$ , the X28C512 will be in standard operating mode.

*Note: Once initiated, the sequence of write operations should not be interrupted.*

## X28C512

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### SYSTEM CONSIDERATIONS

Because the X28C512 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C512 has two power modes, standby and active, proper decoupling of the memory array is of

prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu\text{F}$  high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7  $\mu\text{F}$  electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

# X28C512

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X28C512 .....	-10°C to +85°C
X28C512I .....	-65°C to +135°C
X28C512M .....	-65°C to +135°C
Storage Temperature .....	
-65°C to +150°C	
Voltage on any Pin with	
Respect to Ground .....	
-1.0V to +7.0V	
D.C. Output Current .....	
5 mA	
Lead Temperature	
(Soldering, 10 Seconds) .....	
300°C	

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMEND OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

3826 PGM T02

Supply Voltage	Limits
X28C512	5V ±10%

3826 PGM T03

## D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Current (Active) (TTL Inputs)		50	mA	CE = OE = V <sub>IL</sub> , WE = V <sub>IH</sub> , All I/O's = Open, Address Inputs = .4V/2.4V Levels @ f = 5MHz
I <sub>SB1</sub>	V <sub>CC</sub> Current (Standby) (TTL Inputs)		3	mA	CE = V <sub>IH</sub> , OE = V <sub>IL</sub> , All I/O's = Open, Other Inputs = V <sub>CC</sub>
I <sub>SB2</sub>	V <sub>CC</sub> Current (Standby) (CMOS Inputs)		500	µA	CE = V <sub>CC</sub> - 0.3V, OE = V <sub>IL</sub> , All I/O's = Open, Other Inputs = V <sub>CC</sub>
I <sub>LI</sub>	Input Leakage Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , CE = V <sub>IH</sub>
V <sub>IL</sub> (1)	Input Low Voltage	-1.0	0.8	V	
V <sub>IH</sub> (1)	Input High Voltage	2.0	V <sub>CC</sub> + 1.0	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -400 µA

3856 PGM T04

Notes: (1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.

X28C512

POWER-UP TIMING

Symbol	Parameter	Max.	Units
tPUR <sup>(2)</sup>	Power-up to Read Operation	100	μs
tPUW <sup>(2)</sup>	Power-up to Write Operation	5	ms

3856 PGM T05

CAPACITANCE TA = 25°C, f = 1.0 MHz, VCC = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C <sub>I/O</sub> <sup>(2)</sup>	Input/Output Capacitance	10	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> <sup>(2)</sup>	Input Capacitance	10	pF	V <sub>IN</sub> = 0V

3856 PGM T06

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	10,000		Cycles per Byte
Data Retention	100		Years

3856 PGM T11

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V

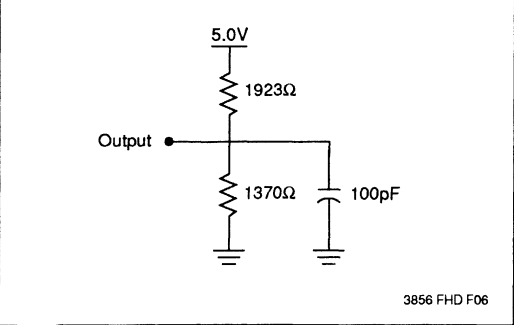
3856 PGM T07

MODE SELECTION

CE	OE	WE	Mode	I/O	Power
L	L	H	Read	D <sub>OUT</sub>	Active
L	H	L	Write	D <sub>IN</sub>	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3856 PGM T08

EQUIVALENT A.C. LOAD CIRCUIT



3856 FHD F06

Note: (2) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

# X28C512

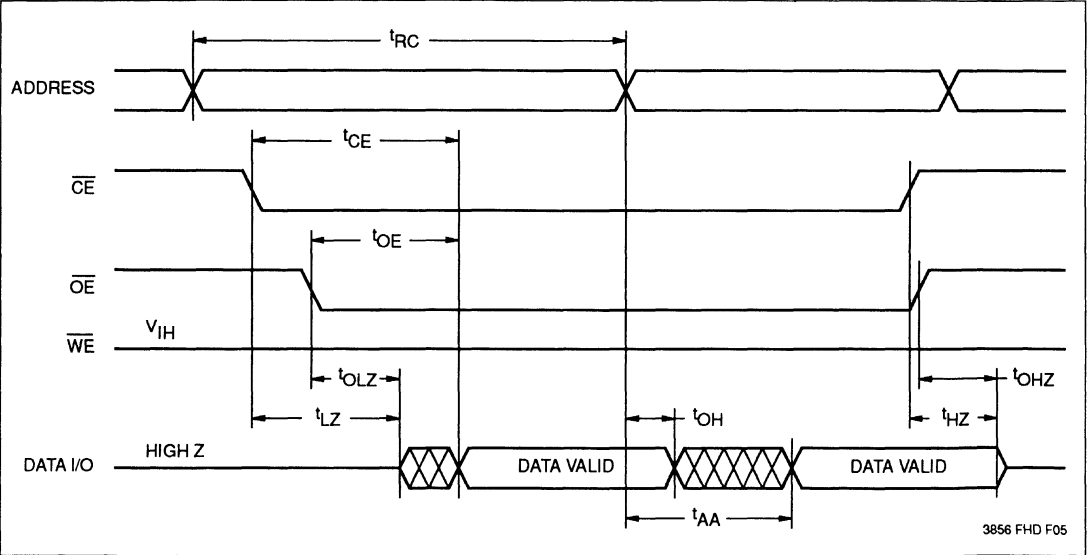
## A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

### Read Cycle Limits

Symbol	Parameter	X28C512-12		X28C512-15		X28C512-20		X28C512-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	120		150		200		250		ns
$t_{CE}$	Chip Enable Access Time		120		150		200		250	ns
$t_{AA}$	Address Access Time		120		150		200		250	ns
$t_{OE}$	Output Enable Access Time		50		50		50		50	ns
$t_{LZ}^{(3)}$	$\overline{CE}$ Low to Active Output	0		0		0		0		ns
$t_{OLZ}^{(3)}$	$\overline{OE}$ Low to Active Output	0		0		0		0		ns
$t_{HZ}^{(3)}$	$\overline{CE}$ High to High Z Output		50		50		50		50	ns
$t_{OHZ}^{(3)}$	$\overline{OE}$ High to High Z Output		50		50		50		50	ns
$t_{OH}$	Output Hold from Address Change	0		0		0		0		ns

3858 PGM T09

### Read Cycle



3856 FHD F05

**Notes:** (3)  $t_{LZ}$  min.,  $t_{HZ}$ ,  $t_{OLZ}$  min., and  $t_{OHZ}$  are periodically sampled and not 100% tested.  $t_{HZ}$  max. and  $t_{OHZ}$  max. are measured, with  $C_L$  - 5pF from the point when  $\overline{CE}$  or  $\overline{OE}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

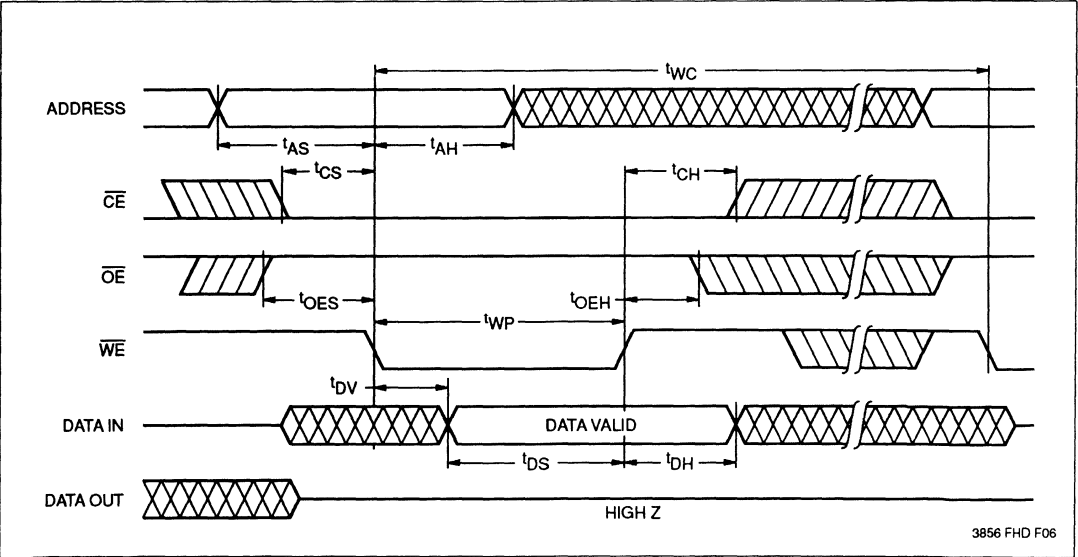
# X28C512

## WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Max.	Units
$t_{WC}^{(4)}$	Write Cycle Time		10	ms
$t_{AS}$	Address Setup Time	0		ns
$t_{AH}$	Address Hold Time	50		ns
$t_{CS}$	Write Setup Time	0		ns
$t_{CH}$	Write Hold Time	0		ns
$t_{CW}$	CE Pulse Width	100		ns
$t_{OES}$	OE High Setup Time	10		ns
$t_{OEH}$	OE High Hold Time	10		ns
$t_{WP}$	WE Pulse Width	100		ns
$t_{WPH}$	WE High Recovery	100		ns
$t_{DV}$	Data Valid		1	$\mu$ s
$t_{DS}$	Data Setup	50		ns
$t_{DH}$	Data Hold	10		ns
$t_{DW}$	Delay to Next Write	10		$\mu$ s
$t_{BLC}$	Byte Load Cycle	0.20	100	$\mu$ s

3856 PGM T10

## WE Controlled Write Cycle

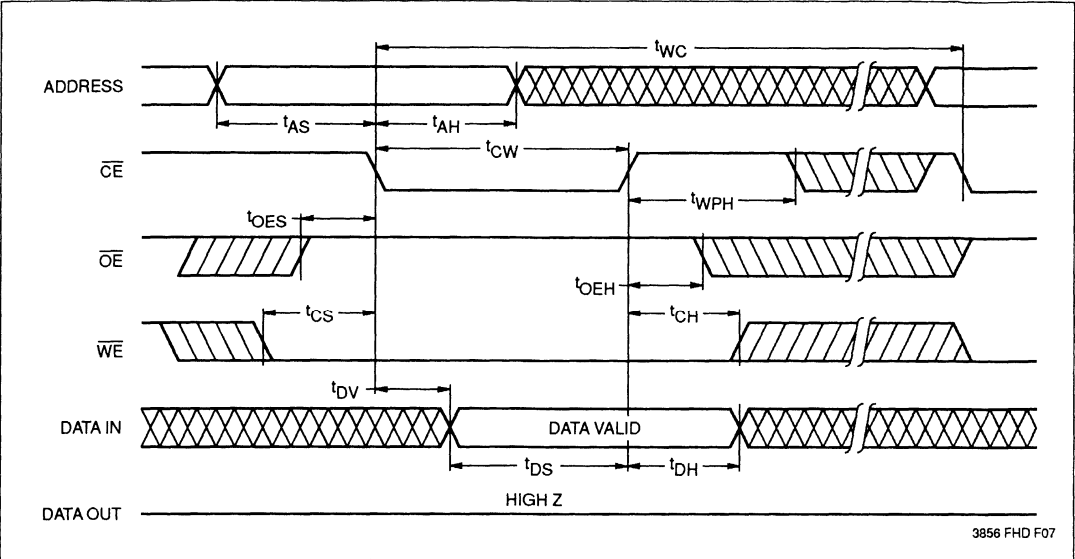


3856 FHD F06

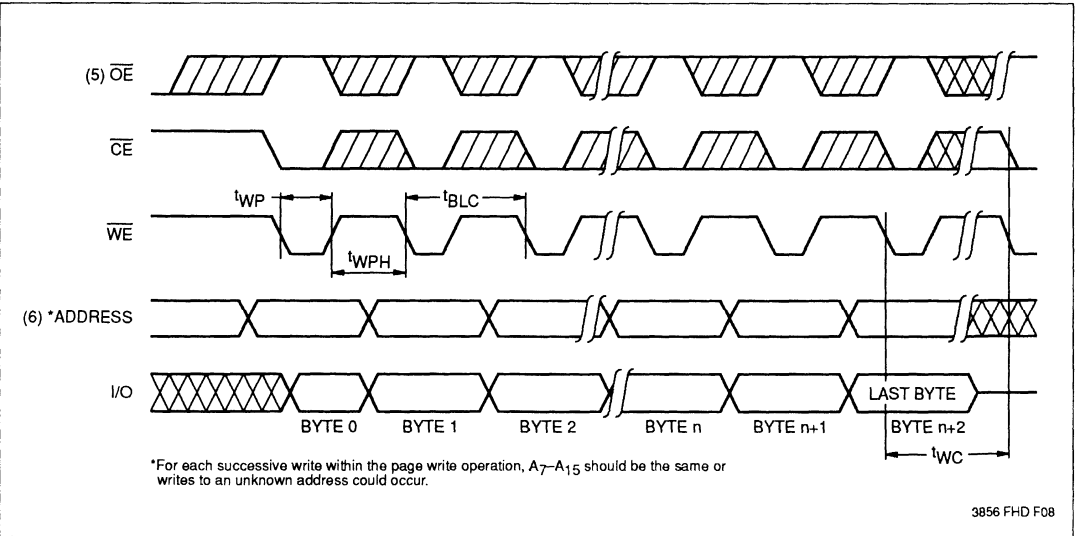
**Notes:** (4)  $t_{WC}$  is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete the internal write operation.

# X28C512

## $\overline{\text{CE}}$ Controlled Write Cycle



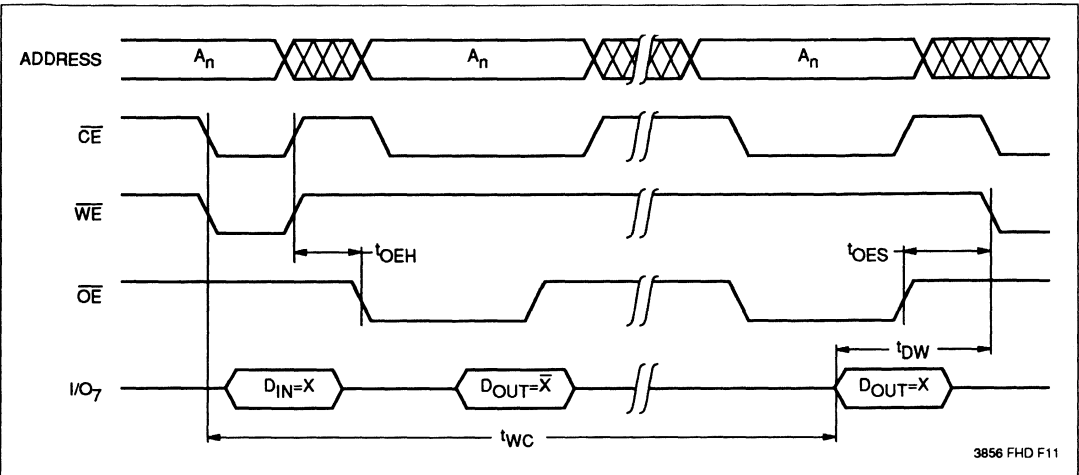
## Page Write Cycle



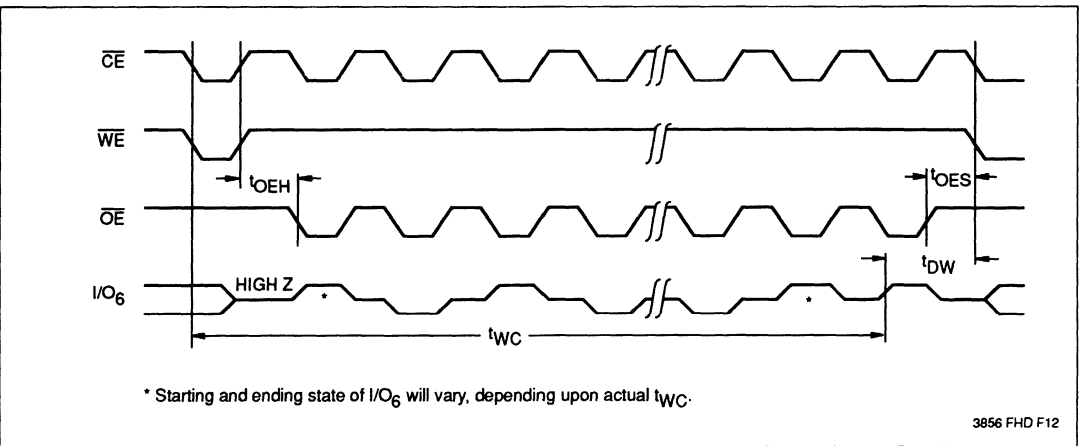
- Notes:**
- (5) Between successive byte writes within a page write operation,  $\overline{\text{OE}}$  can be strobed LOW: e.g. this can be done with  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  HIGH to fetch data from another memory device within the system for the next write; or with  $\overline{\text{WE}}$  HIGH and  $\overline{\text{CE}}$  LOW effectively performing a polling operation.
  - (6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  controlled write cycle timing.

# X28C512

DATA Polling Timing Diagram(7)



Toggle Bit Timing Diagram



**Note:** (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.



**X28C512**

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**NOTES**



1M

X28C010

128K x 8 Bit

## 5 Volt, Byte Alterable E<sup>2</sup>PROM

### FEATURES

- Access Time: 120 ns
- SIMPLE Byte and Page Write
  - Single 5 Volt Supply
  - No External High Voltages or V<sub>pp</sub> Control Circuits
  - Self Timed
    - No Erase Before Write
    - No Complex Programming Algorithms
    - No Overerase Problem
- Low Power CMOS:
  - Active: 50mA
  - Standby: 500 $\mu$ A
- Software Data Protection
  - Protects Data Against System Level Inadvertent Writes
- High Speed Page Write Capability
- Highly Reliable Direct Write™ Cell
  - Endurance: 10,000 Write Cycles
  - Data Retention: 100 Years
- Early End of Write Detection
  - DATA Polling
  - Toggle Bit Polling

### DESCRIPTION

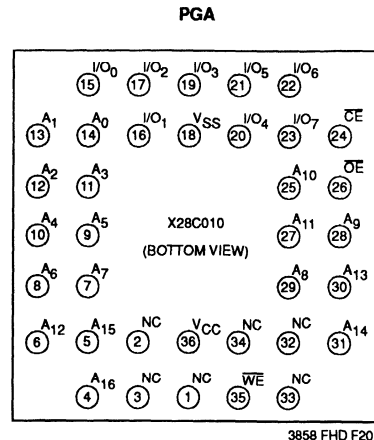
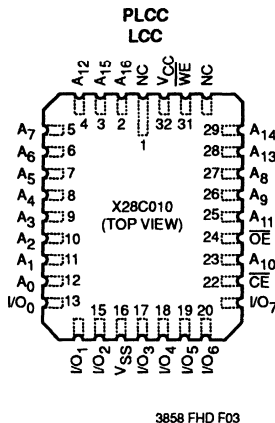
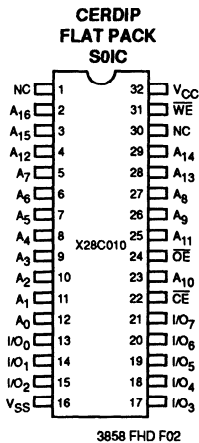
The Xicor X28C010 is a 128K x 8 E<sup>2</sup>PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C010 is a 5V only device. The X28C010 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard EPROMs.

The X28C010 supports a 256-byte page write operation, effectively providing a 19  $\mu$ s/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C010 also features DATA Polling and Toggle Bit test, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28C010 supports Software Data Protection option.

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

3

### PIN CONFIGURATION



# X28C010

## PIN DESCRIPTIONS

### Addresses (A<sub>0</sub>–A<sub>16</sub>)

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{\text{CE}}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{\text{CE}}$  is HIGH, power consumption is reduced.

### Output Enable ( $\overline{\text{OE}}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

### Data In/Data Out (I/O<sub>0</sub>–I/O<sub>7</sub>)

Data is written to or read from the X28C010 through the I/O pins.

### Write Enable ( $\overline{\text{WE}}$ )

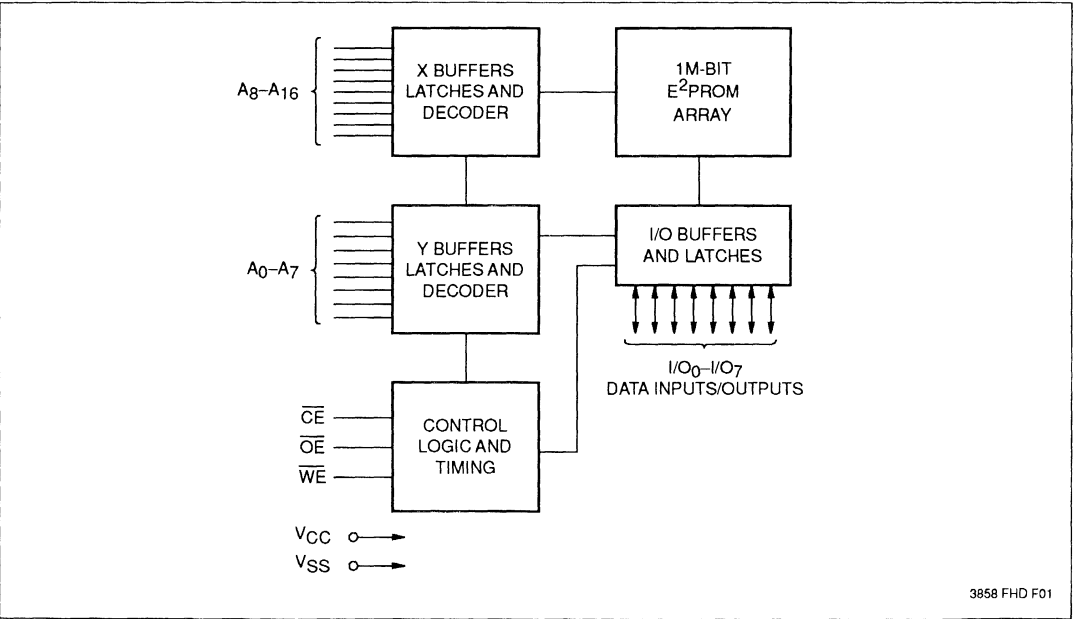
The Write Enable input controls the writing of data to the X28C010.

## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>16</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

3858 PGM T01

## FUNCTIONAL DIAGRAM



3858 FHD F01

## X28C010

### DEVICE OPERATION

#### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

#### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The X28C010 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

#### Page Write Operation

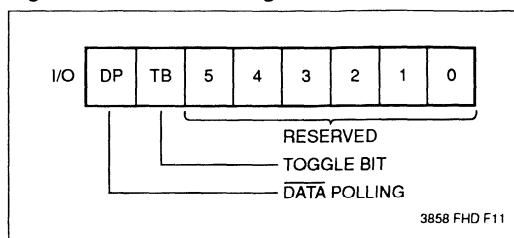
The page write feature of the X28C010 allows the entire memory to be written in 5 seconds. Page write allows two to two hundred fifty-six bytes of data to be consecutively written to the X28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address ( $A_8$  through  $A_{16}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to two hundred fifty-six bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100  $\mu$ s.

#### Write Operation Status Bits

The X28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



#### DATA Polling (I/O<sub>7</sub>)

The X28C010 features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O<sub>7</sub> (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O<sub>7</sub> will reflect true data. Note: If the X28C010 is in the protected state and an illegal write operation is attempted DATA Polling will not operate.

#### Toggle Bit (I/O<sub>6</sub>)

The X28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O<sub>6</sub> will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

# X28C010

DATA Polling I/O<sub>7</sub>  
Figure 2. DATA Polling Bus Sequence

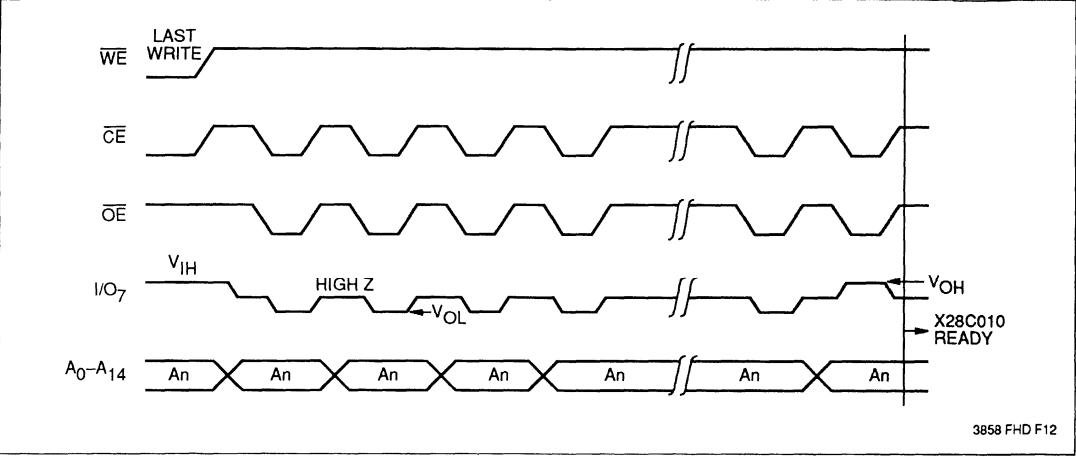
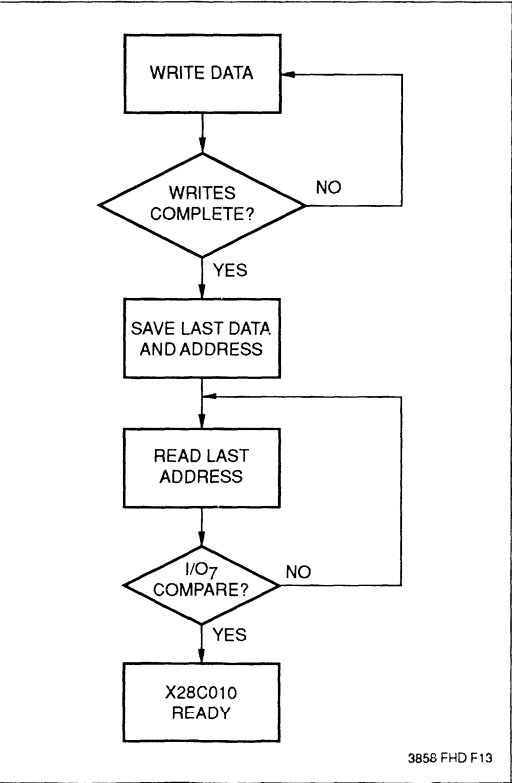


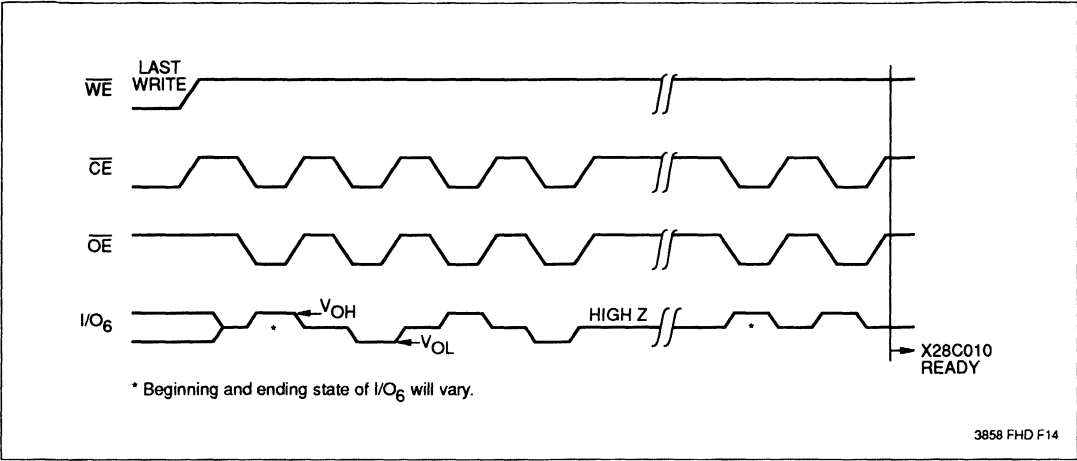
Figure 3. DATA Polling Software Flow



DATA Polling can effectively halve the time for writing to the X28C010. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

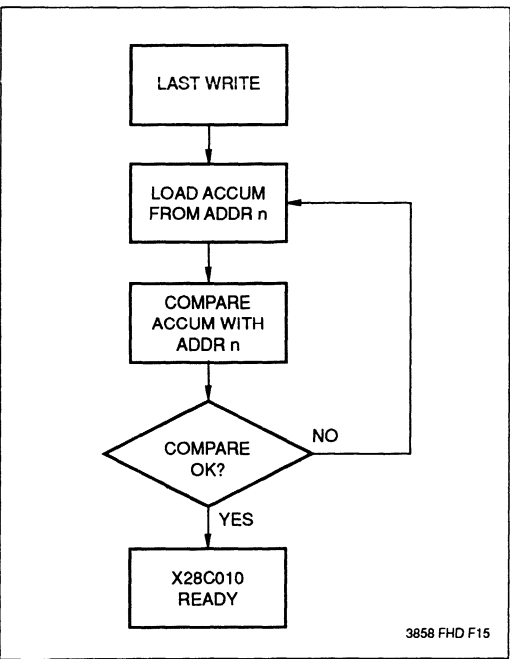
# X28C010

The Toggle Bit I/O<sub>6</sub>  
 Figure 4. Toggle Bit Bus Sequence



3

Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28C010 memories that is frequently updated. Toggle Bit testing can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

## X28C010

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### HARDWARE DATA PROTECTION

The X28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A  $\overline{WE}$  pulse less than 10 ns will not initiate a write cycle.
- Default  $V_{CC}$  Sense—All functions are inhibited when  $V_{CC}$  is  $\leq 3.6V$ .
- Write inhibit—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH, or  $\overline{CE}$  HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

### SOFTWARE DATA PROTECTION

The X28C010 offers a software controlled data protection feature. The X28C010 is shipped from Xicor with the software data protection NOT ENABLED: that is the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once  $V_{CC}$  was stable.

The X28C010 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C010 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

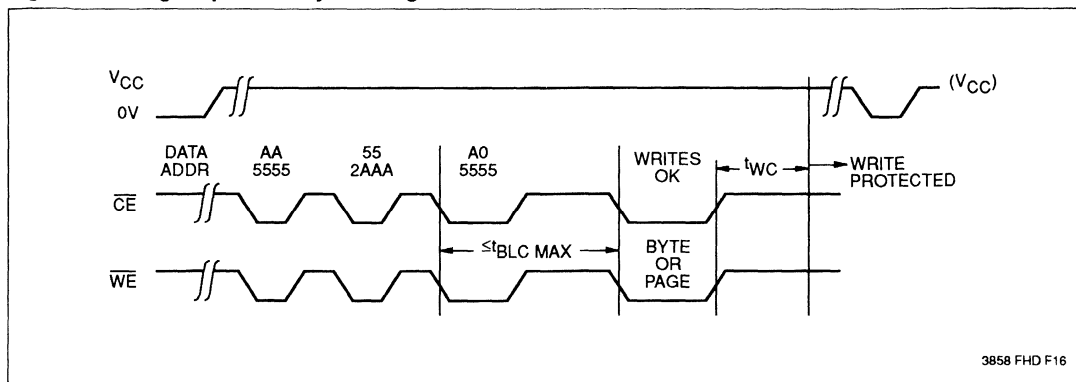
### SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figures 6 and 7 for the sequence. The three byte sequence opens the page write window enabling the host to write from one to two hundred fifty-six bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

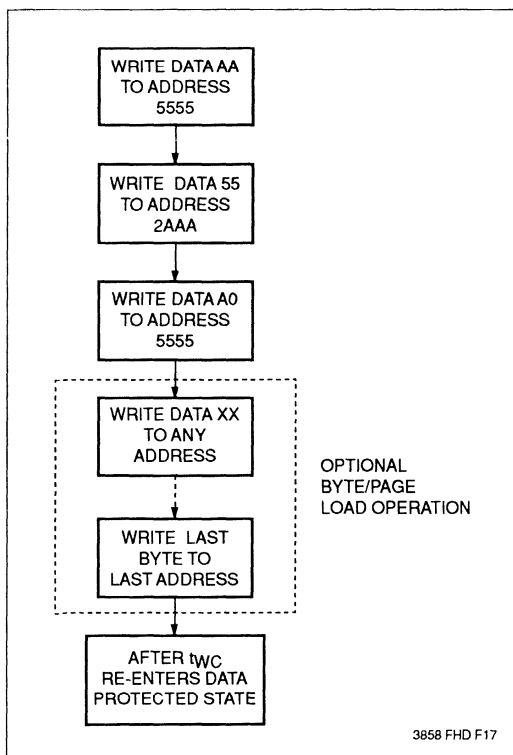
**X28C010**

## Software Data Protection

### Figure 6. Timing Sequence—Byte or Page Write



### Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C010 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C010 will be write protected during power-down and after any subsequent power-up. The state of A<sub>15</sub> and A<sub>16</sub> while executing the algorithm is don't care.

**Note:** Once initiated, the sequence of write operations should not be interrupted.



X28C010

Resetting Software Data Protection  
Figure 8. Reset Software Data Protection Timing Sequence

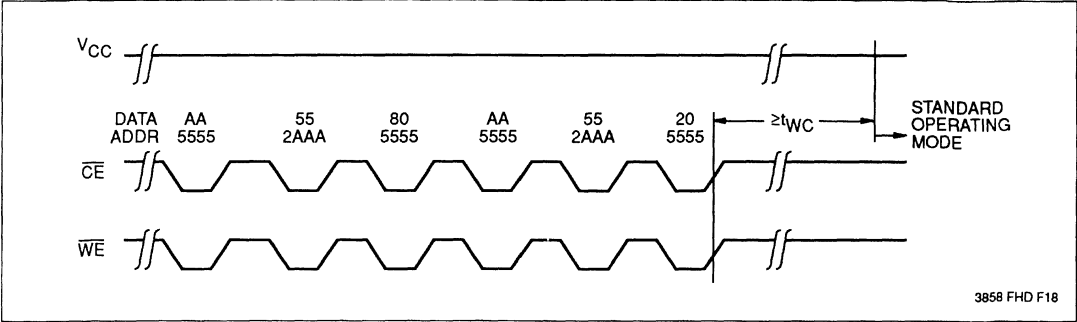
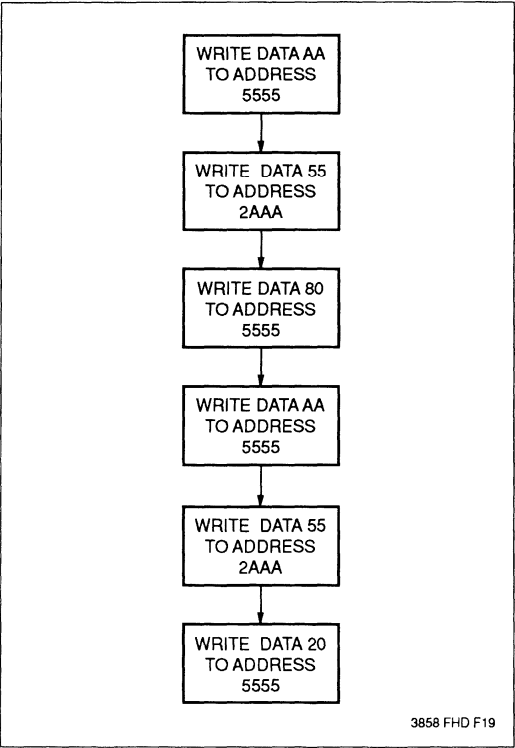


Figure 9. Software Sequence to Deactivate  
Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E<sup>2</sup>PROM programmer, the following six step algorithm will reset the internal protection circuit. After  $t_{WC}$ , the X28C010 will be in standard operating mode.

*Note: Once initiated, the sequence of write operations should not be interrupted.*

## X28C010

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### SYSTEM CONSIDERATIONS

Because the X28C010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C010 has two power modes, standby and active, proper decoupling of the memory array is of

prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu$ F high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7  $\mu$ F electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

X28C010

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X28C010 .....	–10°C to +85°C
X28C010I .....	–65°C to +135°C
X28C010M .....	–65°C to +135°C
Storage Temperature .....	
–65°C to +150°C	
Voltage on any Pin with	
Respect to Ground .....	–1.0V to +7.0V
D.C. Output Current .....	5 mA
Lead Temperature	
(Soldering, 10 Seconds) .....	300°C

\*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMEND OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3826 PGM T02

Supply Voltage	Limits
X28C010	5V ±10%

3826 PGM T03

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Current (Active) (TTL Inputs)		50	mA	$\overline{CE} = \overline{OE} = V_{IL}$ , $\overline{WE} = V_{IH}$ . All I/O's = Open, Address Inputs = .4V/2.4V Levels @ f = 5MHz
I <sub>SB1</sub>	V <sub>CC</sub> Current (Standby) (TTL Inputs)		3	mA	$CE = V_{IH}$ , $OE = V_{IL}$ All I/O's = Open, Other Inputs = V <sub>IH</sub>
I <sub>SB2</sub>	V <sub>CC</sub> Current (Standby) (CMOS Inputs)		500	µA	$\overline{CE} = V_{CC} - 0.3V$ , $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V <sub>CC</sub>
I <sub>LI</sub>	Input Leakage Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , $CE = V_{IH}$
V <sub>IL</sub> (1)	Input Low Voltage	–1.0	0.8	V	
V <sub>IH</sub> (1)	Input High Voltage	2.0	V <sub>CC</sub> + 1.0	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = –400 µA

3858 PGM T02

Notes: (1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.

# X28C010

## POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(2)}$	Power-up to Read Operation	100	$\mu$ s
$t_{PUW}^{(2)}$	Power-up to Write Operation	5	ms

3858 PGM T03

**CAPACITANCE**  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ ,  $V_{CC} = 5\text{V}$

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}^{(2)}$	Input/Output Capacitance	10	pF	$V_{I/O} = 0\text{V}$
$C_{IN}^{(2)}$	Input Capacitance	10	pF	$V_{IN} = 0\text{V}$

3858 PGM T04

## ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	10,000		Cycles per Byte
Data Retention	100		Years

3858 PGM T05

## A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V

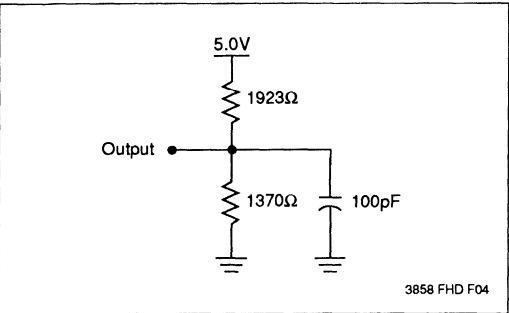
3858 PGM T05

## MODE SELECTION

CE	OE	WE	Mode	I/O	Power
L	L	H	Read	$D_{OUT}$	Active
L	H	L	Write	$D_{IN}$	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3858 PGM T06

## EQUIVALENT A.C. LOAD CIRCUIT



**Note:** (2) This parameter is periodically sampled and not 100% tested.

## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

# X28C010

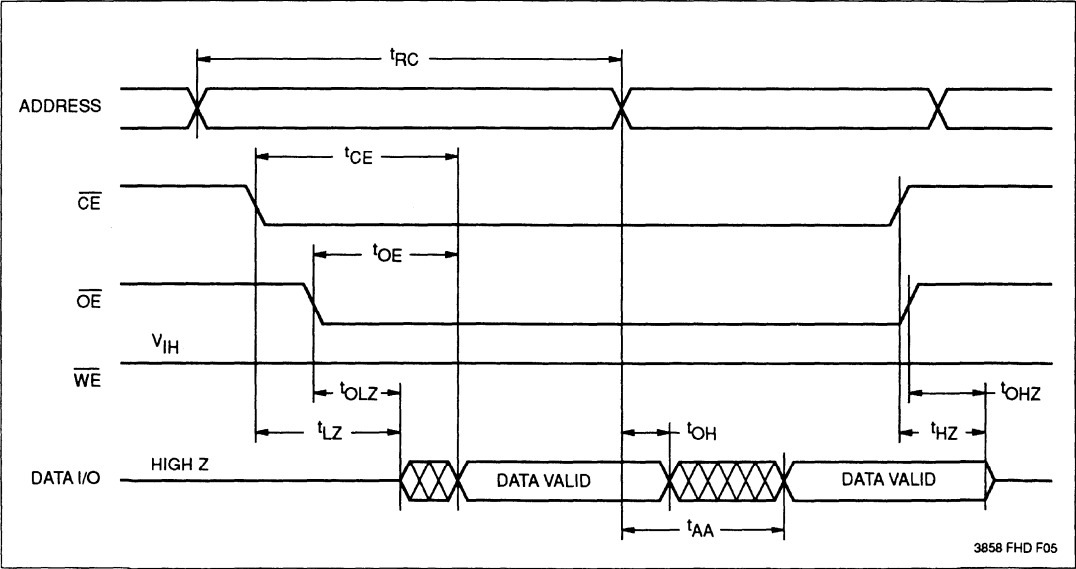
## A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

### Read Cycle Limits

Symbol	Parameter	X28C010-12		X28C010-15		X28C010-20		X28C010-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	120		150		200		250		ns
t <sub>CE</sub>	Chip Enable Access Time		120		150		200		250	ns
t <sub>AA</sub>	Address Access Time		120		150		200		250	ns
t <sub>OE</sub>	Output Enable Access Time		50		50		50		50	ns
t <sub>LZ</sub> <sup>(3)</sup>	CE Low to Active Output	0		0		0		0		ns
t <sub>OLZ</sub> <sup>(3)</sup>	OE Low to Active Output	0		0		0		0		ns
t <sub>HZ</sub> <sup>(3)</sup>	CE High to High Z Output		50		50		50		50	ns
t <sub>OHZ</sub> <sup>(3)</sup>	OE High to High Z Output		50		50		50		50	ns
t <sub>OH</sub>	Output Hold from Address Change	0		0		0		0		ns

3858 PGM T08

### Read Cycle



3858 FHD F05

**Note:** (3)  $t_{LZ}$  min.,  $t_{HZ}$ ,  $t_{OLZ}$  min., and  $t_{OHZ}$  are periodically sampled and not 100% tested.  $t_{HZ}$  max. and  $t_{OHZ}$  max. are measured, with  $C_L = 5pF$ , from the point when  $\overline{CE}$  or  $\overline{OE}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

# X28C010

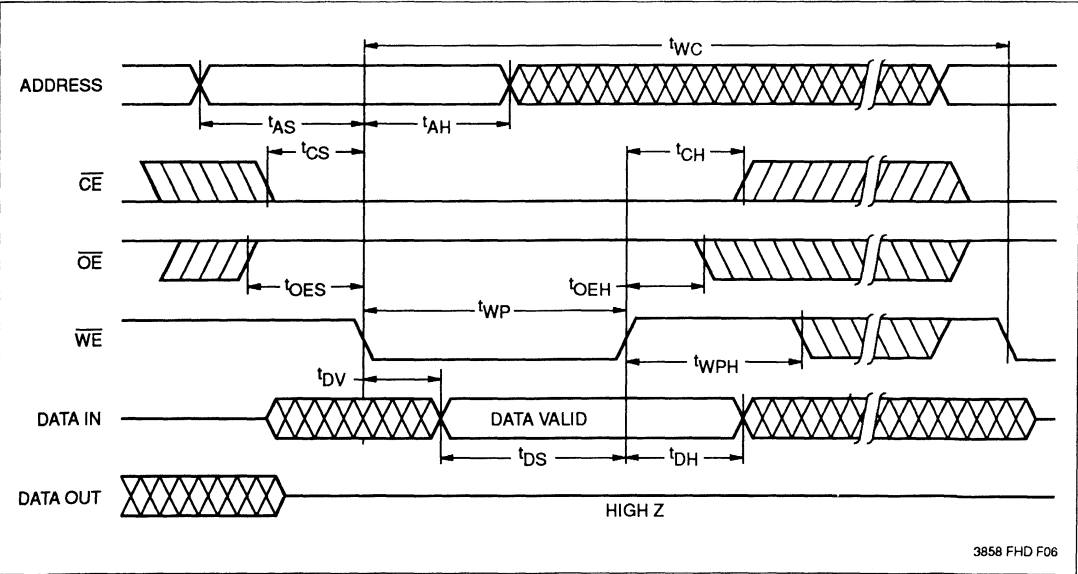
## Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
$t_{WC}^{(4)}$	Write Cycle Time		10	ms
$t_{AS}$	Address Setup Time	0		ns
$t_{AH}$	Address Hold Time	50		ns
$t_{CS}$	Write Setup Time	0		ns
$t_{CH}$	Write Hold Time	0		ns
$t_{CW}$	CE Pulse Width	100		ns
$t_{OES}$	OE High Setup Time	10		ns
$t_{OEH}$	OE High Hold Time	10		ns
$t_{WP}$	WE Pulse Width	100		ns
$t_{WPH}$	WE High Recovery	100		ns
$t_{DV}$	Data Valid		1	$\mu$ s
$t_{DS}$	Data Setup	50		ns
$t_{DH}$	Data Hold	10		ns
$t_{DW}$	Delay to Next Write	10		$\mu$ s
$t_{BLC}$	Byte Load Cycle	0.2	100	$\mu$ s

3858 PGM T09

3

## WE Controlled Write Cycle

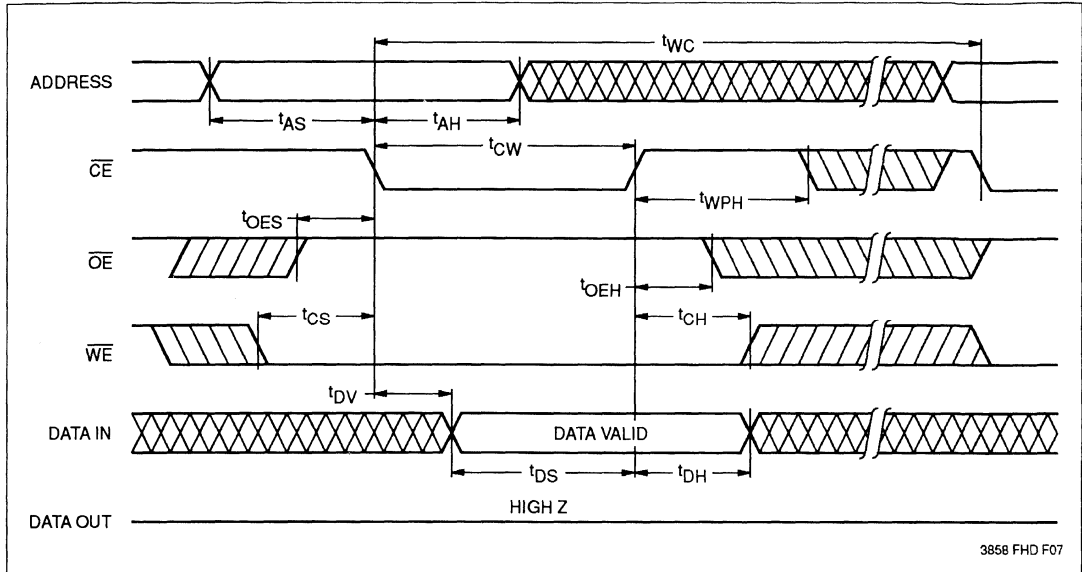


3858 FHD F06

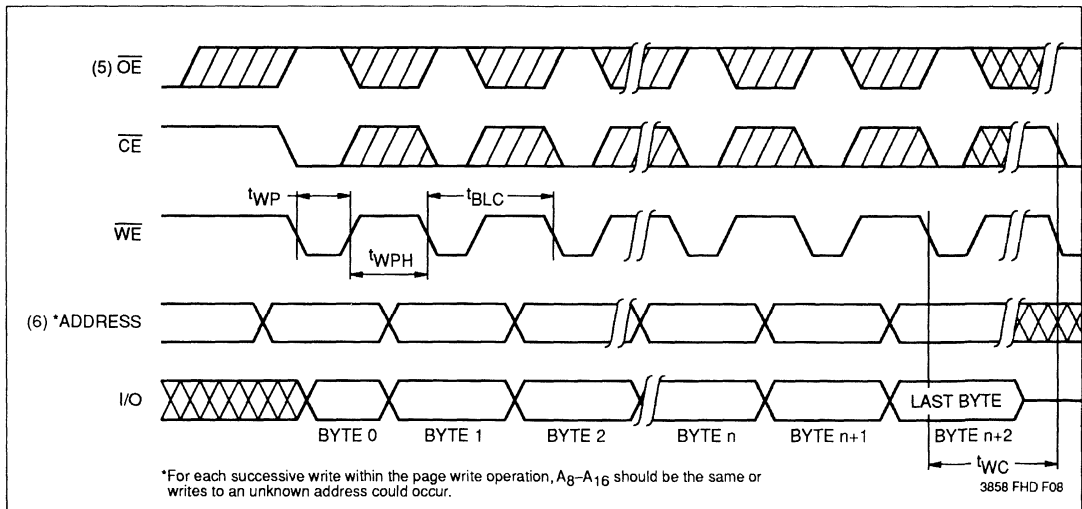
**Notes:** (4)  $t_{WC}$  is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete internal write operation.

## X28C010

### $\overline{\text{CE}}$ Controlled Write Cycle



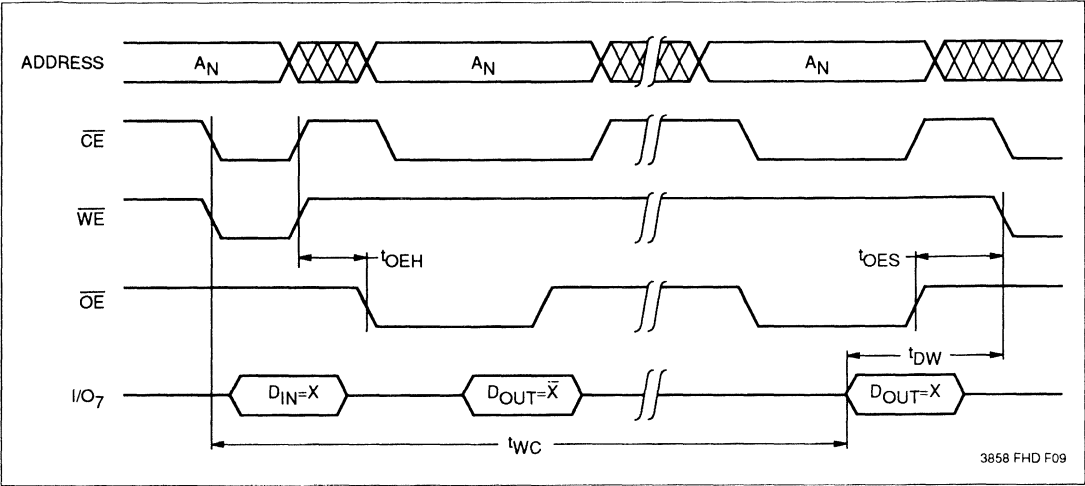
### Page Write Cycle



- Notes:** (5) Between successive byte writes within a page write operation,  $\overline{\text{OE}}$  can be strobed LOW: e.g. this can be done with  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  HIGH to fetch data from another memory device within the system for the next write; or with  $\overline{\text{WE}}$  HIGH and  $\overline{\text{CE}}$  LOW effectively performing a polling operation.
- (6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  controlled write cycle timing.

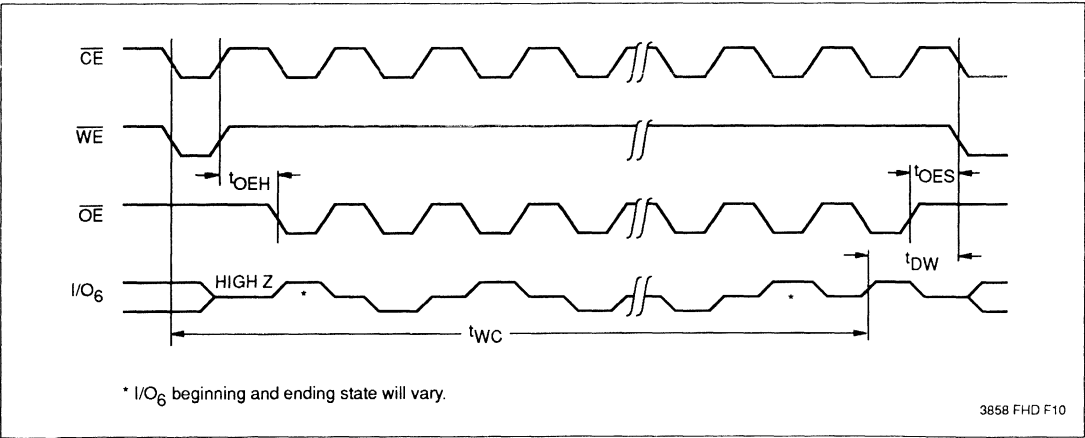
X28C010

DATA Polling Timing Diagram(7)



3

Toggle Bit Timing Diagram



**Note:** (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.



**X28C010**

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**NOTES**



<b>NOVRAM* Data Sheets</b>	<b>1</b>
<b>Serial Products Data Sheets</b>	<b>2</b>
<b>E<sup>2</sup>PROM Data Sheets</b>	<b>3</b>
<b>E<sup>2</sup>POT™ Data Sheets</b>	<b>4</b>
<b>Microcontroller Peripheral Products</b>	<b>5</b>
<b>Memory Subsystems</b>	<b>6</b>
<b>Military Products</b>	<b>7</b>
<b>Die Products</b>	<b>8</b>
<b>Application Notes and Briefs</b>	<b>9</b>
<b>Reliability</b>	<b>10</b>
<b>General Information</b>	<b>11</b>



## X9CMME

### E<sup>2</sup>POT<sup>™</sup> Digitally Controlled Potentiometer

#### FEATURES

- Compatible with X9MME
- Low Power CMOS
  - Active Current, 3 mA Max
  - Standby Current, 500  $\mu A$  Max
- 99 Resistive Elements
  - Temperature Compensated
  - $\pm 20\%$  End to End Resistance Range
- 100 Wiper Tap Points
  - Wiper Positioned via Three Wire Interface
  - Similar to TTL Up/Down Counter
  - Wiper Position Stored in Nonvolatile Memory and Recalled on Power-Up
- 100 Year Wiper Position Data Retention
- X9C102 = 1K Ohms
- X9C103 = 10K Ohms
- X9C503 = 50K Ohms
- X9C104 = 100K Ohms

#### DESCRIPTION

The Xicor X9CMME is a solid state nonvolatile potentiometer and is ideal for digitally controlled resistance trimming.

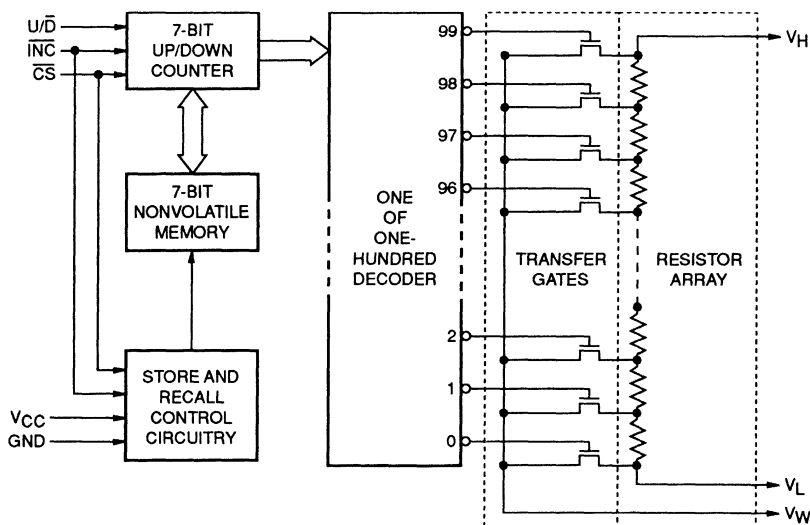
The X9CMME is a resistor array composed of 99 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element is controlled by the  $\overline{CS}$ ,  $U/\overline{D}$ , and  $INC$  inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-on operation.

The resolution of the X9CMME is equal to the maximum resistance value divided by 99. As an example, for the X9C503 (50 K $\Omega$ ) each tap point represents 505 $\Omega$ .

All Xicor nonvolatile memories are designed and tested for applications requiring extended endurance and data retention. Refer to Xicor reliability reports RR-515 and RR-520 for detailed Information.

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#### FUNCTIONAL DIAGRAM



3863 FHD F01

# X9CMME

## PIN DESCRIPTIONS

### $V_H$ and $V_L$

The high ( $V_H$ ) and low ( $V_L$ ) terminals of the X9CMME are equivalent to the fixed terminals of a mechanical potentiometer. The minimum and maximum voltage that may be applied to the terminals is determined by the voltage on  $V_{CC}$ . The minimum voltage is  $-5$  and the maximum is  $+5$ . It should be noted that the terminology of  $V_L$  and  $V_H$  references the relative position of the terminal in relation to wiper movement direction selected by the  $U/\overline{D}$  input and not the voltage potential on the terminal.

### $V_W$

$V_W$  is the wiper terminal, equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically less than  $40\Omega$ .

### Up/Down ( $U/\overline{D}$ )

The  $U/\overline{D}$  input controls the direction of the wiper movement and whether the counter is incremented or decremented.

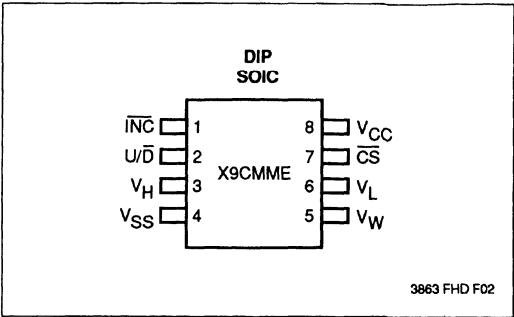
### Increment ( $\overline{INC}$ )

The  $\overline{INC}$  input is negative-edge triggered. Toggling  $\overline{INC}$  will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the  $U/\overline{D}$  input.

### Chip Select ( $\overline{CS}$ )

The device is selected when the  $\overline{CS}$  input is low. The current counter value is stored in nonvolatile memory when  $\overline{CS}$  is returned HIGH while the  $\overline{INC}$  input is also high. After the store operation is complete the X9CMME will be placed in the low power standby mode until the device is selected once again.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
$V_H$	High Terminal
$V_W$	Wiper Terminal
$V_L$	Low Terminal
$V_{SS}$	Ground
$V_{CC}$	Supply Voltage
$U/\overline{D}$	Up/Down Input
$\overline{INC}$	Increment Input
$\overline{CS}$	Chip Select Input
NC	No Connect

3863 PGM T01

# X9CMME

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## DEVICE OPERATION

There are three basic sections of the X9CMME: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The  $\overline{INC}$ ,  $U/\overline{D}$  and  $\overline{CS}$  inputs control the movement of the wiper along the resistor array. With  $\overline{CS}$  set low the X9CMME is selected and enabled to respond to the  $U/\overline{D}$  and  $\overline{INC}$  inputs. High to low transitions on  $\overline{INC}$  will increment or decrement (depending on the state of the  $U/\overline{D}$  input) a seven bit counter. The output of this counter is decoded to select one of one-hundred wiper positions along the resistive array.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The value of the counter is stored in nonvolatile memory whenever  $\overline{CS}$  transitions high while the  $\overline{INC}$  input is also high.

When the X9CMME is powered down, the last counter position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is reset to the value last stored.

## OPERATION NOTES

The system may select the X9CMME, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. The wiper movement is performed as described above; once the new position is reached, the system would keep  $\overline{INC}$  low while taking  $\overline{CS}$  high. The new wiper position would be maintained until changed by the system or until a power-off/on cycle recalled the previously stored data.

This would allow the system to always power-on to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift etc.

The state of  $U/\overline{D}$  may be changed while  $\overline{CS}$  remains low. This allows the host system to enable the X9CMME and then move the wiper up and down until the proper trim is attained.

### $T_{IW}/R_{TOTAL}$

The electronic switches on the X9CMME operate in a "make before break" mode when the wiper changes tap positions. If the wiper is moved several positions multiple taps are connected to the wiper for  $T_{IW}$  ( $\overline{INC}$  to  $V_W$  change). The  $R_{TOTAL}$  value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

### $R_{TOTAL}$ with $V_{CC}$ Removed

The end to end resistance of the array will fluctuate once  $V_{CC}$  is removed.

# X9CMME

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	-65°C to +135°C
Storage Temperature .....	-65°C to +150°C
Voltage on $\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ and $V_{CC}$ Referenced to Ground .....	-1.0V to +7.0V
Voltage on $V_H$ and $V_L$ Referenced to Ground .....	-8.0V to +8.0V
$\Delta V = (V_H \text{ and } V_L)$ X9C102 .....	4 V
X9C103, X9C503 and X9C104 .....	10 V
Lead Temperature (Soldering 10 Seconds) .....	+300°C
Wiper Current .....	$\pm 1$ mA

## ANALOG CHARACTERISTICS

### Electrical Characteristics

End-to-End Resistance Tolerance .....	$\pm 20\%$
Power Rating at 25°C X9C102 .....	16 mW
X9C103, X9C503 and X9C104 .....	10 mW
Wiper Current .....	$\pm 1$ mA Max.
Typical Wiper Resistance .....	40 $\Omega$ at 1 mA
Typical Noise .....	$< -120$ dB/ $\sqrt{\text{Hz}}$ Ref: 1 V

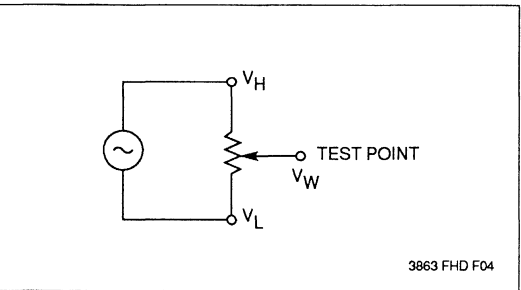
### Resolution

Resistance .....	1%
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### Linearity

Absolute Linearity <sup>(1)</sup> .....	$\pm 1.0$ MI <sup>(2)</sup>
Relative Linearity <sup>(3)</sup> .....	$\pm 0.2$ MI <sup>(2)</sup>

### Test Circuit #1



## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Temperature Coefficient

-40°C to +85°C X9C102 .....	+600 ppm/°C Typical
X9C103, X9C503, X9C104 .....	+300 ppm/°C Typical
Ratiometric Temperature Coefficient .....	$\pm 20$ ppm

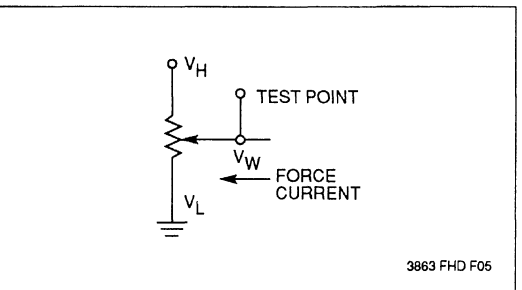
### Wiper Adjustability

Unlimited Wiper Adjustment (Non-store operation)  
Wiper Position Store Operations .... 10,000 Cycles

### Physical Characteristics

Marking Includes  
Manufacturer's Trademark  
Resistance Value or Code  
Date Code

### Test Circuit #2



- Notes:** (1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage  
 $= (V_{W(n)}(\text{actual}) - V_{W(n)}(\text{expected})) = \pm 1$  MI Maximum.  
(2) 1 MI = Minimum Increment =  $R_{TOT}/99$ .  
(3) Relative Linearity is a measure of the error in step size between taps  $= V_{W(n+1)} - [V_{W(n)} + \text{MI}] = +0.2$  MI.

X9CMME

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

3863 PGM T03

Supply Voltage	Limits
X9CMME	5V ± 10%

3863 PGM T04

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(4)	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Active Current		1	3	mA	$\overline{CS} = V_{IL}$ , $U/\overline{D} = V_{IL}$ or $V_{IH}$ and $\overline{INC} = 0.4V$ to $2.4V$ @ max. $t_{CYC}$
I <sub>SB</sub>	Standby Supply Current		200	500	μA	$\overline{CS} = V_{CC} - 0.3V$ , $U/\overline{D}$ and $\overline{INC} = GND$ or $V_{CC} - 0.3V$
I <sub>LI</sub>	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ Input Leakage Current			±10	μA	$V_{IN} = 0V$ to $V_{CC}$
V <sub>IH</sub>	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ Input High Voltage	2.0		$V_{CC} + 1.0$	V	
V <sub>IL</sub>	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ Input Low Voltage	−1.0		0.8	V	
R <sub>W</sub>	Wiper Resistance			100	Ω	Max. Wiper Current ±1mA
V <sub>VH</sub>	VH Terminal Voltage	−5			V	
V <sub>VL</sub>	VL Terminal Voltage	+5			V	
C <sub>IN</sub> (5)	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ Input Capacitance			10	pF	$V_{CC} = 5.0$ , $V_{IN} = 0V$ , $T_A = 25^\circ C$ , $f = 1\text{ MHz}$

3863 PGM T05

STANDARD PARTS

Part Number	Maximum Resistance	Wiper Increments	Minimum Resistance
X9C102	1 KΩ	10.1Ω	40Ω
X9C103	10 KΩ	101Ω	40Ω
X9C503	50 KΩ	505Ω	40Ω
X9C104	100 KΩ	1010Ω	40Ω

3863 PGM T08

Notes: (4) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage.  
(5) This parameter is periodically sampled and not 100% tested.



X9CMME

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Input Reference Levels	1.5V

3863 PGM T05

MODE SELECTION

CS	INC	U/D	Mode
L	$\overline{L}$	H	Wiper Up
L	$\overline{L}$	L	Wiper Down
f	H	X	Store Wiper Position
H	X	X	Standby Current
f	L	X	No Store, Return to Standby

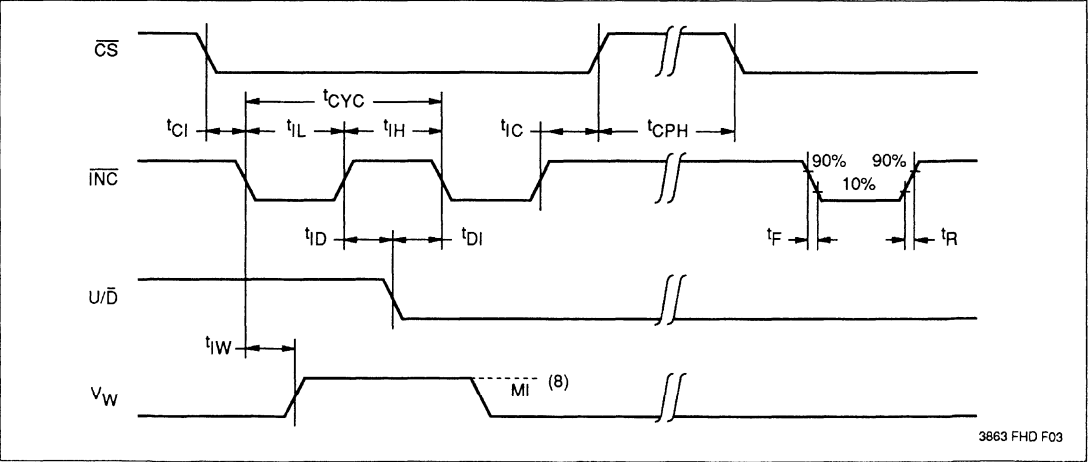
3863 PGM T06

A.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Units
		Min.	Typ. <sup>(6)</sup>	Max.	
t <sub>CI</sub>	CS to INC Setup	100			ns
t <sub>ID</sub>	INC High to U/D Change	100			ns
t <sub>DI</sub>	U/D to INC Setup	2.9			μs
t <sub>IL</sub>	INC Low Period	1			μs
t <sub>IH</sub>	INC High Period	1			μs
t <sub>IC</sub>	INC Inactive to CS Inactive	1			μs
t <sub>CPH</sub>	CS Deselect Time	20			ms
t <sub>IW</sub>	INC to V <sub>w</sub> Change		100	500	μs
t <sub>CYC</sub>	INC Cycle Time	24			μs
t <sub>R</sub> , t <sub>F</sub> <sup>(7)</sup>	INC Input Rise and Fall Time			500	μs
t <sub>PU</sub> <sup>(7)</sup>	Power up to Wiper Stable			500	μs
t <sub>R</sub> V <sub>CC</sub> <sup>(7)</sup>	V <sub>CC</sub> Rise Time	0.5			V/μs

3863 PGM T07

A.C. Timing

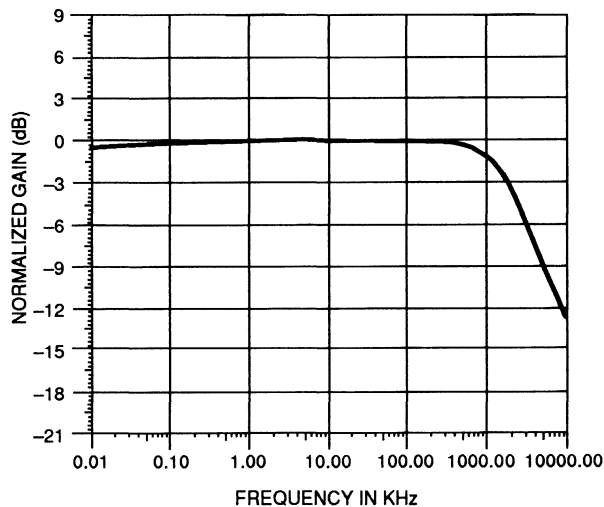


3863 FHD F03

- Notes: (6) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage.  
(7) This parameter is periodically sampled and not 100% tested.  
(8) MI in the A.C. timing diagram refers to the minimum incremental change in the V output due to a change in the wiper position.

**X9CMME**

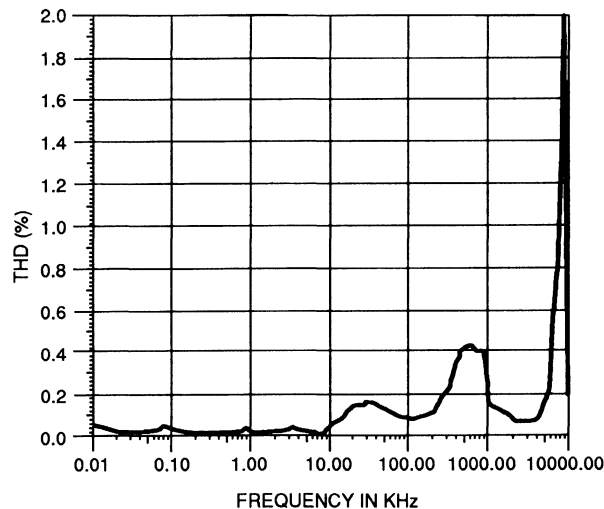
**Typical Frequency Response for X9C102**



**TEST CONDITIONS**  
 $V_{CC} = 5.0V$   
Temp. = Room  
Wiper @ Tap 50  
 $V_H = 0.5V$  RMS  
Normalized (0 dB @ 1KHz)  
Test Circuit #1

4

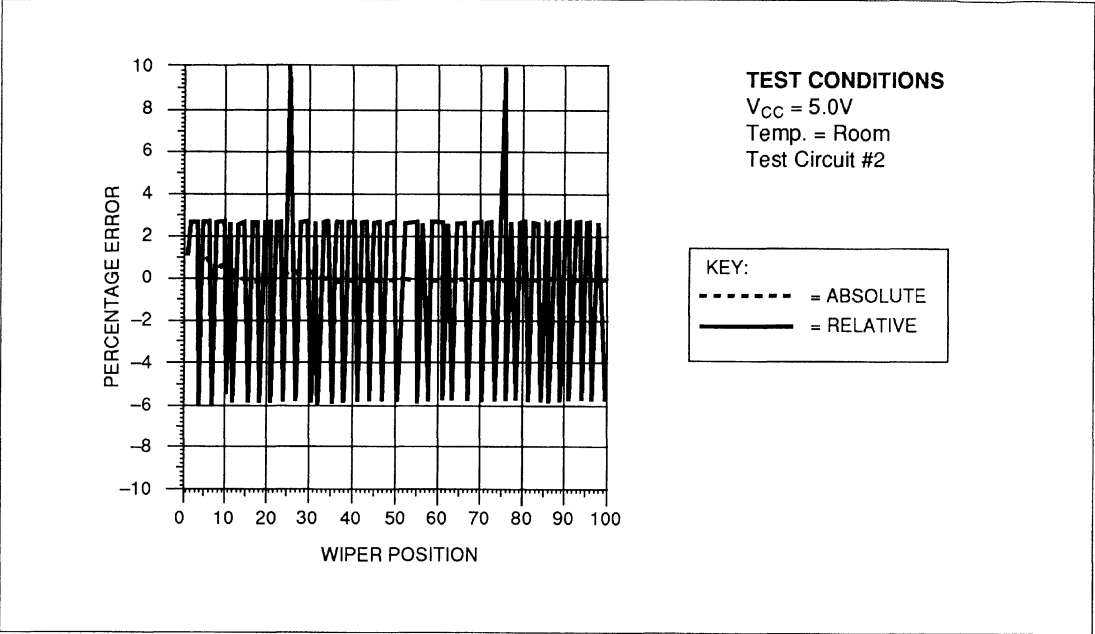
**Typical Total Harmonic Distortion for X9C102**



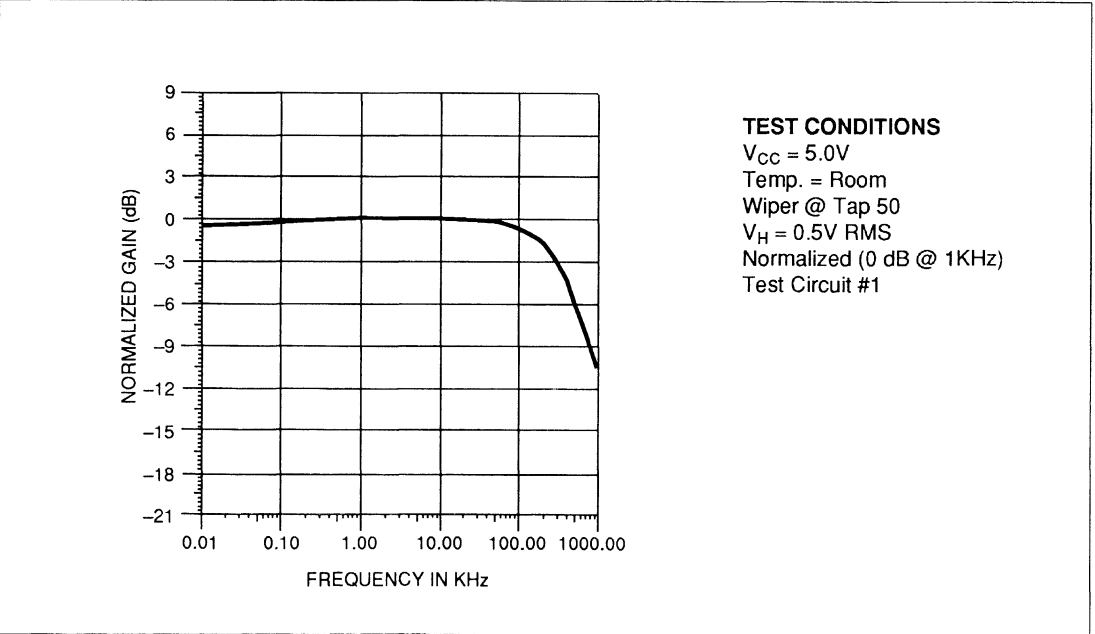
**TEST CONDITIONS**  
 $V_{CC} = 5.0V$   
Temp. = Room  
Wiper @ Tap 50  
 $V_H = 2V$  RMS  
Test Circuit #1

X9CMME

Typical Linearity for X9C102

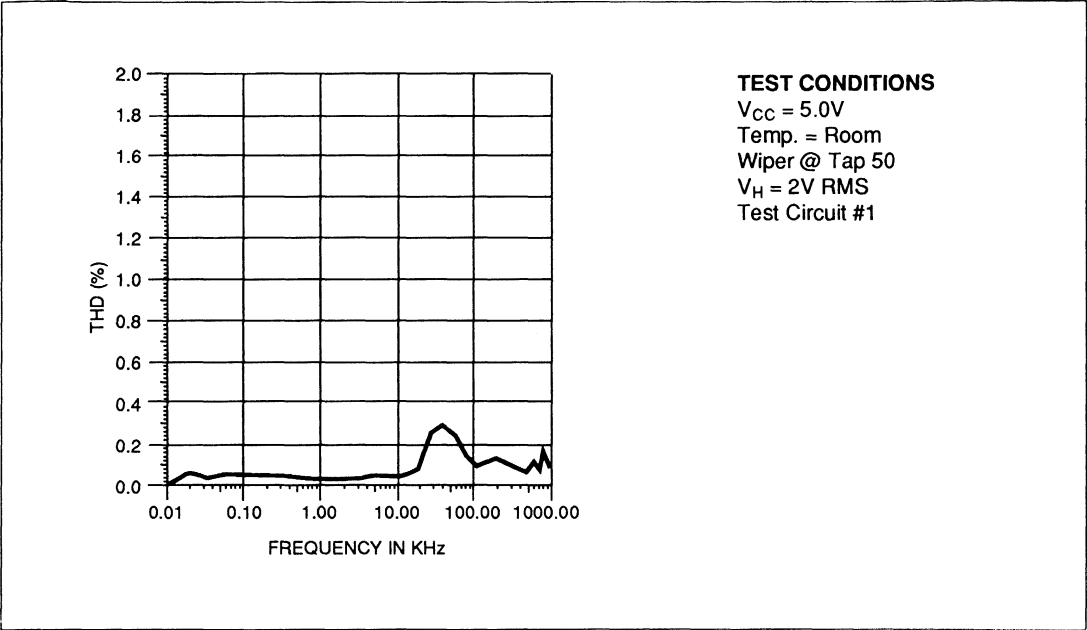


Typical Frequency Response for X9C103



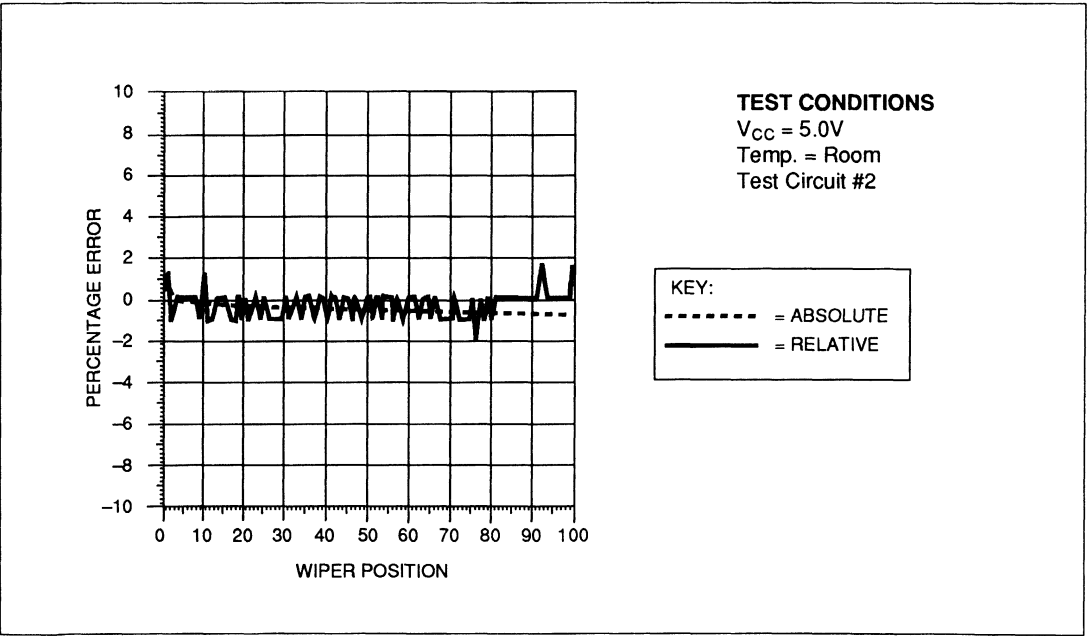
X9CMME

Typical Total Harmonic Distortion for X9C103



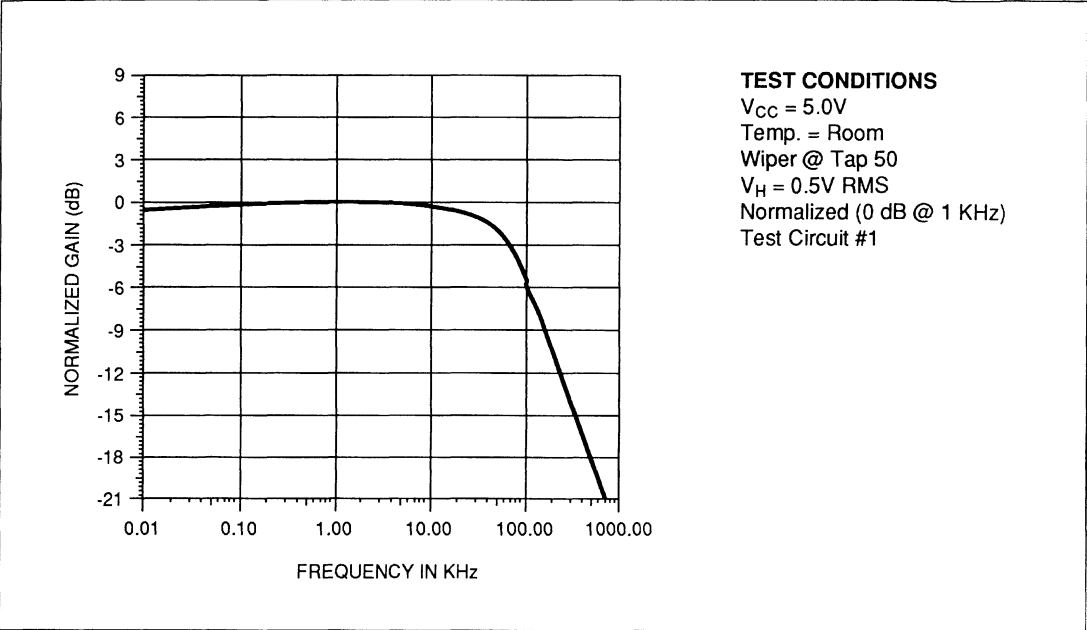
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Typical Linearity for X9C103

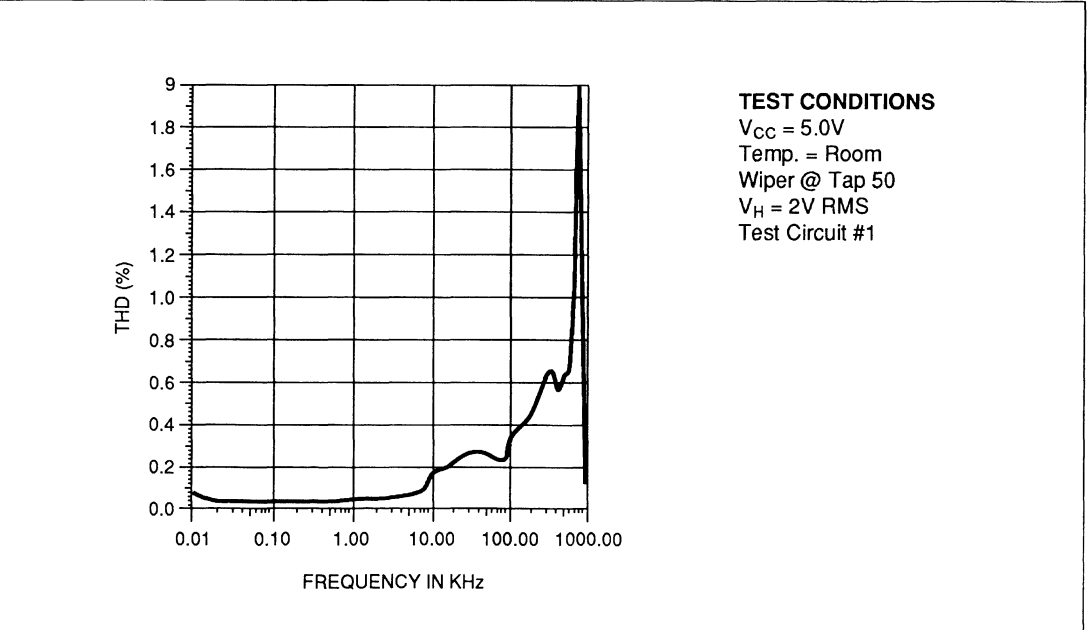


**X9CMME**

**Typical Frequency Response for X9C503**

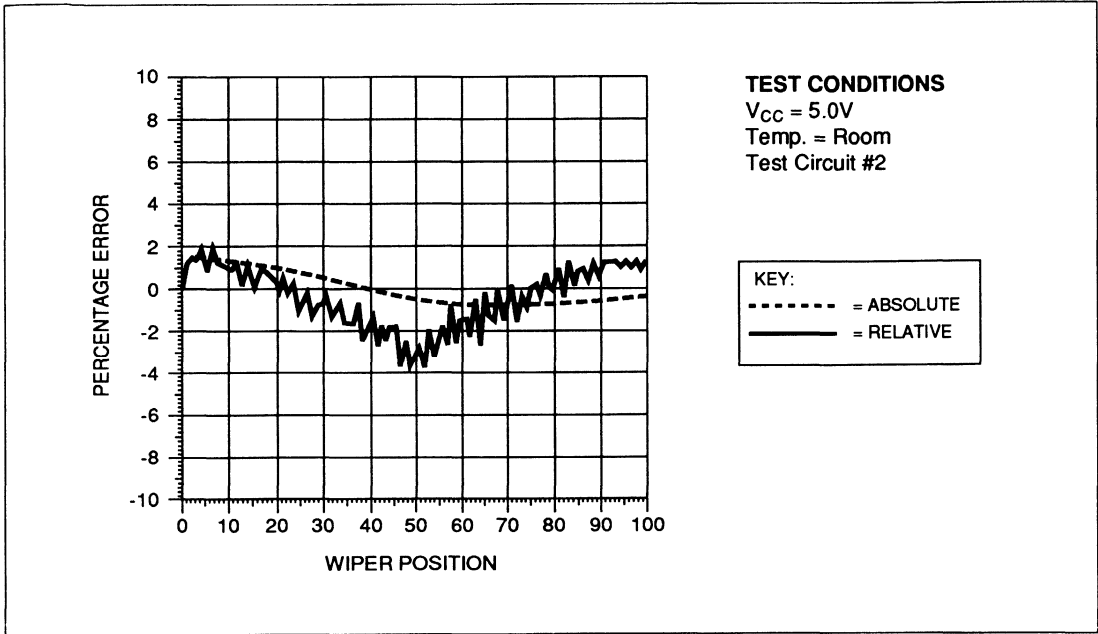


**Typical Total Harmonic Distortion for X9C503**



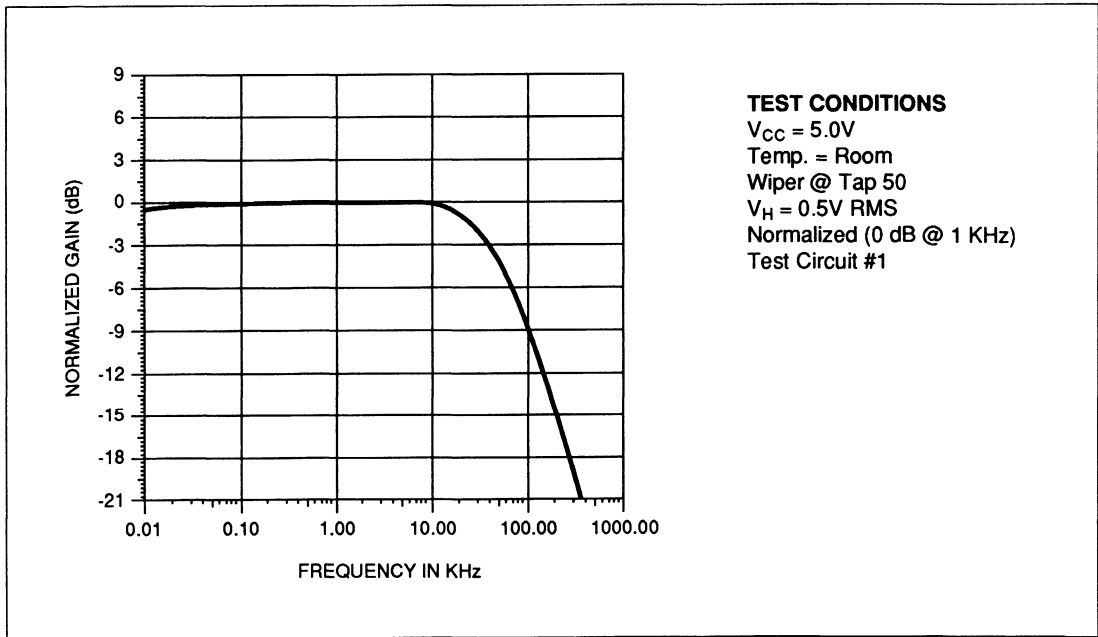
X9CMME

Typical Linearity for X9C503



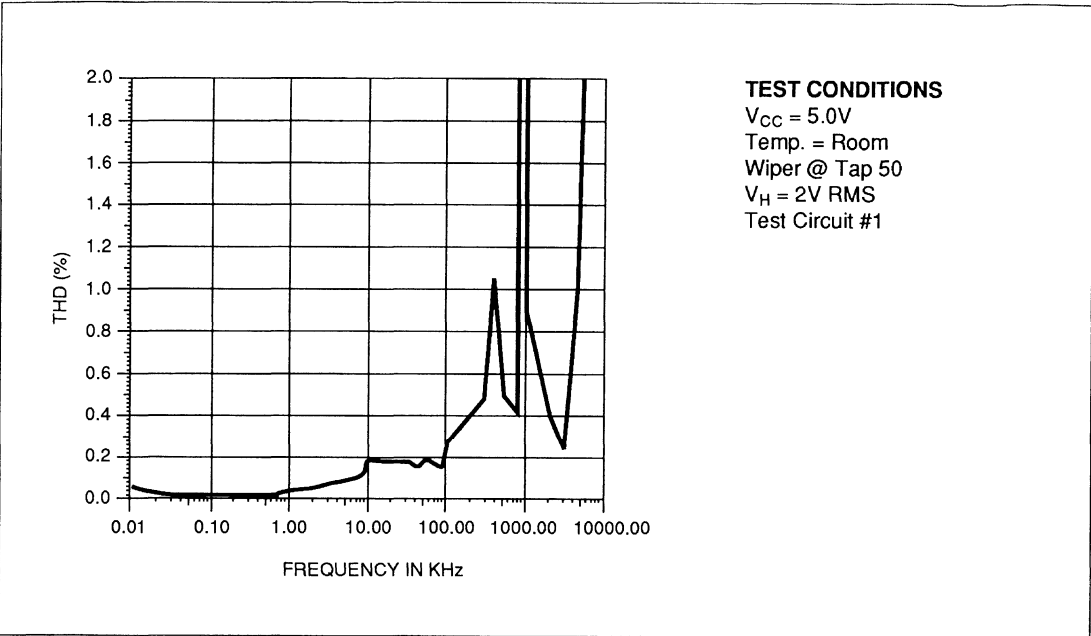
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Typical Frequency Response for X9C104

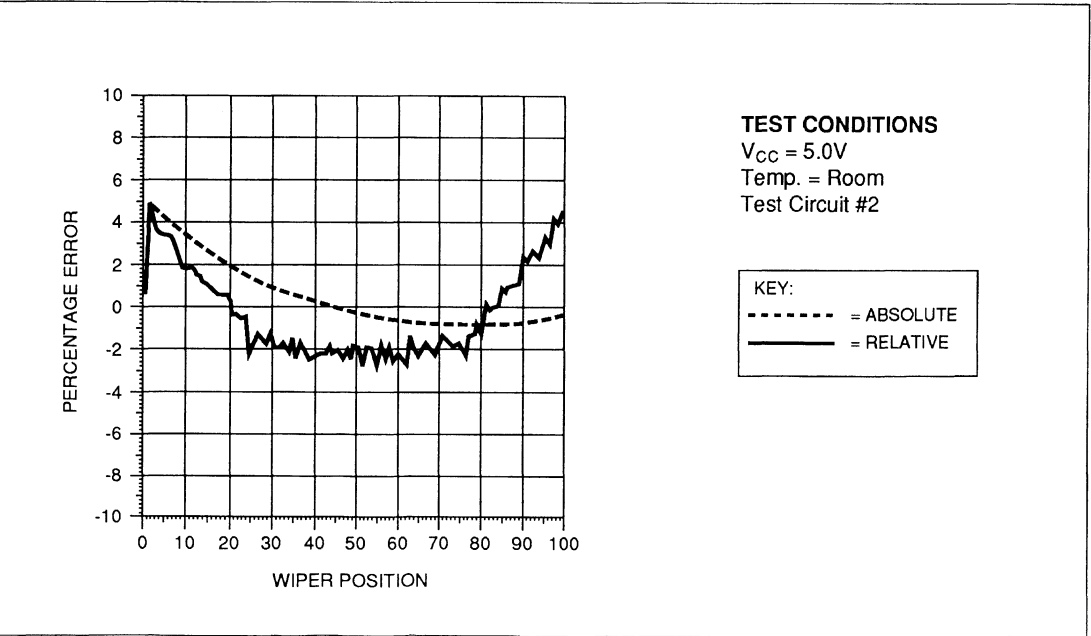


# X9CMME

Typical Total Harmonic Distortion for X9C104



Typical Linearity for X9C104



## X9311

### E<sup>2</sup>POT™ Digitally Controlled Potentiometer

#### FEATURES

- Compatible with X9MME and X9CMME
- Low Power CMOS
  - Active Current, 3 mA Max
  - Standby Current, 500  $\mu$ A Max
- 99 Resistive Elements
  - Temperature Compensated
  - $\pm 20\%$  End to End Resistance Range
  - 0 to 10V Range
- 100 Wiper Tap Points
  - Wiper Positioned via Three Wire Interface
  - Similar to TTL Up/Down Counter
  - Wiper Position Stored in Nonvolatile Memory and Recalled on Power-Up
- 100 Year Wiper Position Data Retention
- X9311Z = 1K Ohms
- X9311W = 10K Ohms
- X9311U = 50K Ohms
- X9311T = 100K Ohms

#### DESCRIPTION

The Xicor X9311 is a solid state nonvolatile potentiometer and is ideal for digitally controlled resistance trimming.

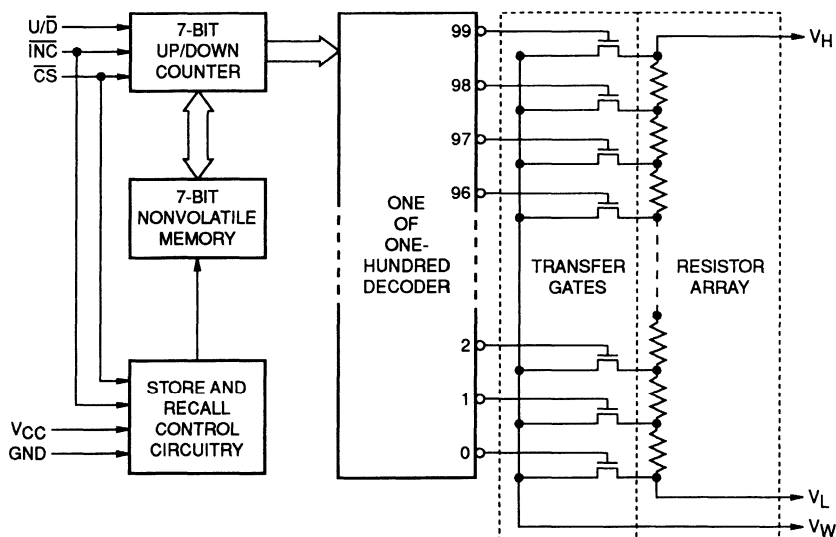
The X9311 is a resistor array composed of 99 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element is controlled by the  $\overline{CS}$ ,  $U/\overline{D}$ , and  $\overline{INC}$  inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-on operation.

The resolution of the X9311 is equal to the maximum resistance value divided by 99. As an example, for the X9311U (50 K $\Omega$ ) each tap point represents 505 $\Omega$ .

All Xicor nonvolatile memories are designed and tested for applications requiring extended endurance and data retention.

4

#### FUNCTIONAL DIAGRAM



3862 FHD F01



# X9311

## PIN DESCRIPTIONS

### $V_H$ and $V_L$

The high ( $V_H$ ) and low ( $V_L$ ) terminals of the X9311 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum and maximum voltage that may be applied to the terminals is determined by the voltage on  $V_{CC}$ . The minimum voltage is 0 and the maximum is +10. It should be noted that the terminology of  $V_L$  and  $V_H$  references the relative position of the terminal in relation to wiper movement direction selected by the  $U/\bar{D}$  input and not the voltage potential on the terminal.

### $V_W$

$V_W$  is the wiper terminal, equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically less than 40 $\Omega$ .

### Up/Down ( $U/\bar{D}$ )

The  $U/\bar{D}$  input controls the direction of the wiper movement and whether the counter is incremented or decremented.

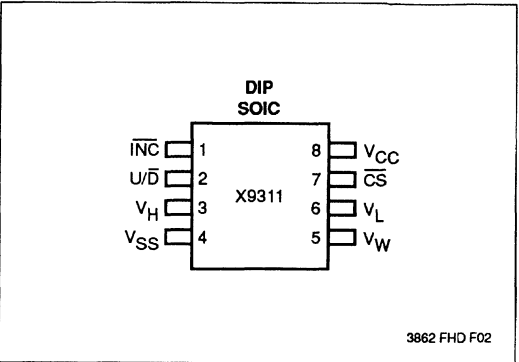
### Increment ( $\overline{INC}$ )

The  $\overline{INC}$  input is negative-edge triggered. Toggling  $\overline{INC}$  will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the  $U/\bar{D}$  input.

### Chip Select ( $\overline{CS}$ )

The device is selected when the  $\overline{CS}$  input is low. The current counter value is stored in nonvolatile memory when  $\overline{CS}$  is returned HIGH while the  $\overline{INC}$  input is also high. After the store operation is complete the X9311 will be placed in the low power standby mode until the device is selected once again.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
$V_H$	High Terminal
$V_W$	Wiper Terminal
$V_L$	Low Terminal
$V_{SS}$	Ground
$V_{CC}$	Supply Voltage
$U/\bar{D}$	Up/Down Input
$\overline{INC}$	Increment Input
$\overline{CS}$	Chip Select Input

3862 PGM T01

## X9311

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### DEVICE OPERATION

There are three basic sections of the X9311: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The  $\overline{INC}$ ,  $U/\overline{D}$  and  $\overline{CS}$  inputs control the movement of the wiper along the resistor array. With  $\overline{CS}$  set low the X9311 is selected and enabled to respond to the  $U/\overline{D}$  and  $\overline{INC}$  inputs. High to low transitions on  $\overline{INC}$  will increment or decrement (depending on the state of the  $U/\overline{D}$  input) a seven bit counter. The output of this counter is decoded to select one of one-hundred wiper positions along the resistive array.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The value of the counter is stored in nonvolatile memory whenever  $\overline{CS}$  transitions high while the  $\overline{INC}$  input is also high.

When the X9311 is powered down, the last counter position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is reset to the value last stored.

### OPERATION NOTES

The system may select the X9311, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. The wiper movement is performed as described above; once the new position is reached, the system would keep  $\overline{INC}$  low while taking  $\overline{CS}$  high. The new wiper position would be maintained until changed by the system or until a power-off/on cycle recalled the previously stored data.

This would allow the system to always power-on to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift etc.

The state of  $U/\overline{D}$  may be changed while  $\overline{CS}$  remains low. This allows the host system to enable the X9311 and then move the wiper up and down until the proper trim is attained.

#### $T_{IW}/R_{TOTAL}$

The electronic switches on the X9311 operate in a "make before break" mode when the wiper changes tap positions. If the wiper is moved several positions multiple taps are connected to the wiper for  $T_{IW}$  ( $\overline{INC}$  to  $V_W$  change). The  $R_{TOTAL}$  value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

#### $R_{TOTAL}$ with $V_{CC}$ Removed

The end to end resistance of the array will fluctuate once  $V_{CC}$  is removed.

# X9311

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	-65°C to +135°C
Storage Temperature .....	-65°C to +150°C
Voltage on $\overline{CS}$ , $\overline{INC}$ , $\overline{U/D}$ and $V_{CC}$ Referenced to Ground .....	-1.0V to +7.0V
Voltage on $V_H$ and $V_L$ Referenced to Ground .....	-1.0V to +13.0V
$\Delta V = (V_H \text{ and } V_L)$ X9311Z .....	4 V
X9311W, X9311U and X9311T .....	10 V
Lead Temperature (Soldering 10 Seconds) .....	+300°C
Wiper Current .....	$\pm 1$ mA

## ANALOG CHARACTERISTICS

### Electrical Characteristics

End-to-End Resistance Tolerance .....	$\pm 20\%$
Power Rating at 25°C X9311Z .....	16 mW
X9311W, X9311U and X9311T .....	10 mW
Wiper Current .....	$\pm 1$ mA Max.
Typical Wiper Resistance .....	40 $\Omega$ at 1 mA
Typical Noise .....	< -120 dB/ $\sqrt{\text{Hz}}$ Ref: 1 V

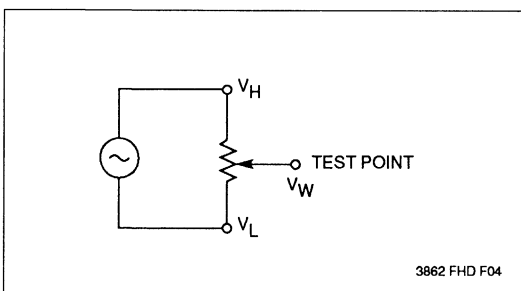
### Resolution

Resistance .....	1%
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### Linearity

Absolute Linearity <sup>(1)</sup> .....	$\pm 1.0$ MI <sup>(2)</sup>
Relative Linearity <sup>(3)</sup> .....	$\pm 0.2$ MI <sup>(2)</sup>

### Test Circuit #1



## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Temperature Coefficient

-40°C to +85°C X9311Z .....	+600 ppm/°C Typical
X9311W, X9311U, X9311T .....	+300 ppm/°C Typical
Ratiometric Temperature Coefficient .....	$\pm 20$ ppm

### Wiper Adjustability

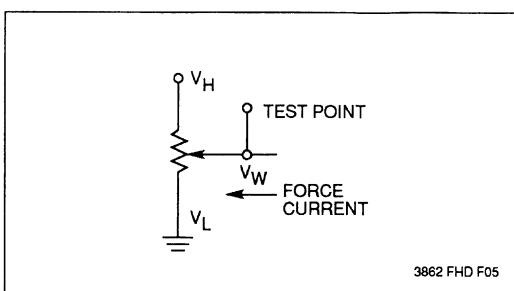
Unlimited Wiper Adjustment (Non-store operation)  
Wiper Position Store Operations .... 10,000 Cycles

### Physical Characteristics

#### Marking Includes

Manufacturer's Trademark  
Resistance Value or Code  
Date Code

### Test Circuit #2



- Notes:** (1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage  
 $= (V_{W(n)}(\text{actual}) - V_{W(n)}(\text{expected})) = \pm 1$  MI Maximum.  
 (2) 1 MI = Minimum Increment =  $R_{TOT}/99$ .  
 (3) Relative Linearity is a measure of the error in step size between taps =  $V_{W(n+1)} - [V_{W(n)} + \text{MI}] = \pm 0.2$  MI.

X9311

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(4)	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Active Current		1	3	mA	$\overline{CS} = V_{IL}$ , $U/\overline{D} = V_{IL}$ or $V_{IH}$ and $\overline{INC} = 0.4V/2.4V$ @ max. $t_{CYC}$
I <sub>SB</sub>	Standby Supply Current		200	500	μA	$CS = V_{CC} - 0.3V$ , $U/\overline{D}$ and $INC = GND$ or $V_{CC} - 0.3V$
I <sub>LI</sub>	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ Input Leakage Current			±10	μA	$V_{IN} = GND$ to $V_{CC}$
V <sub>IH</sub>	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ Input High Voltage	2.0		$V_{CC} + 1.0$	V	
V <sub>IL</sub>	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ Input Low Voltage	-1.0		0.8	V	
R <sub>W</sub>	Wiper Resistance		40	100	Ω	Max. Wiper Current ±1mA
V <sub>VH</sub>	VH Terminal Voltage	0		10	V	
V <sub>VL</sub>	VL Terminal Voltage	0		10	V	
C <sub>IN</sub> (5)	$\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ Input Capacitance			10	pF	$V_{CC} = 5.0$ , $V_{IN} = 0V$ , $T_A = 25^{\circ}C$ , $f = 1\text{ MHz}$

3862 PGM T05

STANDARD PARTS

Part Number	Maximum Resistance	Wiper Increments	Minimum Resistance
X9311Z	1 KΩ	10.1Ω	40Ω
X9311W	10 KΩ	101Ω	40Ω
X9311U	50 KΩ	505Ω	40Ω
X9311T	100 KΩ	1010Ω	40Ω

3862 PGM T08

Notes: (4) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage.  
(5) This parameter is periodically sampled and not 100% tested.

# X9311

## A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Input Reference Levels	1.5V

3862 PGM T05

## MODE SELECTION

$\overline{CS}$	$\overline{INC}$	U/D	Mode
L	$\searrow$	H	Wiper Up
L	$\searrow$	L	Wiper Down
f	H	X	Store Wiper Position
H	X	X	Standby
f	L	X	No Store, Return to Standby

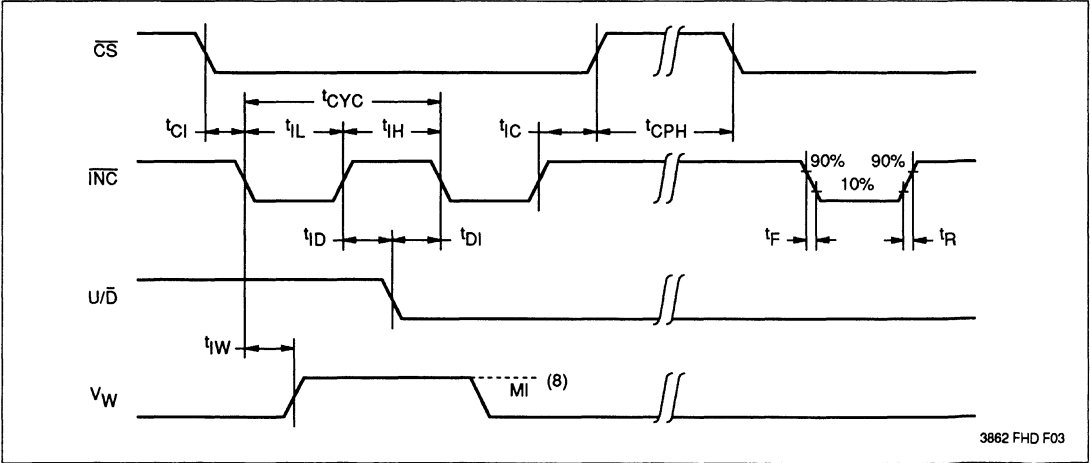
3862 PGM T06

## A.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Units
		Min.	Typ. <sup>(6)</sup>	Max.	
$t_{CI}$	$\overline{CS}$ to $\overline{INC}$ Setup	100			ns
$t_{ID}$	$\overline{INC}$ High to U/D Change	100			ns
$t_{DI}$	U/D to $\overline{INC}$ Setup	2.9			$\mu$ s
$t_{IL}$	$\overline{INC}$ Low Period	1			$\mu$ s
$t_{IH}$	$\overline{INC}$ High Period	1			$\mu$ s
$t_{IC}$	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			$\mu$ s
$t_{CPH}$	$\overline{CS}$ Deselect Time	20			ms
$t_{IW}$	$\overline{INC}$ to $V_W$ Change		100	500	$\mu$ s
$t_{CYC}$	$\overline{INC}$ Cycle Time	4			$\mu$ s
$t_R, t_F^{(7)}$	$\overline{INC}$ Input Rise and Fall Time			500	$\mu$ s
$t_{PU}^{(7)}$	Power up to Wiper Stable			500	$\mu$ s
$t_R V_{CC}^{(7)}$	$V_{CC}$ Rise Time	0.5			V/ $\mu$ s

3862 PGM T07

## A.C. Timing



Notes: (6) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.

(7) This parameter is periodically sampled and not 100% tested.

(8) MI in the A.C. timing diagram refers to the minimum incremental change in the V output due to a change in the wiper position.



Advance Information  
Terminal Voltage 0V to +15V

## X9312

### E<sup>2</sup>POT™ Digitally Controlled Potentiometer

#### FEATURES

- Compatible with X9MME and X9CMME
- Low Power CMOS
  - Active Current, 3 mA Max
  - Standby Current, 500  $\mu$ A Max
- 99 Resistive Elements
  - Temperature Compensated
  - $\pm 20\%$  End to End Resistance Range
  - 0 to 15V Range
- 100 Wiper Tap Points
  - Wiper Positioned via Three Wire Interface
  - Similar to TTL Up/Down Counter
  - Wiper Position Stored In Nonvolatile Memory and Recalled on Power-Up
- 100 Year Wiper Position Data Retention
- X9312W = 10K Ohms
- X9312U = 50K Ohms
- X9312T = 100K Ohms

#### DESCRIPTION

The Xicor X9312 is a solid state nonvolatile potentiometer and is ideal for digitally controlled resistance trimming.

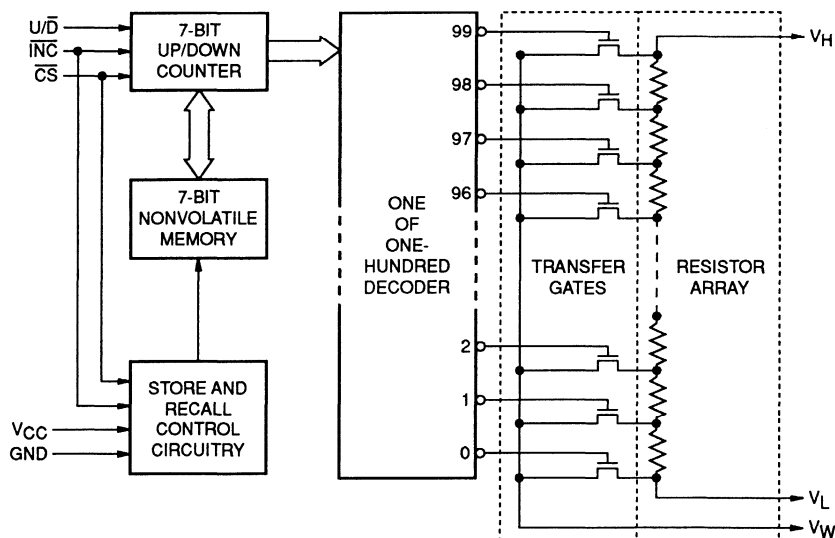
The X9312 is a resistor array composed of 99 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element is controlled by the  $\overline{CS}$ , U/D, and  $\overline{INC}$  inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-on operation.

The resolution of the X9312 is equal to the maximum resistance value divided by 99. As an example, for the X9312U (50 K $\Omega$ ) each tap point represents 505 $\Omega$ .

All Xicor nonvolatile memories are designed and tested for applications requiring extended endurance and data retention.

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#### FUNCTIONAL DIAGRAM



3865 FHD F01

E<sup>2</sup>POT™ is a trademark of Xicor, Inc.

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# X9312

## PIN DESCRIPTIONS

### $V_H$ and $V_L$

The high ( $V_H$ ) and low ( $V_L$ ) terminals of the X9312 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum and maximum voltage that may be applied to the terminals is determined by the voltage on  $V_{CC}$ . The minimum voltage is 0 and the maximum is +15. It should be noted that the terminology of  $V_L$  and  $V_H$  references the relative position of the terminal in relation to wiper movement direction selected by the  $U/\bar{D}$  input and not the voltage potential on the terminal.

### $V_W$

$V_W$  is the wiper terminal, equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically less than 40 $\Omega$ .

### Up/Down ( $U/\bar{D}$ )

The  $U/\bar{D}$  input controls the direction of the wiper movement and whether the counter is incremented or decremented.

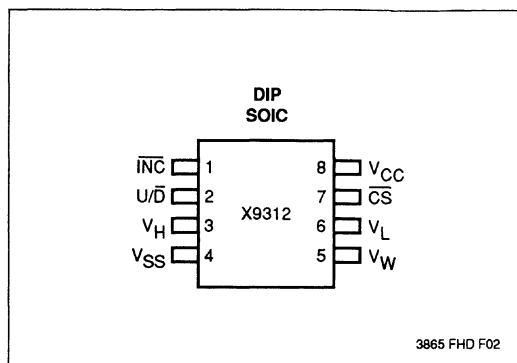
### Increment ( $\overline{INC}$ )

The  $\overline{INC}$  input is negative-edge triggered. Toggling  $\overline{INC}$  will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the  $U/\bar{D}$  input.

### Chip Select ( $\overline{CS}$ )

The device is selected when the  $\overline{CS}$  input is low. The current counter value is stored in nonvolatile memory when  $\overline{CS}$  is returned HIGH while the  $\overline{INC}$  input is also high. After the store operation is complete the X9312 will be placed in the low power standby mode until the device is selected once again.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
$V_H$	High Terminal
$V_W$	Wiper Terminal
$V_L$	Low Terminal
$V_{SS}$	Ground
$V_{CC}$	Supply Voltage
$U/\bar{D}$	Up/Down Input
$\overline{INC}$	Increment Input
$\overline{CS}$	Chip Select Input

3865 PGM T01

## X9312

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### DEVICE OPERATION

There are three basic sections of the X9312: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 99 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The  $\overline{INC}$ ,  $U/\overline{D}$  and  $\overline{CS}$  inputs control the movement of the wiper along the resistor array. With  $\overline{CS}$  set low the X9312 is selected and enabled to respond to the  $U/\overline{D}$  and  $\overline{INC}$  inputs. High to low transitions on  $\overline{INC}$  will increment or decrement (depending on the state of the  $U/\overline{D}$  input) a seven bit counter. The output of this counter is decoded to select one of one-hundred wiper positions along the resistive array.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The value of the counter is stored in nonvolatile memory whenever  $\overline{CS}$  transitions high while the  $\overline{INC}$  input is also high.

When the X9312 is powered down, the last counter position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is reset to the value last stored.

### Operation Notes

The system may select the X9312, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. The wiper movement is performed as described above; once the new position is reached, the system would keep  $\overline{INC}$  low while taking  $\overline{CS}$  high. The new wiper position would be maintained until changed by the system or until a power-off/on cycle recalled the previously stored data.

This would allow the system to always power-on to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift etc.

The state of  $U/\overline{D}$  may be changed while  $\overline{CS}$  remains low. This allows the host system to enable the X9312 and then move the wiper up and down until the proper trim is attained.

#### $T_{IW}/R_{TOTAL}$

The electronic switches on the X9312 operate in a "make before break" mode when the wiper changes tap positions. If the wiper is moved several positions multiple taps are connected to the wiper for  $T_{IW}$  ( $\overline{INC}$  to  $V_W$  change). The  $R_{TOTAL}$  value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

#### $R_{TOTAL}$ with $V_{CC}$ Removed

The end to end resistance of the array will fluctuate once  $V_{CC}$  is removed.



X9312

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....-65°C to +135°C  
Storage Temperature .....-65°C to +150°C  
Voltage on CS, INC, U/D and V<sub>CC</sub>  
    Referenced to Ground .....-1.0V to +7.0V  
Voltage on V<sub>H</sub> and V<sub>L</sub> Referenced to Ground  
ΔV = (V<sub>H</sub> and V<sub>L</sub>)  
    X9312W, X9312U and X9312T ..... 15 V  
Lead Temperature (Soldering 10 Seconds) .....+300°C  
Wiper Current .....±1 mA

ANALOG CHARACTERISTICS

Electrical Characteristics

End-to-End Resistance Tolerance .....±20%  
Power Rating at 25°C  
    X9312W, X9312U and X9312T ..... 15 mW  
Wiper Current .....±1 mA Max.  
Typical Wiper Resistance .....40Ω at 1 mA  
Typical Noise .....< -120 dB/√ Hz Ref: 1 V

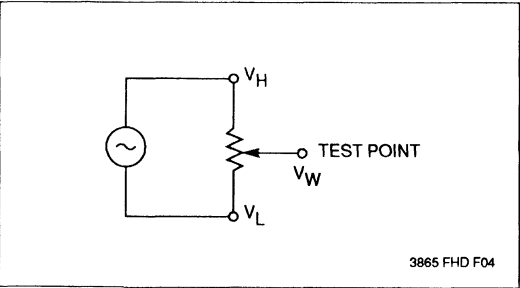
Resolution

Resistance ..... 1%

Linearity

Absolute Linearity<sup>(1)</sup> .....±1.0 MI<sup>(2)</sup>  
Relative Linearity<sup>(3)</sup> .....±0.2 MI<sup>(2)</sup>

Test Circuit #1



\*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Temperature Coefficient

-40°C to +85°C  
X9312W, X9312U and X9312T ..+300 ppm/°C Typical  
Ratiometric Temperature Coefficient .....±20 ppm

Wiper Adjustability

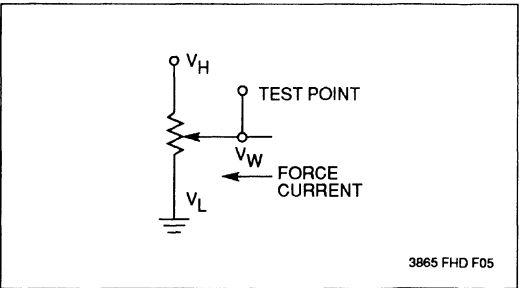
Unlimited Wiper Adjustment (Non-store operation)  
Wiper Position Store Operations .... 10,000 Cycles

Physical Characteristics

Marking Includes

Manufacturer's Trademark  
Resistance Value or Code  
Date Code

Test Circuit #2



- Notes: (1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage  
    = (V<sub>w(n)</sub>(actual) - V<sub>w(n)</sub>(expected)) = ±1 MI Maximum.  
(2) 1 MI = Minimum Increment = R<sub>TOY</sub>/99.  
(3) Relative Linearity is a measure of the error in step size between taps = V<sub>w(n+1)</sub> - [V<sub>w(n)</sub> + MI] = +0.2 MI.

X9312

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

3865 PGM T03

Supply Voltage	Limits
X9312	5V ± 10%

3865 PGM T04

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(4)	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Active Current		1	3	mA	CS = V <sub>IL</sub> , U/D = V <sub>IL</sub> or V <sub>IH</sub> and INC = 0.4V/2.4V @ max. t <sub>CYC</sub>
I <sub>SB</sub>	Standby Supply Current		200	500	μA	CS = V <sub>CC</sub> − 0.3V, U/D and INC = GND or V <sub>CC</sub> − 0.3V
I <sub>LI</sub>	CS, INC, U/D Input Leakage Current			±10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
V <sub>IH</sub>	CS, INC, U/D Input High Voltage	2.0		V <sub>CC</sub> + 1.0	V	
V <sub>IL</sub>	CS, INC, U/D Input Low Voltage	−1.0		0.8	V	
R <sub>W</sub>	Wiper Resistance		40	100	Ω	Max. Wiper Current ±1mA
V <sub>VH</sub>	VH Terminal Voltage	0		15	V	
V <sub>VL</sub>	VL Terminal Voltage	0		15	V	
C <sub>IN</sub> (5)	CS, INC, U/D Input Capacitance			10	pF	V <sub>CC</sub> = 5.0, V <sub>IN</sub> = 0V, T <sub>A</sub> = 25°C, f = 1 MHz

3865 PGM T05

STANDARD PARTS

Part Number	Maximum Resistance	Wiper Increments	Minimum Resistance
X9312W	10 KΩ	101Ω	40Ω
X9312U	50 KΩ	505Ω	40Ω
X9312T	100 KΩ	1010Ω	40Ω

3865 PGM T08

Notes: (4) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage.  
(5) This parameter is periodically sampled and not 100% tested.

# X9312

## A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Input Reference Levels	1.5V

3865 PGM T05

## MODE SELECTION

$\overline{CS}$	$\overline{INC}$	U/D	Mode
L	$\searrow$	H	Wiper Up
L	$\swarrow$	L	Wiper Down
f	H	X	Store Wiper Position
H	X	X	Standby
f	L	X	No Store, Return to Standby

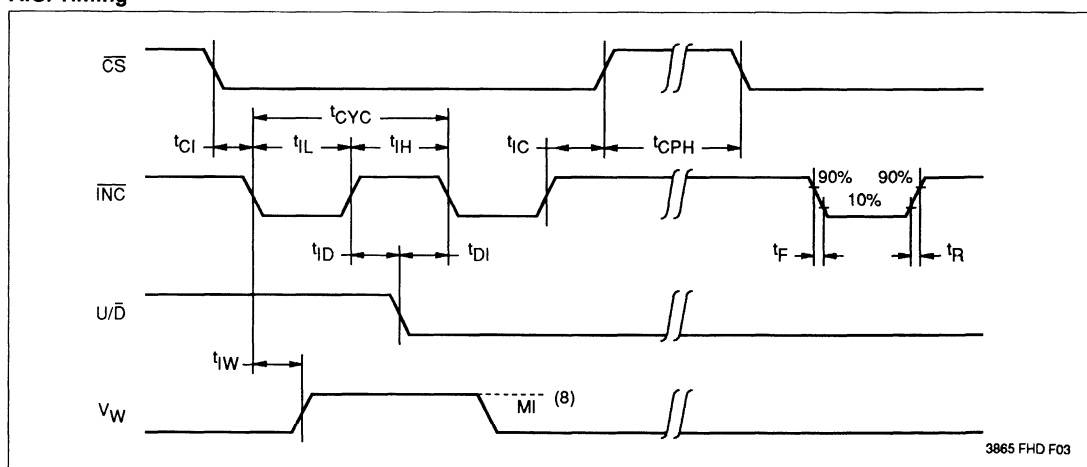
3865 PGM T06

## A.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Units
		Min.	Typ.(6)	Max.	
$t_{CI}$	$\overline{CS}$ to $\overline{INC}$ Setup	100			ns
$t_{ID}$	$\overline{INC}$ High to U/D Change	100			ns
$t_{DI}$	U/D to $\overline{INC}$ Setup	1			$\mu$ s
$t_{IL}$	$\overline{INC}$ Low Period	.5			$\mu$ s
$t_{IH}$	$\overline{INC}$ High Period	.5			$\mu$ s
$t_{IC}$	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			$\mu$ s
$t_{CPH}$	$\overline{CS}$ Deselect Time	20			ms
$t_{IW}$	$\overline{INC}$ to $V_W$ Change		100	500	$\mu$ s
$t_{CYC}$	$\overline{INC}$ Cycle Time	1			$\mu$ s
$t_R, t_F^{(7)}$	$\overline{INC}$ Input Rise and Fall Time			500	$\mu$ s
$t_{PU}^{(7)}$	Power up to Wiper Stable			500	$\mu$ s
$t_R V_{CC}^{(7)}$	$V_{CC}$ Rise Time	0.5			V/ $\mu$ s

3865 PGM T07

## A.C. Timing



3865 FHD F03

Notes: (6) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.

(7) This parameter is periodically sampled and not 100% tested.

(8) MI in the A.C. timing diagram refers to the minimum incremental change in the  $V_W$  output due to a change in the wiper position.

## X9313

### E<sup>2</sup>POT™ Digitally Controlled Potentiometer

#### FEATURES

- Compatible with X9MME and X9CMME
- Low Power CMOS
  - Active Current, 3 mA Max
  - Standby Current, 500  $\mu$ A Max
- 31 Resistive Elements
  - Temperature Compensated
  - $\pm 20\%$  End to End Resistance Range
  - $-5V$  to  $+5V$  Range
- 32 Wiper Tap Points
  - Wiper Positioned via Three Wire Interface
  - Similar to TTL Up/Down Counter
  - Wiper Position Stored in Nonvolatile Memory and Recalled on Power-Up
- 100 Year Wiper Position Data Retention
- X9313Z = 1K Ohms
- X9313W = 10K Ohms

#### DESCRIPTION

The Xicor X9313 is a solid state nonvolatile potentiometer and is ideal for digitally controlled resistance trimming.

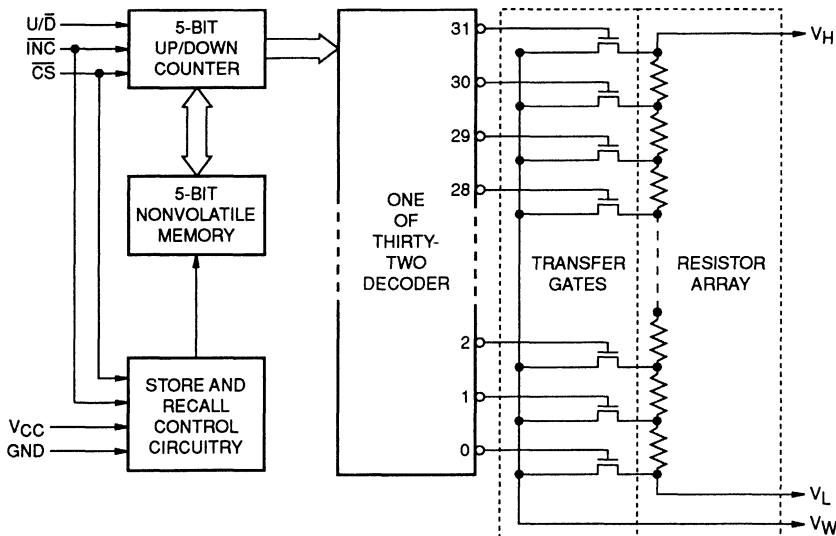
The X9313 is a resistor array composed of 31 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element is controlled by the  $\overline{CS}$ ,  $U/\overline{D}$ , and  $\overline{INC}$  inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-on operation.

The resolution of the X9313 is equal to the maximum resistance value divided by 31. As an example, for the X9313W (10 K $\Omega$ ) each tap point represents 323 $\Omega$ .

All Xicor nonvolatile memories are designed and tested for applications requiring extended endurance and data retention.

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#### FUNCTIONAL DIAGRAM



3866 F:H:D F01

# X9313

## PIN DESCRIPTIONS

### $V_H$ and $V_L$

The high ( $V_H$ ) and low ( $V_L$ ) terminals of the X9313 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum and maximum voltage that may be applied to the terminals is determined by the voltage on  $V_{CC}$ . The minimum voltage is  $-5$  and the maximum is  $+5$ . It should be noted that the terminology of  $V_L$  and  $V_H$  references the relative position of the terminal in relation to wiper movement direction selected by the  $U/\overline{D}$  input and not the voltage potential on the terminal.

### $V_W$

$V_W$  is the wiper terminal, equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically less than  $40\Omega$ .

### Up/Down ( $U/\overline{D}$ )

The  $U/\overline{D}$  input controls the direction of the wiper movement and whether the counter is incremented or decremented.

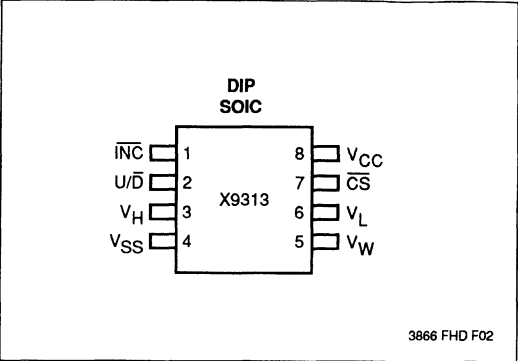
### Increment ( $\overline{INC}$ )

The  $\overline{INC}$  input is negative-edge triggered. Toggling  $\overline{INC}$  will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the  $U/\overline{D}$  input.

### Chip Select ( $\overline{CS}$ )

The device is selected when the  $\overline{CS}$  input is low. The current counter value is stored in nonvolatile memory when  $\overline{CS}$  is returned HIGH while the  $\overline{INC}$  input is also high. After the store operation is complete the X9313 will be placed in the low power standby mode until the device is selected once again.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
$V_H$	High Terminal
$V_W$	Wiper Terminal
$V_L$	Low Terminal
$V_{SS}$	Ground
$V_{CC}$	Supply Voltage
$U/\overline{D}$	Up/Down Input
$\overline{INC}$	Increment Input
$\overline{CS}$	Chip Select Input

3866 PGM T01

## X9313

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### DEVICE OPERATION

There are three basic sections of the X9313: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The  $\overline{\text{INC}}$ ,  $\text{U}/\overline{\text{D}}$  and  $\overline{\text{CS}}$  inputs control the movement of the wiper along the resistor array. With  $\overline{\text{CS}}$  set low the X9313 is selected and enabled to respond to the  $\text{U}/\overline{\text{D}}$  and  $\overline{\text{INC}}$  inputs. High to low transitions on  $\overline{\text{INC}}$  will increment or decrement (depending on the state of the  $\text{U}/\overline{\text{D}}$  input) a seven bit counter. The output of this counter is decoded to select one of one-hundred wiper positions along the resistive array.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The value of the counter is stored in nonvolatile memory whenever  $\overline{\text{CS}}$  transitions high while the  $\overline{\text{INC}}$  input is also high.

When the X9313 is powered down, the last counter position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is reset to the value last stored.

### Operation Notes

The system may select the X9313, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. The wiper movement is performed as described above; once the new position is reached, the system would keep  $\overline{\text{INC}}$  low while taking  $\overline{\text{CS}}$  high. The new wiper position would be maintained until changed by the system or until a power-off/on cycle recalled the previously stored data.

This would allow the system to always power-on to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift etc.

The state of  $\text{U}/\overline{\text{D}}$  may be changed while  $\overline{\text{CS}}$  remains low. This allows the host system to enable the X9313 and then move the wiper up and down until the proper trim is attained.

### $T_{\text{IW}}/R_{\text{TOTAL}}$

The electronic switches on the X9313 operate in a "make before break" mode when the wiper changes tap positions. If the wiper is moved several positions multiple taps are connected to the wiper for  $T_{\text{IW}}$  ( $\overline{\text{INC}}$  to  $V_{\text{W}}$  change). The  $R_{\text{TOTAL}}$  value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

### $R_{\text{TOTAL}}$ with $V_{\text{CC}}$ Removed

The end to end resistance of the array will fluctuate once  $V_{\text{CC}}$  is removed.

# X9313

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	-65°C to +135°C
Storage Temperature .....	-65°C to +150°C
Voltage on $\overline{CS}$ , $\overline{INC}$ , $U/\overline{D}$ and $V_{CC}$ Referenced to Ground .....	-1.0V to +7.0V
Voltage on $V_H$ and $V_L$ Referenced to Ground $\Delta V = (V_H \text{ and } V_L)$ .....	4V
X9313Z .....	10 V
X9313W .....	10 V
Lead Temperature (Soldering 10 Seconds) .....	+300°C
Wiper Current .....	$\pm 1$ mA

## ANALOG CHARACTERISTICS

### Electrical Characteristics

End-to-End Resistance Tolerance .....	$\pm 20\%$
Power Rating at 25°C .....	
X9313Z .....	16 mW
X9313W .....	10 mW
Wiper Current .....	$\pm 1$ mA Max.
Typical Wiper Resistance .....	40 $\Omega$ at 1 mA
Typical Noise .....	< -120 dB/ $\sqrt{\text{Hz}}$ Ref: 1 V

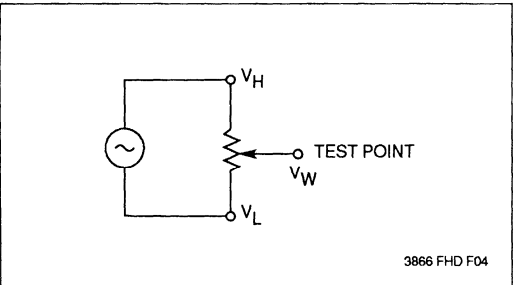
### Resolution

Resistance .....	3%
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### Linearity

Absolute Linearity <sup>(1)</sup> .....	$\pm 1.0$ MI <sup>(2)</sup>
Relative Linearity <sup>(3)</sup> .....	$\pm 0.2$ MI <sup>(2)</sup>

### Test Circuit #1



## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Temperature Coefficient

-40°C to +85°C .....	
X9313Z .....	+600 ppm/°C Typical
X9313W .....	+300 ppm/°C Typical
Ratiometric Temperature Coefficient .....	$\pm 20$ ppm

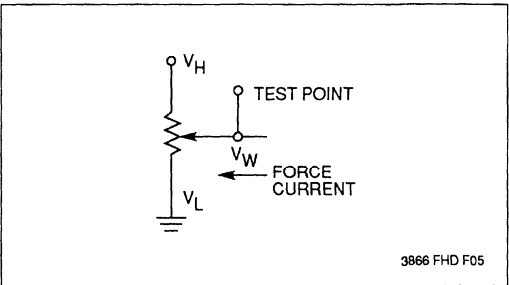
### Wiper Adjustability

Unlimited Wiper Adjustment (Non-store operation)  
Wiper Position Store Operations .... 10,000 Cycles

### Physical Characteristics

Marking Includes  
Manufacturer's Trademark  
Resistance Value or Code  
Date Code

### Test Circuit #2



**Notes:** (1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage  
 $= (V_{W(n)}(\text{actual}) - V_{W(n)}(\text{expected})) = \pm 1$  MI Maximum.  
(2) 1 MI = Minimum Increment =  $R_{TOT}/31$ .  
(3) Relative Linearity is a measure of the error in step size between taps =  $V_{W(n+1)} - [V_{W(n)} + \text{MI}] = +0.2$  MI.

# X9313

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

3866 PGM T03

Supply Voltage	Limits
X9313	5V ± 10%

3866 PGM T04

## D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(4)	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Active Current		1	3	mA	$\overline{CS} = V_{IL}$ , $U/\overline{D} = V_{IL}$ or $V_{IH}$ and $INC = 0.4V/2.4V$ @ max. $t_{CYC}$
I <sub>SB</sub>	Standby Supply Current		200	500	μA	$CS = V_{CC} - 0.3V$ , $U/\overline{D}$ and $INC = GND$ or $V_{CC} - 0.3V$
I <sub>LI</sub>	$\overline{CS}$ , $INC$ , $U/\overline{D}$ Input Leakage Current			±10	μA	$V_{IN} = GND$ to $V_{CC}$
V <sub>IH</sub>	$\overline{CS}$ , $INC$ , $U/\overline{D}$ Input High Voltage	2.0		$V_{CC} + 1.0$	V	
V <sub>IL</sub>	$\overline{CS}$ , $INC$ , $U/\overline{D}$ Input Low Voltage	-1.0		0.8	V	
R <sub>W</sub>	Wiper Resistance		40	100	Ω	Max. Wiper Current ±1mA
V <sub>VH</sub>	VH Terminal Voltage	-5		+5	V	
V <sub>VL</sub>	VL Terminal Voltage	-5		+5	V	
C <sub>IN</sub> (5)	$\overline{CS}$ , $INC$ , $U/\overline{D}$ Input Capacitance			10	pF	$V_{CC} = 5.0$ , $V_{IN} = 0V$ , $T_A = 25^\circ C$ , $f = 1$ MHz

3866 PGM T05

## STANDARD PARTS

Part Number	Maximum Resistance	Wiper Increments	Minimum Resistance
X9313Z	1 KΩ	32.3Ω	40Ω
X9313W	10 KΩ	323Ω	40Ω

3866 PGM T06

**Notes:** (4) Typical values are for  $T_A = 25^\circ C$  and nominal supply voltage.  
(5) This parameter is periodically sampled and not 100% tested.

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X9313

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Input Reference Levels	1.5V

3866 PGM T05

MODE SELECTION

CS	INC	U/D	Mode
L	$\downarrow$	H	Wiper Up
L	$\downarrow$	L	Wiper Down
f	H	X	Store Wiper Position
H	X	X	Standby
f	L	X	No Store, Return to Standby

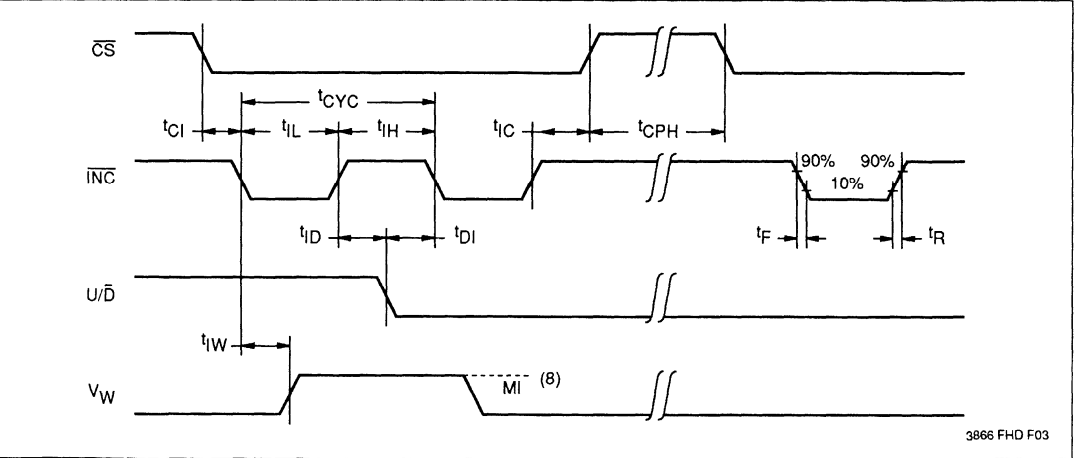
3866 PGM T06

A.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Units
		Min.	Typ.(6)	Max.	
t <sub>CI</sub>	CS to INC Setup	100			ns
t <sub>ID</sub>	INC High to U/D Change	100			ns
t <sub>DI</sub>	U/D to INC Setup	2.9			μs
t <sub>IL</sub>	INC Low Period	1			μs
t <sub>IH</sub>	INC High Period	1			μs
t <sub>IC</sub>	INC Inactive to CS Inactive	1			μs
t <sub>CPH</sub>	CS Deselect Time	20			ms
t <sub>IW</sub>	INC to V <sub>w</sub> Change		100	500	μs
t <sub>CYC</sub>	INC Cycle Time	4			μs
t <sub>R</sub> , t <sub>F</sub> (7)	INC Input Rise and Fall Time			500	μs
t <sub>PU</sub> (7)	Power up to Wiper Stable			500	μs
t <sub>R</sub> V <sub>CC</sub> (7)	V <sub>CC</sub> Rise Time	0.5			V/μs

3866 PGM T07

A.C. Timing



3866 FHD F03

Notes: (6) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage.

(7) This parameter is periodically sampled and not 100% tested.

(8) MI in the A.C. timing diagram refers to the minimum incremental change in the V<sub>w</sub> output due to a change in the wiper position.

### X9241

#### Quad E<sup>2</sup>POT™ Nonvolatile Potentiometer

##### FEATURES

- Four E<sup>2</sup>POTs In One Package
- Two Wire Serial Interface
- Register Oriented Format
  - Directly Write Wiper Position
  - Read Wiper Position
  - Store as Many as Four Positions per Pot
- Instruction Format
  - Quick Transfer of Register Contents to Resistor Array
  - Cascade Resistor Arrays
- Low Power CMOS
- Direct Write Cell
  - Endurance - 100,000 Writes per Register
  - Register Data Retention - 100 years
- 16 Bytes of E<sup>2</sup>PROM memory
- 3 Resistor Array Values
  - 2K to 50K Ohms Mask Programmable
  - Cascadable For Values of .5K to 200K Ohms
- Resolution: 64 Taps each pot
- 20-Pin Plastic DIP and 20-Lead SOIC Packages

##### DESCRIPTION

The X9241 integrates four nonvolatile E<sup>2</sup>POT digitally controlled potentiometers on a monolithic CMOS micro-circuit.

The X9241 contains four resistor arrays, each composed of 63 resistive elements. Between each element and at either end are tap points accessible to the wiper elements. The position of the wiper element on the array is controlled by the user through the two wire serial bus interface.

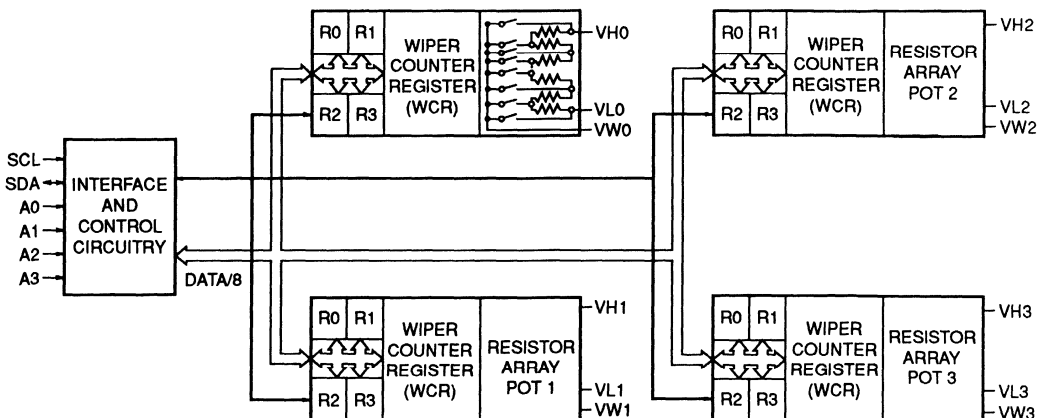
Each resistor array has associated with it a wiper counter register and four 8-bit data registers that can be directly written and read by the user. The contents of the wiper counter register control the position of the wiper on the resistor array.

The data register may be read or written by the user. The contents of the data registers can be transferred to the wiper counter register to position the wiper. The current wiper position can be transferred to any one of its associated data registers.

The arrays may be cascaded to form resistive elements with 127, 190 or 253 taps.

4

##### FUNCTIONAL DIAGRAM



3864 FHD F07

# X9241

## PIN DESCRIPTIONS

### Host Interface Pins

#### Serial Clock (SCL)

The SCL input is used to clock data into and out of the X9241.

#### Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values refer to the guidelines for calculating typical values of Bus Pull-Up Resistors graph.

#### Address

The Address inputs are used to set the least significant 4 bits of the 8 bit slave address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9241

### Potentiometer Pins

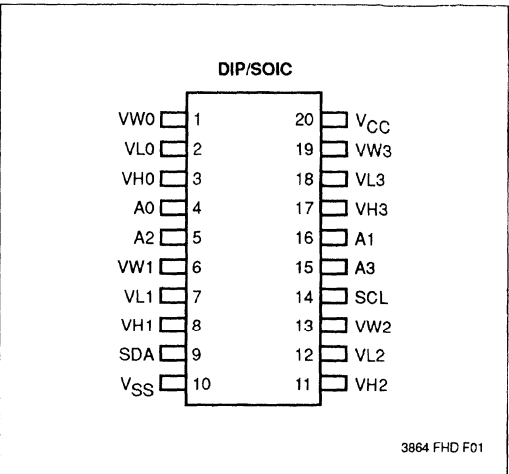
**V<sub>H</sub>** (V<sub>H0</sub> – V<sub>H3</sub>), **V<sub>L</sub>** (V<sub>L0</sub> – V<sub>L3</sub>)

The VH and VL inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

**V<sub>W</sub>** (V<sub>W0</sub> – V<sub>W3</sub>)

The wiper outputs are equivalent to the wiper output of a mechanical potentiometer.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
SCL	Serial Clock
SDA	Serial Data
A0–A3	Address
V <sub>H0</sub> –V <sub>H3</sub> , V <sub>L0</sub> –V <sub>L0</sub>	Potentiometers (terminal equivalent)
V <sub>W0</sub> –V <sub>W0</sub>	Potentiometers (wiper equivalent)

3864 PGM T01

# X9241

## PRINCIPLES OF OPERATION

The X9241 is a highly integrated microcircuit incorporating four resistor arrays, their associated registers and counters and the serial interface logic providing direct communication between the host and the E<sup>2</sup>POT potentiometers.

### Serial Interface

The X9241 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9241 will be considered a slave device in all applications.

### Clock and Data Conventions

Data states on the SDA line can change only during SCL low periods ( $t_{LOW}$ ). SDA state changes during SCL High are reserved for indicating start and stop conditions.

### Start Condition

All commands to the X9241 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH ( $t_{HIGH}$ ). The X9241 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

### Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

### Acknowledge

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data. See Figure 7.

The X9241 will respond with an acknowledge after recognition of a start condition and its slave address and

once again after successful receipt of the command byte. If the command is followed by a data byte the X9241 will respond with a final acknowledge.

### Array Description

The X9241 is comprised of four resistor arrays. Each array contains 63 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer ( $V_H$  and  $V_L$  inputs).

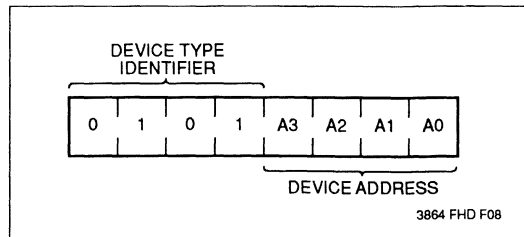
At both ends of each array and between each resistor segment is a FET switch connected to the wiper ( $V_W$ ) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by the Wiper Counter Register (WCR). The six least significant bits of the WCR are decoded to select, and enable, one of sixty-four switches.

The WCR may be written directly, or it can be changed by transferring the contents of one of four associated data registers into the WCR. These data registers and the WCR can be read and written by the host system.

### Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (refer to Figure 1 below) For the X9241 this is fixed as 0101[B].

Figure 1. Slave Address

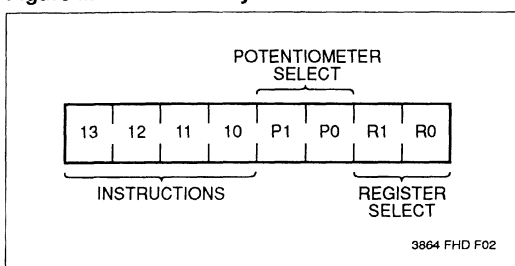


The next four bits of the slave address are the device address. The physical device address is defined by the state of the A0-A3 inputs. The X9241 compares the serial data stream with the Address input state; a successful compare of all four address bits is required for the X9241 to respond with an acknowledge.

## Instruction Structure

The next byte sent to the X9241 contains the instruction and register pointer information. The four most significant bits are the instruction. The next four bits point to one of four pots and when applicable they point to one of four associated registers. The format is shown below in Figure 2.

**Figure 2. Instruction Byte Format**



The four high order bits define the instruction. The next two bits (P1 and P0) select which one of the four potentiometers is to be affected by the instruction. The last two bits (R1 and R0) select one of the four registers that is to be acted upon when a register oriented instruction is issued.

Four of the nine instructions end with the transmission of the instruction byte. The basic sequence is illustrated in Figure 3. These two-byte instructions exchange data between the WCR and one of the data registers. A transfer from a data register to a WCR is essentially a write to a Static RAM. The response of the wiper to this

action will be delayed  $t_{STPWV}$ . A transfer from WCR current wiper position, to a data register is a write to nonvolatile memory and takes a minimum of  $t_{WR}$  to complete. The transfer can occur between one of the four potentiometers and one of its associated registers; or it may occur globally, wherein the transfer occurs between all four of the potentiometers and one of their associated registers.

Four instructions require a three byte sequence to complete. These instructions transfer data between the host and the X9241; either between the host and one of the data registers or directly between the host and the WCR. These instructions are: Read WCR, read the current wiper position of the selected pot; Write WCR, change current wiper position of the selected pot; Read Data Register, read the contents of the selected non-volatile register; Write Data Register, write a new value to the selected data register. The sequence of operations is shown in Figure 4.

The Increment/decrement command is different from the other commands. Once the command is issued and the X9241 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse ( $t_{HIGH}$ ) while SDA is HIGH, the selected wiper will move one resistor segment towards the  $V_H$  terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the  $V_L$  terminal. A detailed illustration of the sequence and timing for this operation are shown in Figures 5 and 6 respectively.

**Figure 3. Two-Byte Command Sequence**

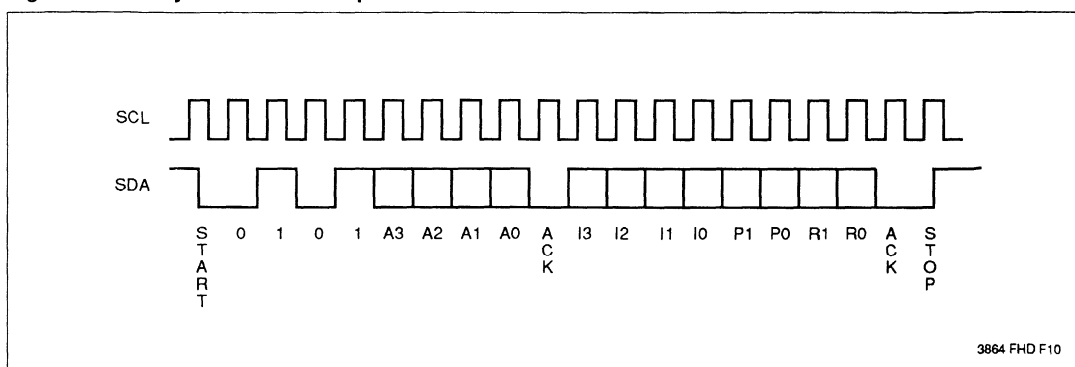


Figure 4. Three-Byte Command Sequence

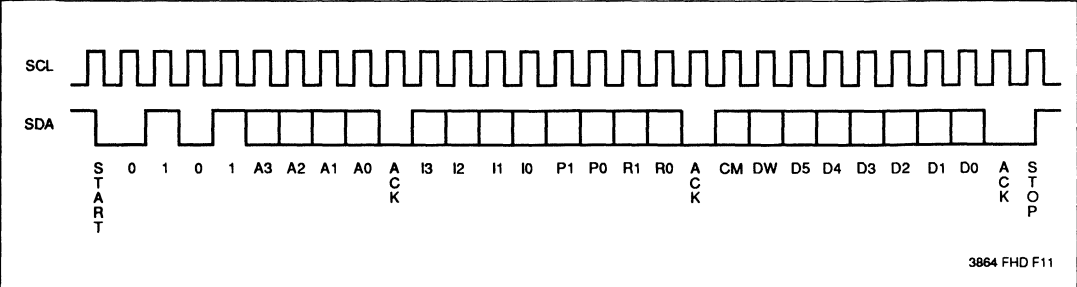
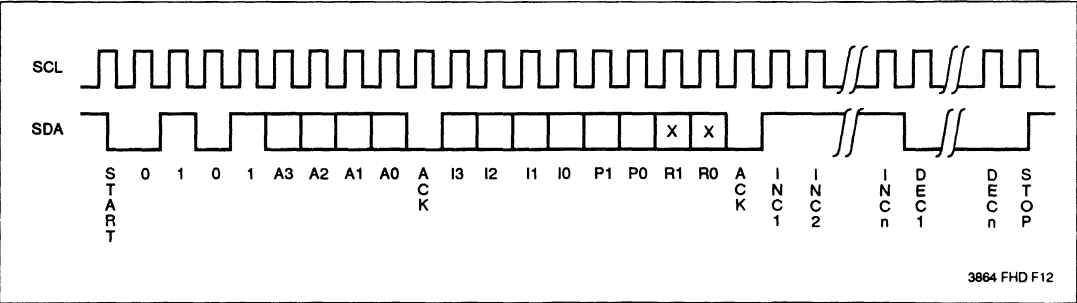


Figure 5. Increment/Decrement Command Sequence



4

Figure 6. Increment/Decrement Timing Limits

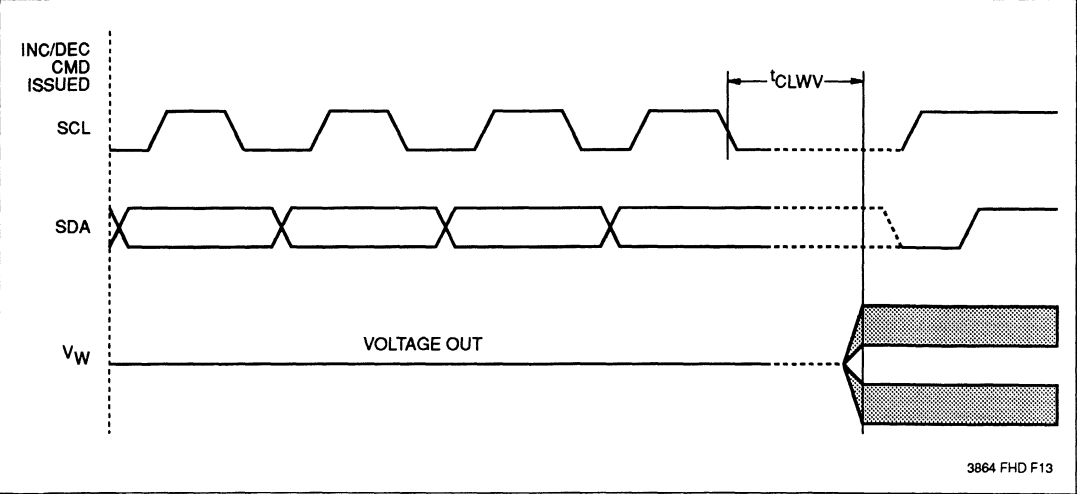


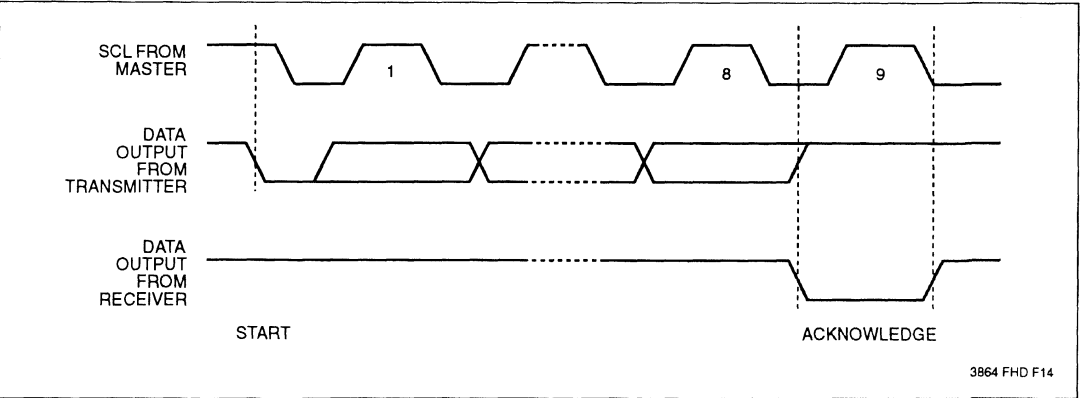
Table 1. Instruction Set

Instruction	Instruction Format								Operation
	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	P <sub>1</sub>	P <sub>0</sub>	R <sub>1</sub>	R <sub>0</sub>	
Read WCR	1	0	0	1	1/0 <sup>(7)</sup>	1/0	N/A <sup>(8)</sup>	N/A	Read the contents of the Wiper Counter Register pointed to by P <sub>1</sub> –P <sub>0</sub>
Write WCR	1	0	1	0	1/0	1/0	N/A	N/A	Write new value to the Wiper Counter Register pointed to by P <sub>1</sub> –P <sub>0</sub>
Read Data Register	1	0	1	1	1/0	1/0	1/0	1/0	Read the contents of the Register pointed to by P <sub>1</sub> –P <sub>0</sub> and R <sub>1</sub> –R <sub>0</sub>
Write Data Register	1	1	0	0	1/0	1/0	1/0	1/0	Write new value to the Register pointed to by P <sub>1</sub> –P <sub>0</sub> and R <sub>1</sub> –R <sub>0</sub>
XFR Data Register to WCR	1	1	0	1	1/0	1/0	1/0	1/0	Transfer the contents of the WCR pointed to by P <sub>1</sub> –P <sub>0</sub> and R <sub>1</sub> –R <sub>0</sub> to its associated WCR
XFR WCR to Data Register	1	1	1	0	1/0	1/0	1/0	1/0	Transfer the contents of the WCR pointed to by P <sub>1</sub> –P <sub>0</sub> to the Register pointed to by R <sub>1</sub> –R <sub>0</sub>
Global XFR Data Register to WCR	0	0	0	1	N/A	N/A	1/0	1/0	Transfer the contents of all four Data Registers pointed to by R <sub>1</sub> –R <sub>0</sub> to their respective WCR
Global XFR WCR to Data Register	1	0	0	0	N/A	N/A	1/0	1/0	Transfer the contents of all WCRs to their respective data Registers pointed to by R <sub>1</sub> –R <sub>0</sub>
Increment/Decrement Wiper	0	0	1	0	1/0	1/0	N/A	N/A	Enable Increment/decrement of the WCR pointed to by P <sub>1</sub> –P <sub>0</sub>

3864 PGM T11

Notes: (7) 1/0 = data is one or zero (typical)  
(8) N/A = Not applicable or don't care; that is, a data register is not involved in the operation and need not be addressed (typical)

Figure 7. Acknowledge Response from Receiver



3864 FHD F14

DETAILED OPERATION

All four E2POT potentiometers share the serial interface and share a common architecture. Each potentiometer is comprised of a resistor array, a wiper counter register and four data registers. A detailed discussion of the register organization and array operation follows.

Wiper Counter Register

The X9241 contains four wiper counter registers (WCR), one for each E2POT potentiometer. The WCR can be envisioned as a 6-bit parallel and serial load counter with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write WCR instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/ Decrement instruction; finally, it is loaded with the contents of its data register zero (R0) upon power-up.

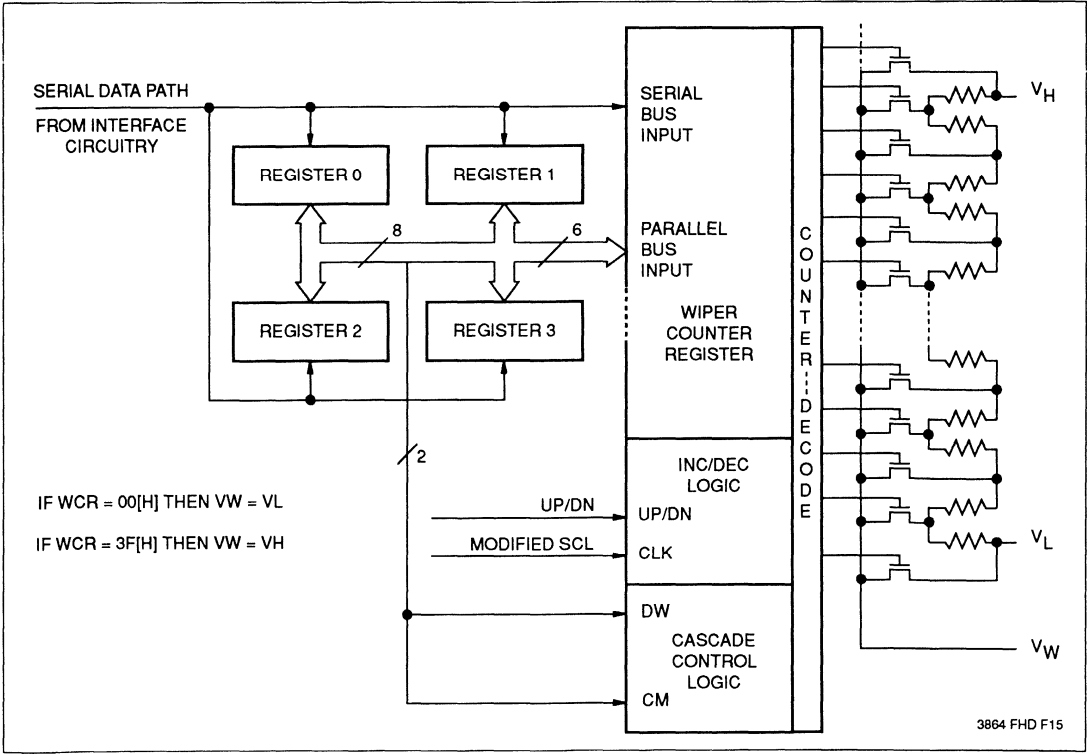
The WCR is a volatile register; that is, its contents are lost when the X9241 is powered-down. Although the register is automatically loaded with the value in R0 upon power-up, it should be noted this may be different from the value present at power-down.

Data Registers

Each potentiometer has four *nonvolatile* data registers. These can be read or written directly by the host and data can be transferred between any of the four data registers and the WCR. It should be noted all operations changing data in one of these registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, these registers can be used as regular memory locations that could possibly store system parameters or user preference data.

Figure 8. Detailed Potentiometer Block Diagram





**Cascade Mode**

The X9241 provides a mechanism for cascading the arrays. That is, the sixty-three resistor elements of one array may be cascaded (linked) with the resistor elements of an adjacent array.

**Cascade Control Bits**

The data byte, for the three-byte commands, contains 6 bits (LSBs) for defining the wiper position plus two high order bits, CM (Cascade Mode) and DW (Disable Wiper).

The state of CM enables or disables (normal operation) cascade mode. When the CM bit of the WCR is set to zero (0) the potentiometer is in the normal operation mode. When the CM bit of the WCR is set to one (1) the potentiometer is cascaded with its adjacent higher order potentiometer. For example; if bit 7 of WCR2 is set to one, pot 2 will be cascaded to pot 3.

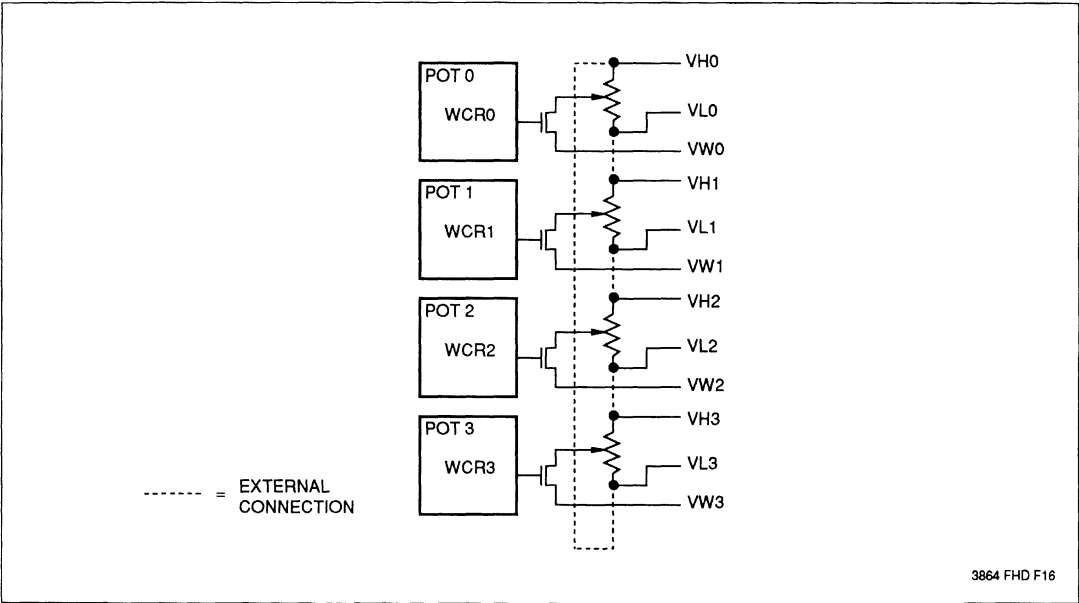
The state of DW enables or disables the wiper. When the

DW bit of the WCR is set to zero (0) the wiper is enabled; when set to one (1) the wiper is disabled. If the wiper is disabled, the wiper terminal will be electrically isolated and float.

When operating in cascade mode VH, VL and the wiper terminals of the cascaded arrays must be electrically connected externally. All but one of the wipers must be disabled. The user can alter the wiper position by writing directly to the WCR or indirectly by transferring the contents of the data registers to the WCR or by using the increment/decrement command.

When using the increment/decrement command the wiper position will automatically transition between arrays. The current position of the wiper can be determined by reading the WCR registers; if the DW bit is 0, the wiper in that array is active. If the current wiper position is to be maintained, a global XFR WCR to Data Register command must be issued before powerdown.

**Figure 9. Cascading Arrays**



X9241

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....-65°C to +135°C  
Storage Temperature .....-65°C to +150°C  
Voltage on SCK, SCL or any Address Input  
    With Respect to GND .....-1.0V to +7.0V  
Voltage on any V<sub>H</sub> or V<sub>L</sub> Referenced to GND ..... ± 8V  
 $\Delta V = [V_H - V_L]$  ..... 16V

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

3864 PGM T02

\*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Supply Voltage	Limits
X9241	5V ± 10%

3864 PGM T03

ANALOG CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Units	
	End to End Resistance	-20		+20	%	
	Power Rating			50	mW	25°C, each pot
	Wiper Current	-1		+1	mA	
	Wiper Resistance		40	100	Ω	Wiper Current = ± 1mA
V <sub>TERM</sub>	Voltage on any V <sub>H</sub> or or V <sub>L</sub> Pin	-5		+5	V	
	Noise		≤120dB		√Hz	Ref: 1V
	Resolution (4)		1.6	.4	%	
	Absolute Linearity (1)	-1		+1	MI(3)	V <sub>w(n)(actual)</sub> - V <sub>w(n)(expected)</sub>
	Relative Linearity (2)	-0.2		+0.2	MI(3)	V <sub>w(n+1)</sub> - [V <sub>w(n)</sub> + MI]
	Temperature Coefficient		±300		ppm/°C	

3864 PGM T04

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Units	
I <sub>CC</sub>	Supply Current (Active)			3	mA	f <sub>SCL</sub> = 100KHz, SDA = Open, Other Inputs = GND
I <sub>SB</sub>	V <sub>CC</sub> Current (Standby)		200	500	μA	SCL=SDA=V <sub>CC</sub> , Addr.=GND
I <sub>LI</sub>	Input Leakage Current			10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current			10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , CE = V <sub>IH</sub>
V <sub>IH</sub>	Input High Voltage	V <sub>CC</sub> x 0.7		V <sub>CC</sub> + 0.5	V	
V <sub>IL</sub>	Input Low Voltage	-1.0		V <sub>CC</sub> x 0.3	V	
V <sub>OL</sub>	Output Low Voltage			0.4	V	I <sub>OL</sub> = 3 mA

3864 PGM T05

- Notes:** (1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.  
(2) Relative Linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.  
(3) MI = RTOT/63 or (V<sub>H</sub> - V<sub>L</sub>)/63, single pot  
(4) Max. = all four arrays cascaded together, Typical = individual array resolutions.

# X9241

## ENDURANCE AND DATA RETENTION

Parameter	Min.	Units	Conditions
Minimum Endurance	100,000	Writes per Register	
Data Retention	100	Years	

3800 PGM T06

## CAPACITANCE

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}^{(5)}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0V$
$C_{IN}^{(5)}$	Input Capacitance (A0, A1, A2, A3 and SCL)	6	pF	$V_{IN} = 0V$

3800 PGM T07

## POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}^{(6)}$	Power-up to Initiation of Read Operation	1	ms
$t_{PUW}^{(6)}$	Power-up to Initiation of Write Operation	5	ms

3864 PGM T08

## A.C. CONDITIONS OF TEST

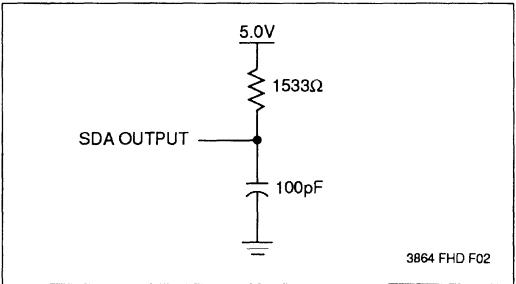
Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
Input and Output Timing Levels	$V_{CC} \times 0.5$

3864 PGM T09

**Notes:** (5) This parameter is periodically sampled and not 100% tested.

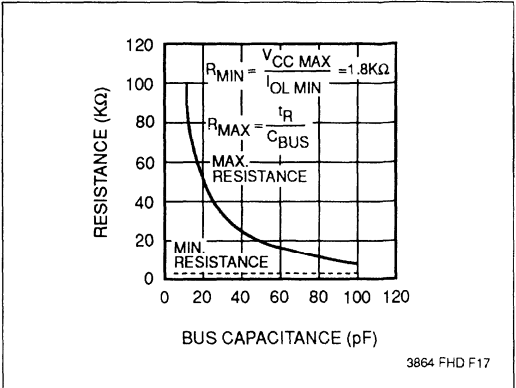
(6)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

## EQUIVALENT A.C. TEST CIRCUIT



3864 FHD F02

## Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



3864 FHD F17

A.C. CHARACTERISTICS (Over recommended operating conditions unless otherwise stated)

Symbol	Parameter	Limits		Units	Reference Figure
		Min.	Max.		
$f_{SCL}$	SCL Clock Frequency	0	100	KHz	10
$t_{LOW}$	Clock Low Period	4700		ns	10
$t_{HIGH}$	Clock High Period	4000		ns	10
$t_R$	SCL and SDA Rise Time		1000	ns	10
$t_F$	SCL and SDA Fall Time		300	ns	10
$T_i$	Noise Suppression Time Constant (Glitch Filter)		100	ns	10
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4700		ns	10 & 12
$t_{HD:STA}$	Start Condition Hold Time	4000		ns	10 & 12
$t_{SU:DAT}$	Data in Setup Time	250		ns	10
$t_{HD:DAT}$	Data in Hold Time	0		ns	10
$t_{AA}$	SCL Low to SDA Data Out Valid	300	3500	ns	11
$t_{DH}$	Data Out Hold Time	300		ns	11
$t_{SU:STO}$	Stop Condition Setup Time	4700		ns	10 & 12
$t_{BUF}$	Bus Free Time Prior to New Transmission	4700		ns	10
$t_{WR}$	Write Cycle Time (Nonvolatile Write Operation)		10	ms	13
$t_{STPWV}$	Wiper Response Time From Stop Generation		500	$\mu$ s	13
$t_{CLWV}$	Wiper Response From Clock Low		500	$\mu$ s	6

3864 PGM T10

Figure 10. Input Bus Timing

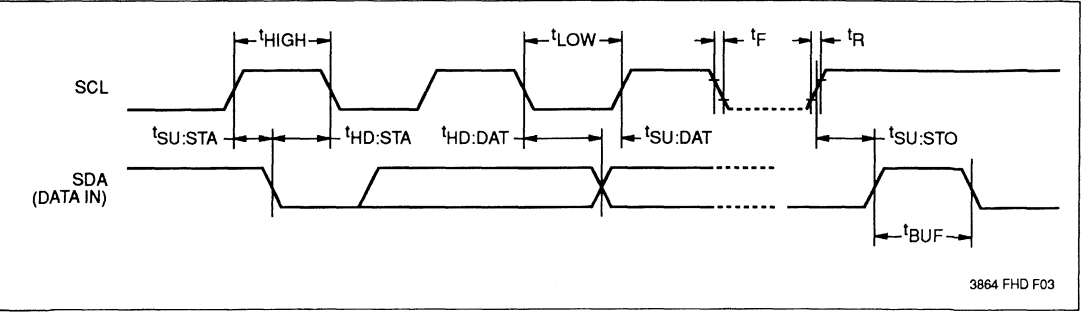


Figure 11. Output Bus Timing

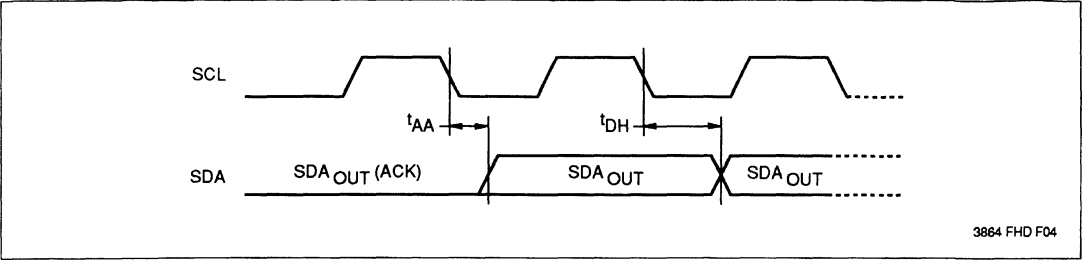


Figure 12. Start Stop Timing

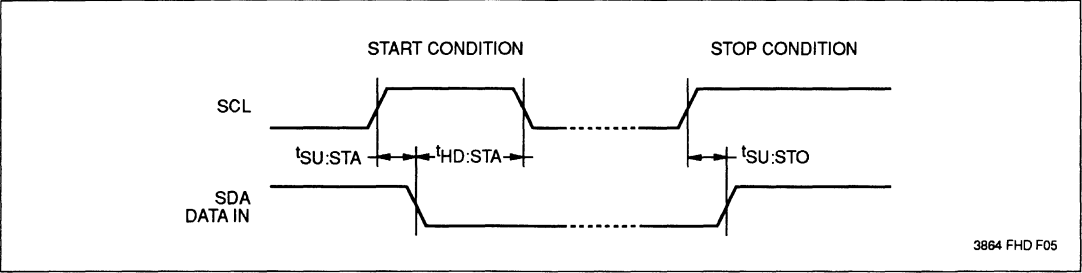
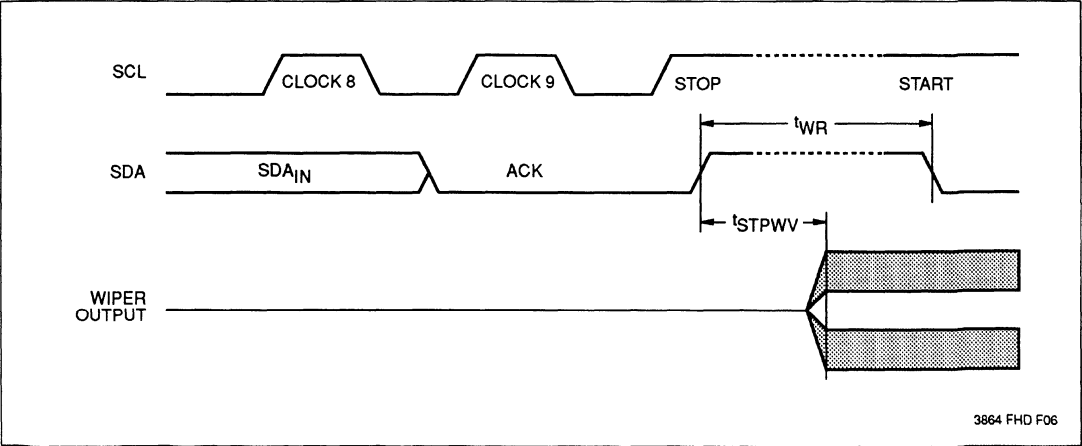


Figure 13. Write Cycle and Wiper Response Timing





<b>NOVRAM* Data Sheets</b>	<b>1</b>
<b>Serial Products Data Sheets</b>	<b>2</b>
<b>E<sup>2</sup>PROM Data Sheets</b>	<b>3</b>
<b>E<sup>2</sup>POT™ Data Sheets</b>	<b>4</b>
<b>Microcontroller Peripheral Products</b>	<b>5</b>
<b>Memory Subsystems</b>	<b>6</b>
<b>Military Products</b>	<b>7</b>
<b>Die Products</b>	<b>8</b>
<b>Application Notes and Briefs</b>	<b>9</b>
<b>Reliability</b>	<b>10</b>
<b>General Information</b>	<b>11</b>





Preliminary Information  
68XX Microcontroller Family Compatible

64K

X68C64

8192 x 8 Bit

E<sup>2</sup> Micro-Peripheral

FEATURES

- **CONCURRENT READ WRITE™**
  - Dual Plane Architecture
    - Isolates Read/Write Functions Between Planes
    - Allows Continuous Execution of Code From One Plane While Writing in the Other Plane
- **Multiplexed Address/Data Bus**
  - Direct Interface to Popular 8-bit Microcontrollers, e.g., Motorola M6801/03, M68HC11 Family
- **High Performance CMOS**
  - Fast Access Time, 120 ns
  - Low Power
    - 60 mA Maximum Active
    - 500  $\mu$ A Maximum Standby
- **Software Data Protection**
- **Block Protect Register**
  - Individually Set Write Lock Out in 1K Blocks
- **Toggle Bit**
  - Early End of Write Detection
- **Page Mode Write**
  - Allows up to 32 Bytes to be Written in One Write Cycle

DESCRIPTION

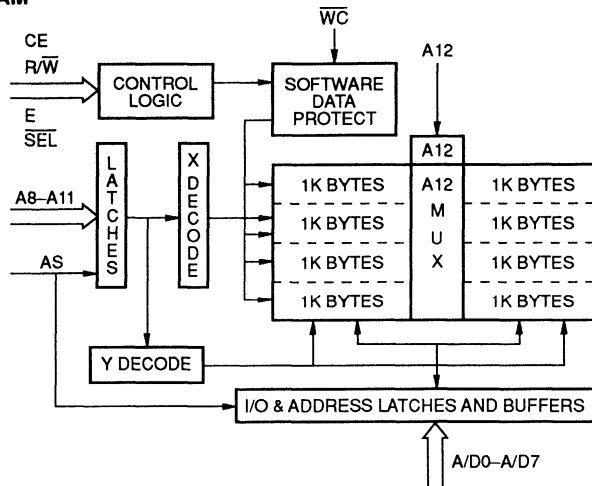
The X68C64 is an 8K x 8 E<sup>2</sup>PROM fabricated with advanced CMOS Textured Poly Floating Gate Technology. The X68C64 features a Multiplexed Address and Data bus allowing direct interface to a variety of popular single-chip microcontrollers operating in expanded multiplexed mode without the need for additional interface circuitry.

The X68C64 is internally configured as two independent 4K x 8 memory arrays. This feature provides the ability to perform nonvolatile memory updates in one array and continue operation out of code stored in the other array; effectively eliminating the need for an auxiliary memory device for code storage.

The X68C64 also provides a second generation software data protection scheme called Block Protect. Block Protect can provide write lockout of the entire device or selected 1K blocks. There are 8, 1K x 8 blocks that can be write protected individually in any combination required by the user. Block Protect, in addition to Write Control input, allows the different segments of the memory to have varying degrees of alterability in normal system operation.

5

FUNCTIONAL DIAGRAM



3868 FHD F02

CONCURRENT READ WRITE™ is a trademark of Xicor, Inc.

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# X68C64

## PIN DESCRIPTIONS

### Address/Data (A/D<sub>0</sub>–A/D<sub>7</sub>)

Multiplexed low-order addresses and data. The addresses flow into the device while AS is HIGH. After AS transitions from a HIGH to LOW the addresses are latched. Once the addresses are latched these pins input data or output data depending on E, R/W, and CE.

### Addresses (A<sub>8</sub>–A<sub>12</sub>)

High order addresses flow into the device when AS = V<sub>IH</sub> and are latched when AS goes low.

### Chip Enable (CE)

The Chip Enable input must be HIGH to enable all read/write operations. When CE is LOW and AS is LOW, the X68C64 is placed in the low power standby mode.

### Enable (E)

When used with a MC6801 or MC6803 the E input is tied directly to the E output of the microcontroller.

### Read/Write (R/W)

When used with a MC6801 or MC6803 the R/W input is tied directly to the R/W output of the microcontroller.

### Address Strobe (AS)

Addresses flow through the latches to address decoders when AS is HIGH and are latched when AS transitions from a HIGH to LOW.

### Device Select ( $\overline{\text{SEL}}$ )

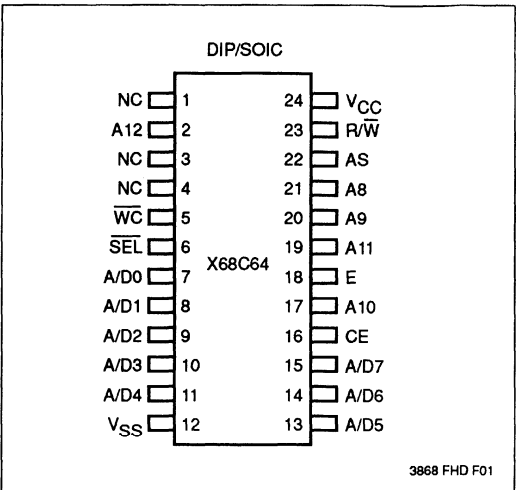
Must be connected to V<sub>SS</sub>.

### Write Control ( $\overline{\text{WC}}$ )

The Write Control allows external circuitry to abort a page load cycle once it has been initiated. This input is useful in applications in which a power failure or processor RESET could interrupt a page load cycle. In this case, the microcontroller might drive all signals HIGH, causing bad data to be latched into the E<sup>2</sup>PROM. If the Write Control input is driven HIGH (before t<sub>TBLC</sub> Max) after Read/Write (R/W) goes HIGH, the write cycle will be aborted.

When  $\overline{\text{WC}}$  is LOW (tied to V<sub>SS</sub>) the X68C64 will be enabled to perform write operations. When  $\overline{\text{WC}}$  is HIGH normal read operations may be performed, but all attempts to write to the device will be disabled.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
AS	Address Strobe
A/D <sub>0</sub> –A/D <sub>7</sub>	Address Inputs/Data I/O
A <sub>8</sub> –A <sub>12</sub>	Address Inputs
E	Enable Input
R/W	Read/Write Input
CE	Chip Enable
$\overline{\text{WC}}$	Write Control
SEL	Device Select—Connect to V <sub>SS</sub>
V <sub>SS</sub>	Ground
V <sub>CC</sub>	Supply Voltage

# X68C64

## PRINCIPLES OF OPERATION

The X68C64 is a highly integrated peripheral device for a wide variety of single-chip microcontrollers. The X68C64 provides 8K bytes of 5-volt E<sup>2</sup>PROM which can be used either for Program Storage, Data Storage or a combination of both in systems based upon Von Neumann (68XX) architectures. The X68C64 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the Address/Data bus to provide a "Seamless" interface.

The interface inputs on the X68C64 are configured such that it is possible to directly connect them to the proper interface signals of the appropriate single-chip microcontroller.

The X68C64 is internally organized as two independent planes of 4K bytes of memory with the A<sub>12</sub> input selecting which of the two planes of memory are to be accessed. While the processor is executing code out of one plane, write operations can take place in the other plane, allowing the processor to continue execution of code out of the X68C64 during a byte or page write to the device.

The X68C64 also features an advanced implementation of the Software Data Protection scheme, called Block Protect, which allows the device to be broken into 8 independent sections of 1K bytes. Each of these sections can be independently enabled for write operations; thereby allowing certain sections of the device to be secured so that updates can only occur in a controlled environment (e.g. in an automotive application, only at an authorized service center). The desired set-up configuration is stored in a nonvolatile register, ensuring the configuration data will be maintained after the device is powered down.

The X68C64 also features a Write Control input ( $\overline{WC}$ ), which serves as an external control over the completion of a previously initiated page load cycle.

The X68C64 also features the industry standard 5-volt E<sup>2</sup>PROM characteristics such a byte or page mode write and toggle-bit polling.

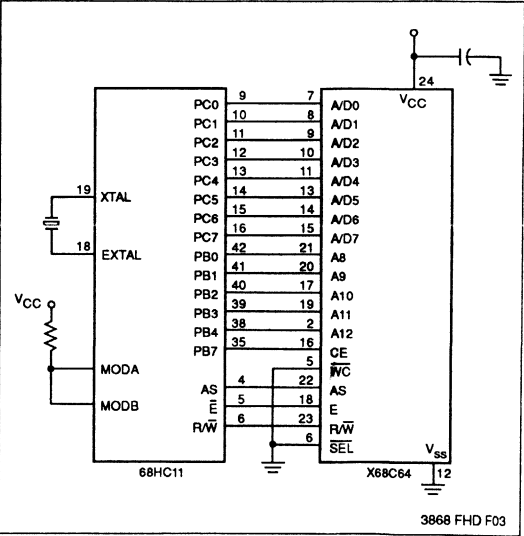
## DEVICE OPERATION

Motorola 68XX operation requires the microcontroller's AS, E and R/ $\overline{W}$  outputs tied to the X68C64 AS, E and R/ $\overline{W}$  inputs respectively.

The falling edge of AS will latch the addresses for both a read and write operation. The state of R/ $\overline{W}$  output determines the operation to be performed, with the E signal acting as a data strobe.


If R/ $\overline{W}$  is HIGH and CE HIGH (read operation) data will be output on A/D<sub>0</sub>–A/D<sub>7</sub> after E transitions HIGH. If R/ $\overline{W}$  is LOW and CE is HIGH (write operation) data presented at A/D<sub>0</sub>–A/D<sub>7</sub> will be strobed into the X68C64 on the HIGH to LOW transition of E.

## Typical Application



# X68C64

## MODE SELECTION

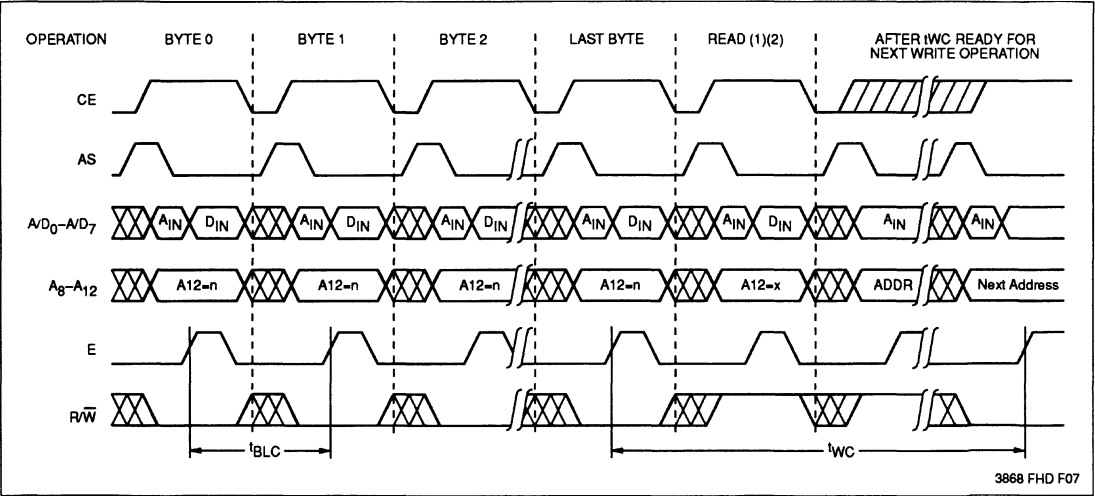
CE	E	R/ $\overline{W}$	Mode	I/O	Power
V <sub>SS</sub>	X	X	Standby	High Z	Standby (CMOS)
V <sub>IL</sub>	X	X	Standby	High Z	Standby (TTL)
V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Read	DOUT	Active
V <sub>IH</sub>		V <sub>IL</sub>	Write	DIN	Active

## PAGE WRITE OPERATION

Regardless of the microcontroller employed, the X68C64 supports page mode write operations. This allows the microcontroller to write from one to thirty-two bytes of data to the X68C64. Each individual write within a page write operation must conform to the byte write timing

requirements. The rising edge of E starts a timer delaying the internal programming cycle 100  $\mu$ s. Therefore, each successive write operation must begin within 100  $\mu$ s of the last byte written. The following waveforms illustrate the sequence and timing requirements.

### Page Write Timing Sequence for E Controlled Operation



- Notes:**
- (1) For each successive write within a page write cycle A<sub>5</sub>–A<sub>12</sub> must be the same.
  - (2) Although it is not illustrated, the microcontroller may interleave read operations between the individual byte writes within the page write operation. Two responses are possible.
    - a. Reading from the same plane being written (A<sub>12</sub> of Read = A<sub>12</sub> of Write) is effectively a Toggle Bit Polling operation.
    - b. Reading from the opposite plane being written (A<sub>12</sub> of Read  $\neq$  A<sub>12</sub> of Write) true data will be returned, facilitating the use of a single memory component as both program and data store.

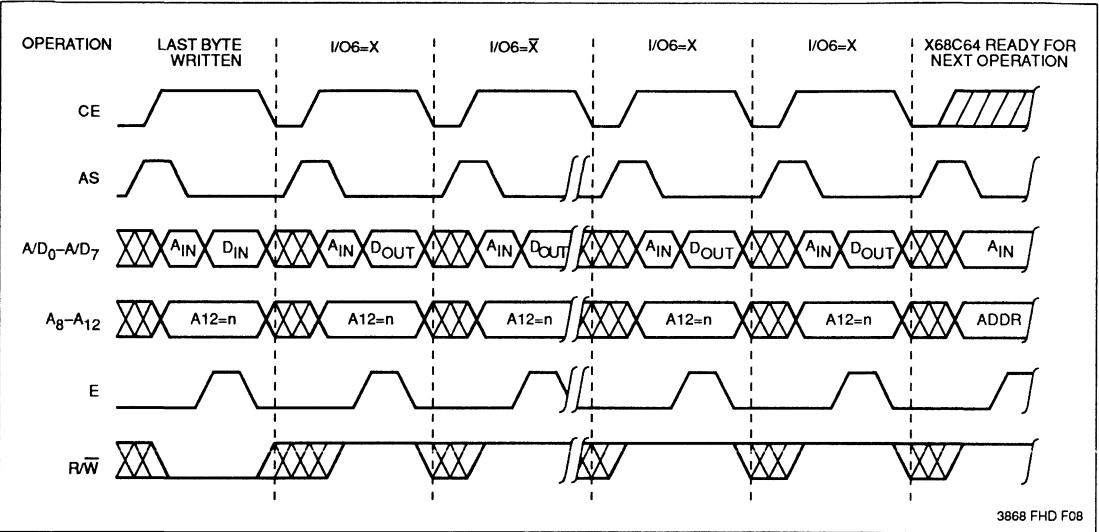
# X68C64

## Toggle Bit Polling

Because the X68C64 typical write timing is less than the specified 5 ms, Toggle Bit Polling has been provided to determine the early end of write. During the internal programming cycle I/O<sub>6</sub> will toggle from one to zero and zero to one on subsequent attempts to read the device.

When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations. Due to the dual plane architecture, reads for polling must occur in the plane that was written; that is, the state of A<sub>12</sub> during write must match the state of A<sub>12</sub> during polling.

## Toggle Bit Polling E Control

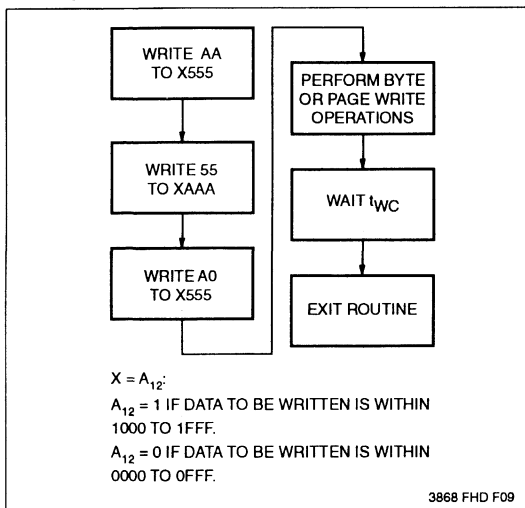


## X68C64

### DATA PROTECTION

The X68C64 provides two levels of data protection through software control. There is a global software data protection feature similar to the industry standard for E<sup>2</sup>PROMs and a new Block Protect write lock out protection providing a second level data security option.

#### Writing with SDP



#### Software Data Protection

Software data protection (SDP) is employed to protect the entire array against inadvertent writes. To write to the X68C64, a three byte command sequence must precede the byte(s) being written.

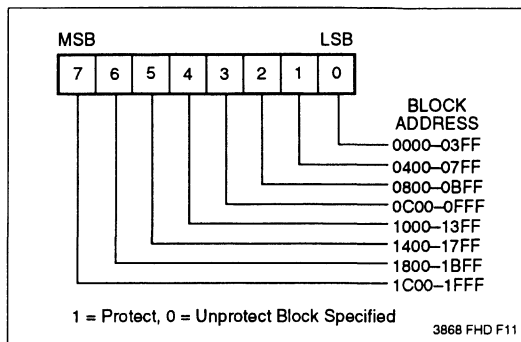
All write operations, both the command sequence and any data write operations must conform to the page write timing requirements.

#### Block Protect Write Lockout

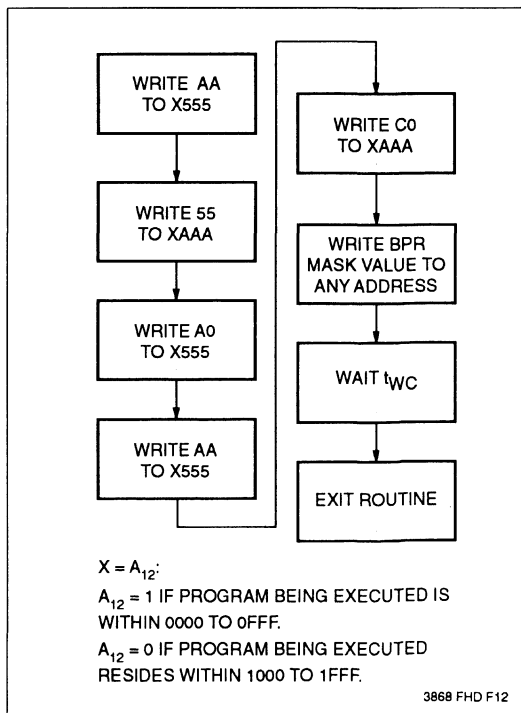
The X68C64 provides a second level of data security referred to as Block Protect write lockout. This is accessed through an extension of the SDP command sequence. Block Protect allows the user to lock out writes to 1K x 8 blocks of memory. Unlike SDP which prevents inadvertent writes, but still allows easy system access to writing the memory, Block Protect will lock out all attempts unless it is specifically disabled by the host. This could be used to set a higher level of protection in a system where a portion of the memory is used for Program Store and another portion is used as Data Store.

Setting write lockout is accomplished by writing a five byte command sequence opening access to the Block Protect Register (BPR). After the fifth byte is written the user writes to the BPR selecting which blocks to protect or unprotect. All write operations, both the command sequence and writing the data to the BPR, must conform to the page write timing requirements.

#### Block Protect Register Format



#### Setting BPR Command Sequence



X68C64

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X68C64	−10°C to +85°C
X68C64I	−65°C to +135°C
Storage Temperature	
−65°C to +150°C	
Voltage on any Pin with	
Respect to VSS	
−1.0V to +7V	
D.C. Output Current	
5 mA	
Lead Temperature	
(Soldering, 10 Seconds)	
300°C	

\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

Supply Voltage	Limits
X68C64	5V ± 10%

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Current (Active)		60	mA	CE = V <sub>IL</sub> , All I/O's = Open, Other Inputs = V <sub>CC</sub> , AS = V <sub>IH</sub>
I <sub>SB1</sub> (CMOS)	V <sub>CC</sub> Current (Standby)		500	μA	CE = V <sub>SS</sub> , All I/O's = Open, Other Inputs = V <sub>CC</sub> − 0.3V, AS = V <sub>SS</sub>
I <sub>SB2</sub> (TTL)	V <sub>CC</sub> Current (Standby)		6	mA	CE = V <sub>IH</sub> , All I/O's = Open, Other Inputs = V <sub>IH</sub> , AS = V <sub>IL</sub>
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , E = V <sub>IL</sub>
V <sub>IL</sub> (1)	Input Low Voltage	−1.0	0.8	V	
V <sub>IH</sub> (1)	Input High Voltage	2.0	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = −400 μA

CAPACITANCE T<sub>A</sub> = 25°C, F = 1.0MHZ, V<sub>CC</sub> = 5V

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (2)	Input/Output Capacitance	10	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (2)	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t <sub>PUR</sub> (2)	Power-Up to Read	1	ms
t <sub>PW</sub> (2)	Power-Up to Write	5	ms

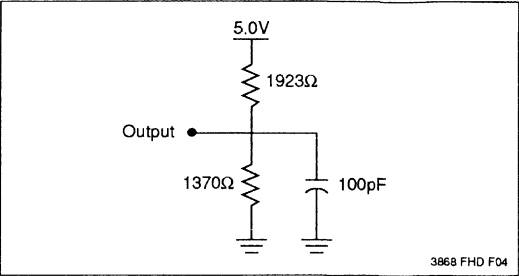
Notes: (1) V<sub>IL</sub> MIN and V<sub>IH</sub> MAX are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.

X68C64

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

TEST CIRCUIT

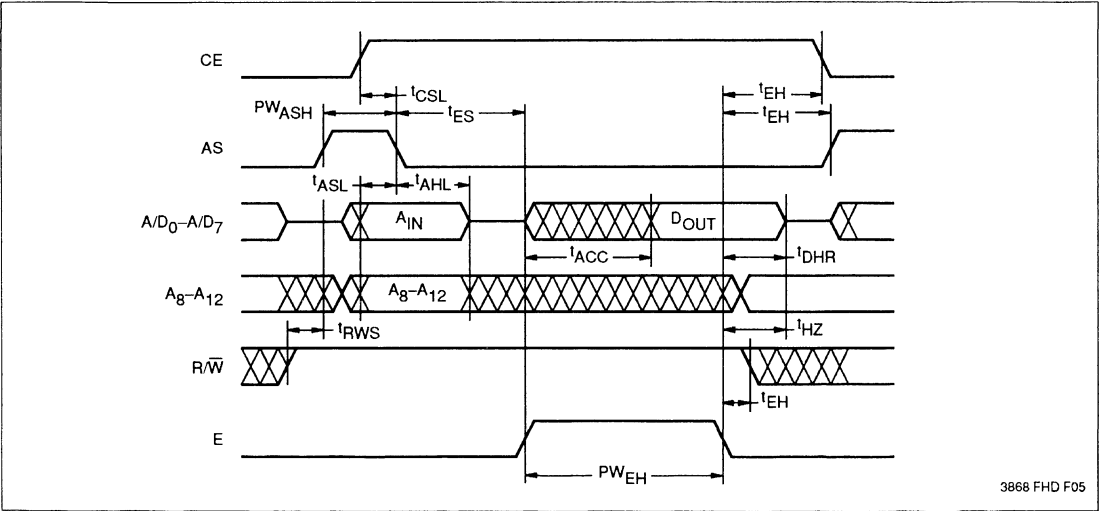


A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

E Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
PW <sub>ASH</sub>	Address Strobe Pulse Width	80		ns
t <sub>ASL</sub>	Address Setup Time	20		ns
t <sub>AHL</sub>	Address Hold Time	30		ns
t <sub>ACC</sub>	Data Access Time		120	ns
t <sub>DHR</sub>	Data Hold Time	0		ns
t <sub>CSL</sub>	CE Setup Time	7		ns
PW <sub>EH</sub>	E Pulse Width	150		ns
t <sub>ES</sub>	Enable Setup Time	30		ns
t <sub>EH</sub>	E Hold Time	20		ns
t <sub>RWS</sub>	R/W Setup Time	20		ns
t <sub>HZ</sub>	E Low to High Z Output		50	ns
t <sub>LZ</sub> <sup>(3)</sup>	E High to Low Z Output	0		ns

E Controlled Read Cycle



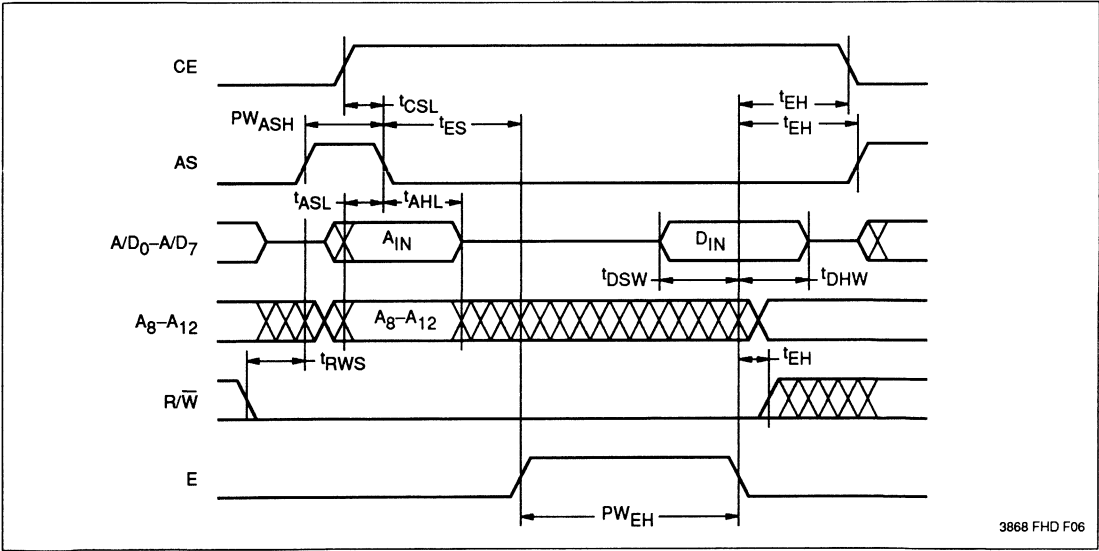
Note: (3) This parameter is periodically sampled and not 100% tested.

X68C64

E Controlled Write Cycle

Symbol	Parameter	Min.	Max.	Units
PW <sub>ASH</sub>	Address Strobe Pulse Width	80		ns
t <sub>ASL</sub>	Address Setup Time	20		ns
t <sub>AHL</sub>	Address Hold Time	30		ns
t <sub>DSW</sub>	Data Setup Time	50		ns
t <sub>DHW</sub>	Data Hold Time	30		ns
t <sub>CSL</sub>	CE Setup Time	7		ns
PW <sub>EH</sub>	E Pulse Width	120	50	ns
t <sub>WC</sub>	Write Cycle Time		5	ms
t <sub>ES</sub>	Enable Setup Time	30		ns
t <sub>RWS</sub>	R/W Setup Time	20		ns
t <sub>EH</sub>	E Hold Time	20		ns
t <sub>BLC</sub>	Byte Load Time (Page Write)	0.3	100	μs

E Controlled Write Cycle



**Note:** (4) **t<sub>WC</sub>** is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.



**X68C64**

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**NOTES**



Preliminary Information  
**Z8® Microcontroller Family Compatible**

**64K**

**X86C64**

**8192 x 8 Bit**

**E<sup>2</sup> Micro-Peripheral**

**FEATURES**

- **CONCURRENT READ WRITE™**
  - Dual Plane Architecture
  - Isolates Read/Write Functions Between Planes
  - Allows Continuous Execution of Code From One Plane While Writing in the Other Plane
- **Multiplexed Address/Data Bus**
  - Direct Interface to Popular 8-bit Microcontrollers, e.g. Zilog Z8 Family
- **High Performance CMOS**
  - Fast Access Time, 120 ns
  - Low Power
  - 60 mA Maximum Active
  - 200  $\mu$ A Maximum Standby
- **Software Data Protection**
- **Block Protect Register**
  - Individually Set Write Lock Out in 1K Blocks
- **Toggle Bit**
  - Early End of Write Detection
- **Page Mode Write**
  - Allows up to 32 Bytes to be Written in One Write Cycle

**DESCRIPTION**

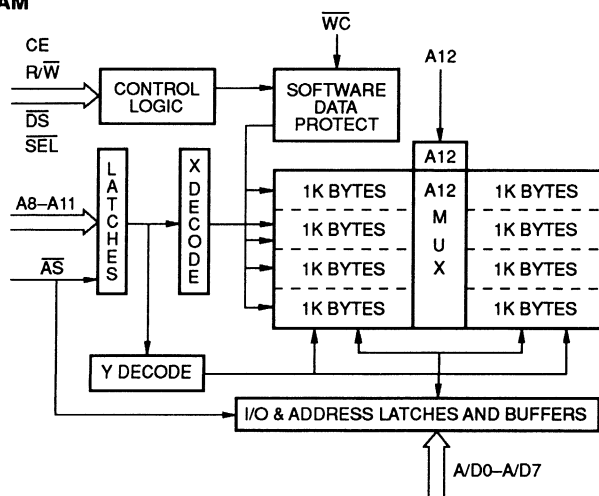
The X86C64 is an 8K x 8 E<sup>2</sup>PROM fabricated with advanced CMOS Textured Poly Floating Gate Technology. The X86C64 features a Multiplexed Address and Data bus allowing direct interface to a variety of popular single-chip microcontrollers operating in expanded multiplexed mode without the need for additional interface circuitry.

The X86C64 is internally configured as two independent 4K x 8 memory arrays. This feature provides the ability to perform nonvolatile memory updates in one array and continue operation out of code stored in the other array; effectively eliminating the need for an auxiliary memory device for code storage.

The X86C64 also provides a second generation software data protection scheme called Block Protect. Block Protect can provide write lockout of the entire device or selected 1K blocks. There are 8, 1K x 8 blocks that can be write protected individually in any combination required by the user. Block Protect, in addition to Write Control input, allows the different segments of the memory to have varying degrees of alterability in normal system operation.

5

**FUNCTIONAL DIAGRAM**



3819 FHD F02

Z8® is a registered trademark of Zilog Corporation  
CONCURRENT READ WRITE™ is a trademark of Xicor, Inc.

© Xicor, 1991 Patents Pending

# X86C64

## PIN DESCRIPTIONS

### Address/Data (A/D<sub>0</sub>–A/D<sub>7</sub>)

Multiplexed low-order addresses and data. The addresses flow into the device while  $\overline{AS}$  is LOW. After  $\overline{AS}$  transitions from a LOW to HIGH the addresses are latched. Once the addresses are latched these pins input data or output data depending on  $\overline{DS}$ , R/W, and CE.

### Addresses (A<sub>8</sub>–A<sub>12</sub>)

High order addresses flow into the device when  $\overline{AS} = V_{IL}$  and are latched when  $\overline{AS}$  goes HIGH.

### Chip Enable (CE)

The Chip Enable input must be HIGH to enable all read/write operations. When CE is LOW and  $\overline{AS}$  is HIGH, the X86C64 is placed in the low power standby mode.

### Data Strobe ( $\overline{DS}$ )

When used with a Z8 the  $\overline{DS}$  input is tied directly to the DS output of the microcontroller.

### Read/Write (R/W)

When used with a Z8 the R/W input is tied directly to the R/W output of the microcontroller.

### Address Strobe ( $\overline{AS}$ )

Addresses flow through the latches to address decoders when  $\overline{AS}$  is LOW and are latched when  $\overline{AS}$  transitions from a LOW to HIGH.

### Device Select ( $\overline{SEL}$ )

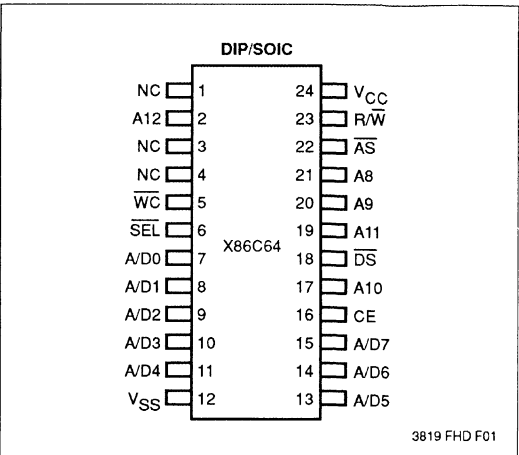
Must be connected to  $V_{SS}$ .

### Write Control ( $\overline{WC}$ )

The Write Control allows external circuitry to abort a page load cycle once it has been initiated. This input is useful in applications in which a power failure or processor RESET could interrupt a page load cycle. In this case, the microcontroller might drive all signals HIGH, causing bad data to be latched into the E<sup>2</sup>PROM. If the Write Control input is driven HIGH (before  $t_{BLC}$  Max) after Read/Write (R/W) goes HIGH, the write cycle will be aborted.

When  $\overline{WC}$  is LOW (tied to  $V_{SS}$ ) the X86C64 will be enabled to perform write operations. When  $\overline{WC}$  is HIGH normal read operations may be performed, but all attempts to write to the device will be disabled.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
$\overline{AS}$	Address Strobe
A/D <sub>0</sub> –A/D <sub>7</sub>	Address Inputs/Data I/O
A <sub>8</sub> –A <sub>12</sub>	Address Inputs
$\overline{DS}$	Data Strobe Input
R/W	Read/Write Input
CE	Chip Enable
$\overline{WC}$	Write Control
$\overline{SEL}$	Device Select—Connect to $V_{SS}$
$V_{SS}$	Ground
$V_{CC}$	Supply Voltage

3819 PGM T01

# X86C64

## PRINCIPLES OF OPERATION

The X86C64 is a highly integrated peripheral device for a wide variety of single-chip microcontrollers. The X86C64 provides 8K bytes of 5-volt E<sup>2</sup>PROM which can be used either for Program Storage, Data Storage or a combination of both in systems based upon Von Neumann (86XX) architectures. The X86C64 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the Address/Data bus to provide a "Seamless" interface.

The interface inputs on the X86C64 are configured such that it is possible to directly connect them to the proper interface signals of the appropriate single-chip microcontroller.

The X86C64 is internally organized as two independent planes of 4K bytes of memory with the A<sub>12</sub> input selecting which of the two planes of memory are to be accessed. While the processor is executing code out of one plane, write operations can take place in the other plane, allowing the processor to continue execution of code out of the X86C64 during a byte or page write to the device.

The X86C64 also features an advanced implementation of the Software Data Protection scheme, called Block Protect, which allows the device to be broken into 8 independent sections of 1K bytes. Each of these sections can be independently enabled for write operations; thereby allowing certain sections of the device to be secured so that updates can only occur in a controlled environment (e.g. in an automotive application, only at an authorized service center). The desired set-up configuration is stored in a nonvolatile register, ensuring the configuration data will be maintained after the device is powered down.

The X86C64 also features a Write Control input ( $\overline{WC}$ ), which serves as an external control over the completion of a previously initiated page load cycle.

The X86C64 also features the industry standard 5-volt E<sup>2</sup>PROM characteristics such as a byte or page mode write and toggle-bit polling.

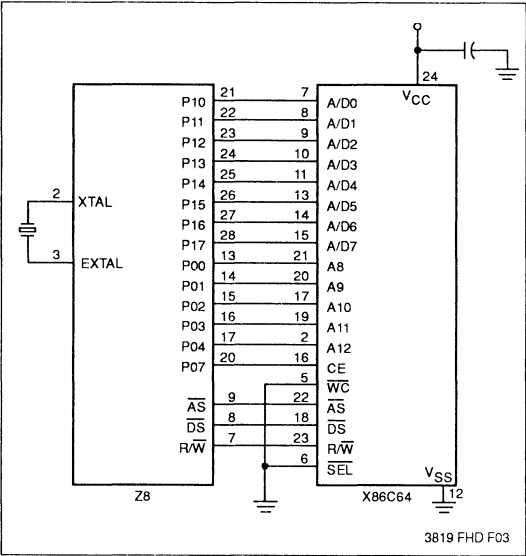
## DEVICE OPERATION

Zilog Z8 operation requires the microcontroller's  $\overline{AS}$ ,  $\overline{DS}$  and R/ $\overline{W}$  outputs tied to the X86C64  $\overline{AS}$ ,  $\overline{DS}$  and R/ $\overline{W}$  inputs respectively.

The rising edge of  $\overline{AS}$  will latch the addresses for both a read and write operation. The state of R/ $\overline{W}$  output determines the operation to be performed, with the  $\overline{DS}$  signal acting as a data strobe.


If R/ $\overline{W}$  is HIGH and CE HIGH (read operation) data will be output on A/D<sub>0</sub>–A/D<sub>7</sub> after  $\overline{DS}$  transitions LOW. If R/ $\overline{W}$  is LOW and CE is HIGH (write operation) data presented at A/D<sub>0</sub>–A/D<sub>7</sub> will be strobed into the X86C64 on the LOW to HIGH transition of  $\overline{DS}$ .

## Typical Application



# X86C64

## MODE SELECTION

CE	$\overline{DS}$	R/ $\overline{W}$	Mode	I/O	Power
V <sub>SS</sub>	X	X	Standby	High Z	Standby (CMOS)
V <sub>IL</sub>	X	X	Standby	High Z	Standby (TTL)
V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Read	D <sub>OUT</sub>	Active
V <sub>IH</sub>		V <sub>IL</sub>	Write	D <sub>IN</sub>	Active

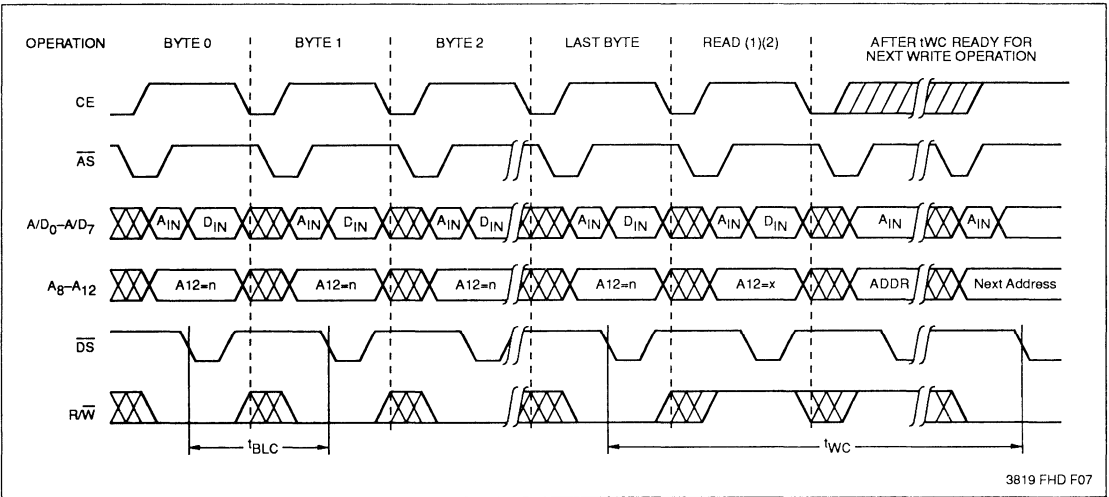
3819 PGM T08

## PAGE WRITE OPERATION

Regardless of the microcontroller employed, the X86C64 supports page mode write operations. This allows the microcontroller to write from one to thirty-two bytes of data to the X86C64. Each individual write within a page write operation must conform to the byte write timing

requirements. The falling edge of  $\overline{DS}$  starts a timer delaying the internal programming cycle 100  $\mu$ s. Therefore, each successive write operation must begin within 100  $\mu$ s of the last byte written. The following waveforms illustrate the sequence and timing requirements.

### Page Write Timing Sequence for $\overline{DS}$ Controlled Operation



3819 FHD F07

- Notes:**
- (1) For each successive write within a page write cycle A<sub>5</sub>-A<sub>12</sub> must be the same.
  - (2) Although it is not illustrated, the microcontroller may interleave read operations between the individual byte writes within the page write operation. Two responses are possible.
    - a. Reading from the same plane being written (A<sub>12</sub> of Read = A<sub>12</sub> of Write) is effectively a Toggle Bit Polling operation.
    - b. Reading from the opposite plane being written (A<sub>12</sub> of Read  $\neq$  A<sub>12</sub> of Write) true data will be returned, facilitating the use of a single memory component as both program and data store.

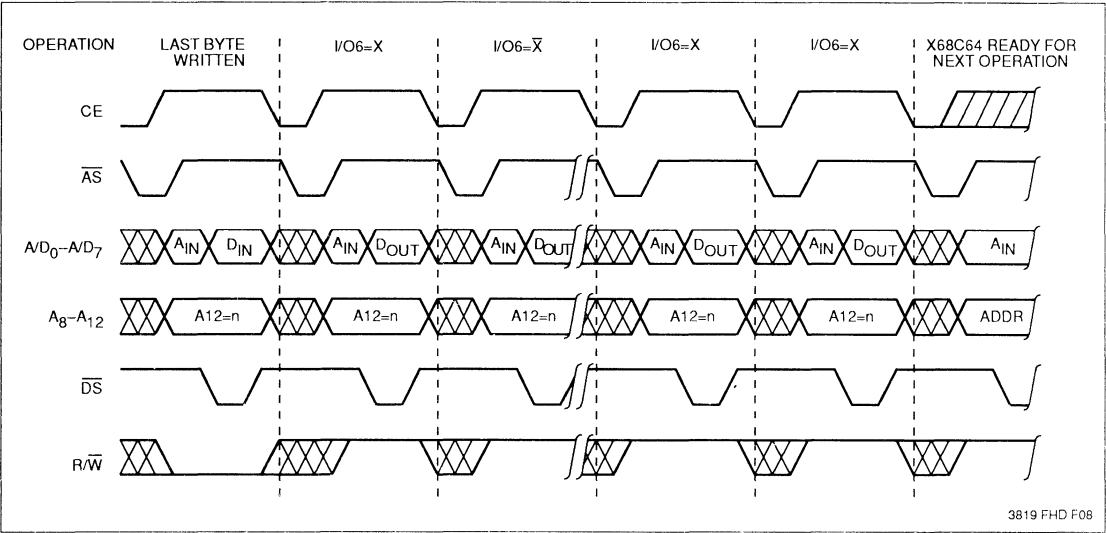
# X86C64

## Toggle Bit Polling

Because the X86C64 typical write timing is less than the specified 5 ms, Toggle Bit Polling has been provided to determine the early end of write. During the internal programming cycle I/O<sub>6</sub> will toggle from one to zero and zero to one on subsequent attempts to read the device.

When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations. Due to the dual plane architecture, reads for polling must occur in the plane that was written; that is, the state of A<sub>12</sub> during write must match the state of A<sub>12</sub> during polling.

## Toggle Bit Polling $\overline{DS}$ Control

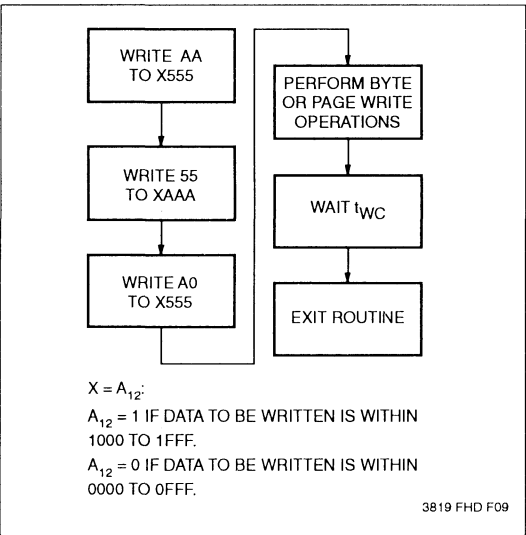


# X86C64

## DATA PROTECTION

The X86C64 provides two levels of data protection through software control. There is a global software data protection feature similar to the industry standard for E2PROMs and a new Block Protect write lock out protection providing a second level data security option.

### Writing with SDP



### Software Data Protection

Software data protection (SDP) is employed to protect the entire array against inadvertent writes. To write to the X86C64, a three byte command sequence must precede the byte(s) being written.

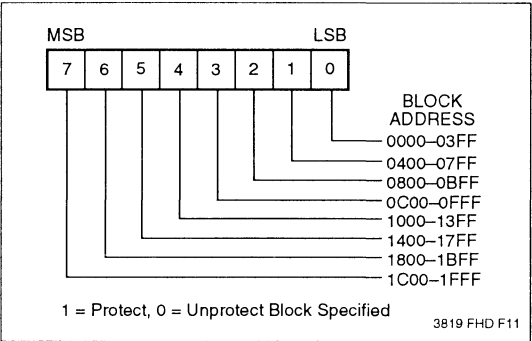
All write operations, both the command sequence and any data write operations must conform to the page write timing requirements.

### Block Protect Write Lockout

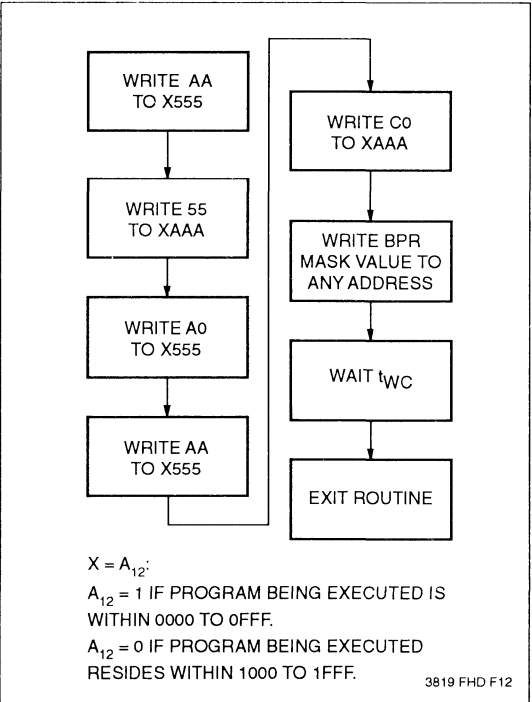
The X86C64 provides a second level of data security referred to as Block Protect write lockout. This is accessed through an extension of the SDP command sequence. Block Protect allows the user to lock out writes to 1K x 8 blocks of memory. Unlike SDP which prevents inadvertent writes, but still allows easy system access to writing the memory, Block Protect will lock out all attempts unless it is specifically disabled by the host. This could be used to set a higher level of protection in a system where a portion of the memory is used for Program Store and another portion is used as Data Store.

Setting write lockout is accomplished by writing a five byte command sequence opening access to the Block Protect Register (BPR). After the fifth byte is written the user writes to the BPR selecting which blocks to protect or unprotect. All write operations, both the command sequence and writing the data to the BPR, must conform to the page write timing requirements.

### Block Protect Register Format



### Setting BPR Command Sequence



X86C64

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X86C64	−10°C to +85°C
X86C64I	−65°C to +135°C
Storage Temperature	
Voltage on any Pin with	
Respect to VSS	−1.0V to +7V
D.C. Output Current	
Lead Temperature	
(Soldering, 10 Seconds)	300°C

\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	−40°C	+85°C
Military	−55°C	+125°C

Supply Voltage	Limits
X86C64	5V ± 10%

3819 PGM T03

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Current (Active)		60	mA	CE = V <sub>IL</sub> , All I/O's = Open, Other Inputs = V <sub>CC</sub> , AS = V <sub>IL</sub>
ISB1(CMOS)	V <sub>CC</sub> Current (Standby)		500	μA	CE = V <sub>SS</sub> , All I/O's = Open, Other Inputs = V <sub>CC</sub> − 0.3V
ISB2(TTL)	V <sub>CC</sub> Current (Standby)		6	mA	CE = V <sub>IH</sub> , All I/O's = Open, Other Inputs = V <sub>IH</sub>
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , DS = V <sub>IH</sub>
V <sub>IL</sub> (1)	Input Low Voltage	−1.0	0.8	V	
V <sub>IH</sub> (1)	Input High Voltage	2.0	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = −400 μA

3819 PGM T04

CAPACITANCE T<sub>A</sub> = 25°C, F = 1.0MHZ, V<sub>CC</sub> = 5V

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (2)	Input/Output Capacitance	10	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (2)	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

3819 PGM T05

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t <sub>PUR</sub> (2)	Power-Up to Read	1	ms
t <sub>PUW</sub> (2)	Power-Up to Write	5	ms

3819 PGM T06

Notes: (1) V<sub>IL</sub> MIN and V<sub>IH</sub> MAX are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.



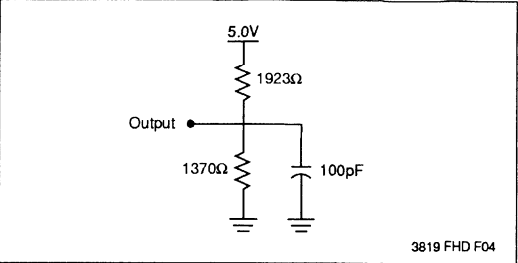
X86C64

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3819 PGM T07

EQUIVALENT A.C. TEST CIRCUIT



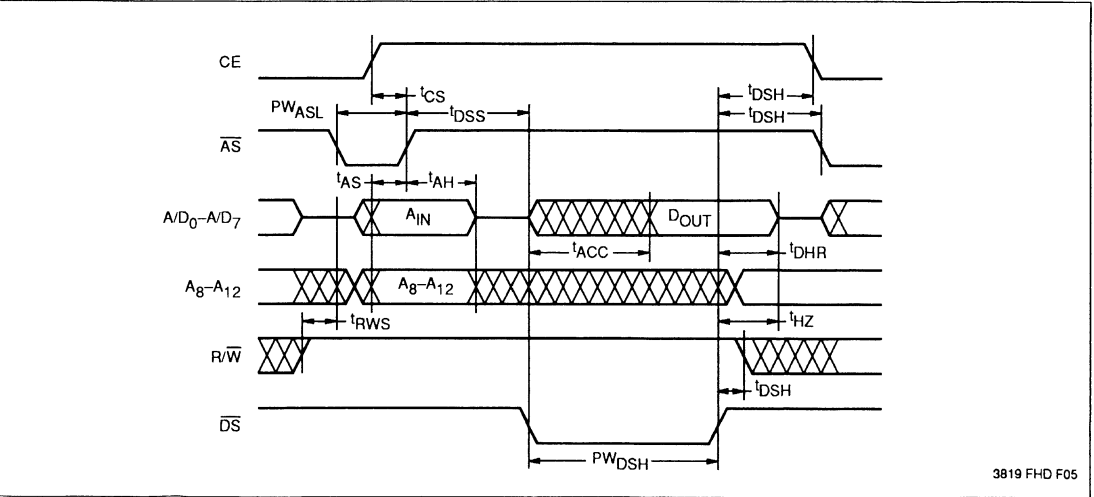
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

$\overline{DS}$  Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
PW <sub>ASL</sub>	Address Strobe Pulse Width	80		ns
t <sub>AS</sub>	Address Setup Time	20		ns
t <sub>AH</sub>	Address Hold Time	30		ns
t <sub>ACC</sub>	Data Access Time		120	ns
t <sub>DHR</sub>	Data Hold Time	0		ns
t <sub>CS</sub>	CE Setup Time	7		ns
PW <sub>DSH</sub>	$\overline{DS}$ Pulse Width	150		ns
t <sub>DSS</sub>	$\overline{DS}$ Setup Time	30		ns
t <sub>DSH</sub>	$\overline{DS}$ Hold Time	20		ns
t <sub>RWS</sub>	R/W Setup Time	20		ns
t <sub>HZ</sub>	$\overline{DS}$ High to High Z Output		50	ns
t <sub>LZ</sub> <sup>(3)</sup>	$\overline{DS}$ Low to Low Z Output	0		ns

3819 PGM T09

$\overline{DS}$  Controlled Read Cycle



**Note:** (3) This parameter is periodically sampled and not 100% tested.

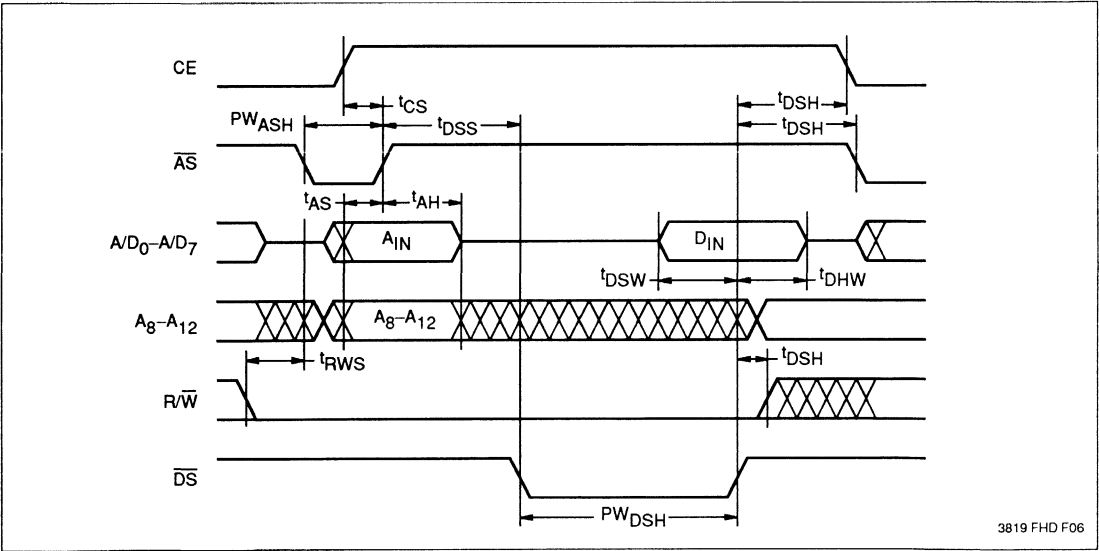
X86C64

$\overline{\text{DS}}$  Controlled Write Cycle

Symbol	Parameter	Min.	Max.	Units
PW <sub>ASH</sub>	Address Strobe Pulse Width	80		ns
t <sub>AS</sub>	Address Setup Time	20		ns
t <sub>AH</sub>	Address Hold Time	30		ns
t <sub>DSW</sub>	Data Setup Time	50		ns
t <sub>DHW</sub>	Data Hold Time	30		ns
t <sub>CS</sub>	CE Setup Time	7		ns
PW <sub>DSH</sub>	$\overline{\text{DS}}$ Pulse Width	120	50	ns
t <sub>WC</sub>	Write Cycle Time		5	ms
t <sub>DSS</sub>	Enable Setup Time	30		ns
t <sub>RWS</sub>	R/W Setup Time	20		ns
t <sub>DSH</sub>	$\overline{\text{DS}}$ Hold Time	20		ns
t <sub>BLC</sub>	Byte Load Time (Page Write)	0.3	100	$\mu\text{s}$

3819 PGM T10

$\overline{\text{DS}}$  Controlled Write Cycle



**Note:** (4)  $t_{WC}$  is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

**X86C64**

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**NOTES**



Preliminary Information  
8051 Microcontroller Family Compatible

64K

X88C64

8192 x 8 Bit

E<sup>2</sup> Micro-Peripheral

FEATURES

- **CONCURRENT READ WRITE™**
  - Dual Plane Architecture
  - Isolates Read/Write Functions Between Planes
  - Allows Continuous Execution of Code From One Plane While Writing in the Other Plane
- **Multiplexed Address/Data Bus**
  - Direct Interface to Popular 8051 Family
- **High Performance CMOS**
  - Fast Access Time, 120 ns
  - Low Power
    - 60 mA Active Maximum
    - 500  $\mu$ A Standby Maximum
- **Software Data Protection**
- **Block Protect Register**
  - Individually Set Write Lock Out in 1K Blocks
- **Toggle Bit**
  - Early End of Write Detection
- **Page Mode Write**
  - Allows up to 32 Bytes to be Written in One Write Cycle

DESCRIPTION

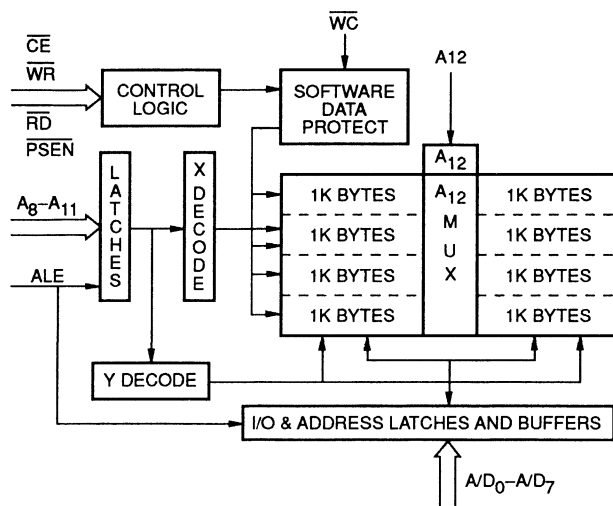
The X88C64 is an 8K x 8 E<sup>2</sup>PROM fabricated with advanced CMOS Textured Poly Floating Gate Technology. The X88C64 features a Multiplexed Address and Data bus allowing direct interface to a variety of popular single-chip microcontrollers operating in expanded multiplexed mode without the need for additional interface circuitry.

The X88C64 is internally configured as two independent 4K x 8 memory arrays. This feature provides the ability to perform nonvolatile memory updates in one array and continue operation out of code stored in the other array; effectively eliminating the need for an auxiliary memory device for code storage.

The X88C64 also provides a second generation software data protection scheme called Block Protect. Block Protect can provide write lockout of the entire device or selected 1K blocks. There are 8 1K x 8 blocks that can be write protected individually in any combination required by the user. Block Protect, in addition to Write Control input, allows the different segments of the memory to have varying degrees of alterability in normal system operation.

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FUNCTIONAL DIAGRAM



3867 FHD F02

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# X88C64

## PIN DESCRIPTIONS

### Address/Data (A/D<sub>0</sub>–A/D<sub>7</sub>)

Multiplexed low-order addresses and data. The Addresses flow into the device while ALE is HIGH. After ALE transitions from a HIGH to LOW the addresses are latched. Once the addresses are latched these pins input data or output data depending on  $\overline{RD}$ ,  $\overline{WR}$ ,  $\overline{PSEN}$  and  $\overline{CE}$ .

### Addresses (A<sub>8</sub>–A<sub>12</sub>)

High order addresses flow into the device when ALE =  $V_{IH}$  and are latched when ALE goes low.

### Chip Enable ( $\overline{CE}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH and ALE is LOW, the X88C64 is placed in the low power standby mode.

### Program Store Enable ( $\overline{PSEN}$ )

When the X88C64 is to be used in a 8051 based system,  $\overline{PSEN}$  is tied directly to the microcontroller's  $\overline{PSEN}$  output.

### Read ( $\overline{RD}$ )

When the X88C64 is to be used in a 8051 based system,  $\overline{RD}$  is tied directly to the microcontroller's  $\overline{RD}$  output.

### Write ( $\overline{WR}$ )

When the X88C64 is to be used in a 8051 based system,  $\overline{WR}$  is tied directly to the microcontroller's  $\overline{WR}$  output.

### Address Latch Enable (ALE)

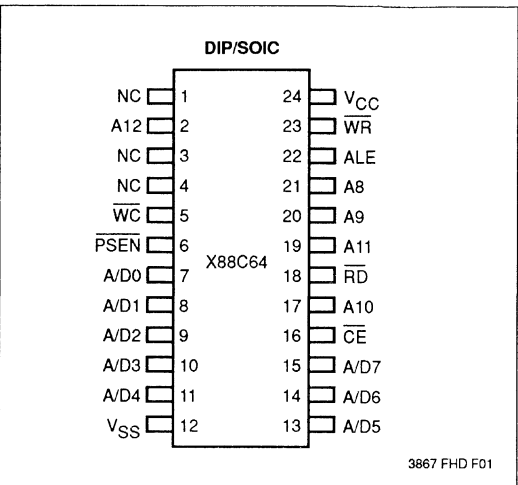
Addresses flow through the latches to address decoders when ALE is HIGH and are latched when ALE transitions from a HIGH to LOW.

### Write Control ( $\overline{WC}$ )

The Write Control allows external circuitry to abort a page load cycle once it has been initiated. This input is useful in applications in which a power failure or processor RESET could interrupt a page load cycle. In this case, the microcontroller might drive all signals HIGH, causing bad data to be latched into the E<sup>2</sup>PROM. If the Write Control input is driven HIGH (before  $t_{BLC\ Max}$ ) after Write ( $\overline{WR}$ ) goes HIGH, the write cycle will be aborted.

When  $\overline{WC}$  is LOW (tied to  $V_{SS}$ ) the X88C64 will be enabled to perform write operations. When  $\overline{WC}$  is HIGH normal read operations may be performed, but all attempts to write to the device will be disabled.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
ALE	Address Latch Enable
A/D <sub>0</sub> –A/D <sub>7</sub>	Address Inputs/Data I/O
A <sub>8</sub> –A <sub>12</sub>	Address Inputs
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
$\overline{PSEN}$	Program Store Enable Input
$\overline{CE}$	Chip Enable
$\overline{WC}$	Write Control
V <sub>SS</sub>	Ground
V <sub>CC</sub>	Supply Voltage

3867 PGM T01

X88C64

PRINCIPLES OF OPERATION

The X88C64 is a highly integrated peripheral device for a wide variety of single-chip microcontrollers. The X88C64 provides 8K bytes of 5-volt E<sup>2</sup>PROM which can be used either for Program Storage, Data Storage or a combination of both in systems based upon Harvard (80XX) architectures. The X88C64 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the Address/Data bus to provide a "Seamless" interface.

The interface inputs on the X88C64 are configured such that it is possible to directly connect them to the proper interface signals of the appropriate single-chip microcontroller. In the Harvard type system, the reading of data from the chip is controlled either by the  $\overline{\text{PSEN}}$  or the  $\overline{\text{RD}}$  signal, which essentially maps the X88C64 into both the Program and the Data Memory address map.

The X88C64 is internally organized as two independent planes of 4K bytes of memory with the A<sub>12</sub> input selecting which of the two planes of memory are to be accessed. While the processor is executing code out of one plane, write operations can take place in the other plane, allowing the processor to continue execution of code out of the X88C64 during a byte or page write to the device.

The X88C64 also features an advanced implementation of the Software Data Protection scheme, called Block Protect, which allows the device to be broken into 8 independent sections of 1K bytes. Each of these sections can be independently enabled for write operations; thereby allowing certain sections of the device to be secured so that updates can only occur in a controlled environment (e.g. in an automotive application, only at an authorized service center). The desired set-up configuration is stored in a nonvolatile register, ensuring the configuration data will be maintained after the device is powered down.

The X88C64 also features a Write Control input ( $\overline{\text{WC}}$ ), which serves as an external control over the completion of a previously initiated page load cycle.

The X88C64 also features the industry standard 5-volt E<sup>2</sup>PROM characteristics such as byte or page mode write and toggle-bit polling.

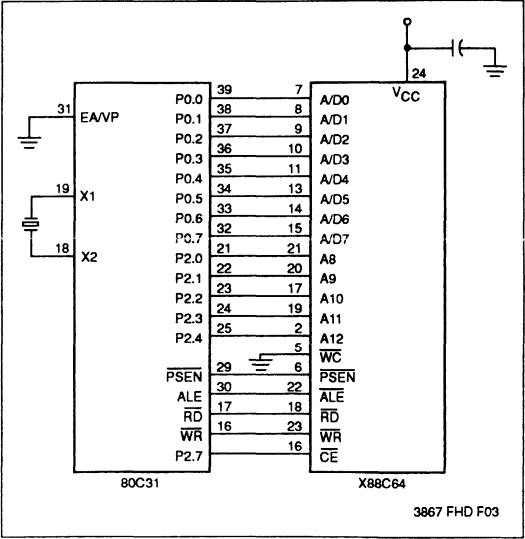
DEVICE OPERATION

Modes  
Mixed Program/Data Memory

By properly assigning the address spaces, a single X88C64 can be used as both the Program and Data Memory. This would be accomplished by connecting all the 8051 control outputs to the corresponding inputs of the X88C64.

In this configuration, one plane of memory could be dedicated to Program Store and the other plane dedicated to Data Store. The Data Store can be fully protected by enabling block protect write lock out.

TYPICAL APPLICATION



Program Memory Mode

This mode of operation is read only. The  $\overline{\text{PSEN}}$  and  $\overline{\text{ALE}}$  inputs of the X88C64 are tied directly to the  $\overline{\text{PSEN}}$  and  $\overline{\text{ALE}}$  outputs of the X88C64 are tied directly to the  $\overline{\text{PSEN}}$  and  $\overline{\text{ALE}}$  outputs of the microcontroller. The  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  inputs are tied HIGH.

When  $\overline{\text{ALE}}$  is HIGH, the A/D<sub>0</sub>–A/D<sub>7</sub> and A<sub>8</sub>–A<sub>12</sub> addresses flow into the device. The addresses, both low and high order, are latched when  $\overline{\text{ALE}}$  transitions LOW ( $V_{IL}$ ).  $\overline{\text{PSEN}}$  will then go LOW and after  $t_{PLDV}$ , valid data is presented on the A/D<sub>0</sub>–A/D<sub>7</sub> pins.  $\overline{\text{CE}}$  must be LOW during the entire operation.

# X88C64

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## DATA MEMORY MODE

This mode of operation allows both read and write functions. The  $\overline{\text{PSEN}}$  input is tied to  $V_{\text{IH}}$  or to  $V_{\text{CC}}$  through a pullup resistor. The  $\text{ALE}$ ,  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  inputs are tied directly to the microcontroller's  $\text{ALE}$ ,  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  outputs.

### Read


This operation is quite similar to the Program Memory read. A HIGH to LOW transition on  $\text{ALE}$  latches the

addresses and the data will be output on the AD pins after  $\overline{\text{RD}}$  goes LOW ( $t_{\text{RLDV}}$ ).

### Write

A write is performed by latching the addresses on the falling edge of  $\text{ALE}$ . Then  $\overline{\text{WR}}$  is strobed low followed by valid data being presented at the  $\text{A/D}_0\text{--A/D}_7$  pins. The data will be latched into the X88C64 on the rising edge of  $\overline{\text{WR}}$ .

## MODE SELECTION

$\overline{\text{CE}}$	$\overline{\text{PSEN}}$	$\overline{\text{RD}}$	$\overline{\text{WR}}$	Mode	I/O	Power
$V_{\text{CC}}$	X	X	X	Standby	High Z	Standby (CMOS)
$V_{\text{IH}}$	X	X	X	Standby	High Z	Standby (TTL)
$V_{\text{IL}}$	$V_{\text{IL}}$	$V_{\text{IH}}$	$V_{\text{IH}}$	Read	DOUT	Active
$V_{\text{IL}}$	$V_{\text{IH}}$	$V_{\text{IL}}$	$V_{\text{IH}}$	Read	DOUT	Active
$V_{\text{IL}}$	$V_{\text{IH}}$	$V_{\text{IH}}$		Write	DIN	Active

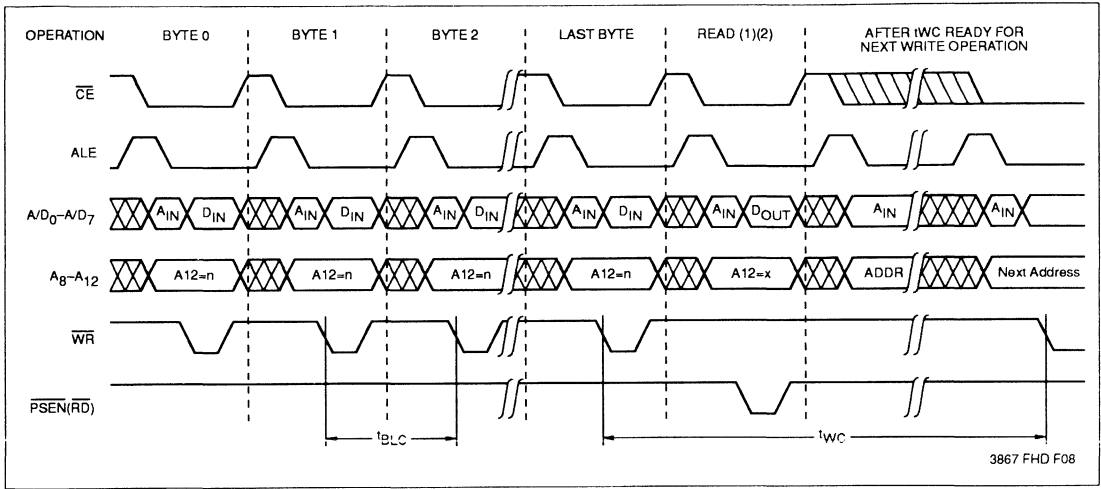
# X88C64

## PAGE WRITE OPERATION

Regardless of the microcontroller employed, the X88C64 supports page mode write operations. This allows the microcontroller to write from one to thirty-two bytes of data to the X88C64. Each individual write within a page

write operation must conform to the byte write timing requirements. The falling edge of WR starts a timer delaying the internal programming cycle 100  $\mu$ s. Therefore, each successive write operation must begin within 100  $\mu$ s of the last byte written. The following waveforms illustrate the sequence and timing requirements.

Page Write Timing Sequence for  $\overline{\text{WR}}$  Controlled Operation



- Notes:**
- (1) For each successive write within a page write cycle  $\text{A}_5\text{--}\text{A}_{12}$  must be the same.
  - (2) Although it is not illustrated, the microcontroller may interleave read operations between the individual byte writes within the page write operation. Two responses are possible:
    - a. Reading from the same plane being written ( $\text{A}_{12}$  of Read =  $\text{A}_{12}$  of Write) is effectively a Toggle Bit Polling operation.
    - b. Reading from the opposite plane being written ( $\text{A}_{12}$  of Read  $\neq$   $\text{A}_{12}$  of Write) true data will be returned, facilitating the use of a single memory component as both program and data store.



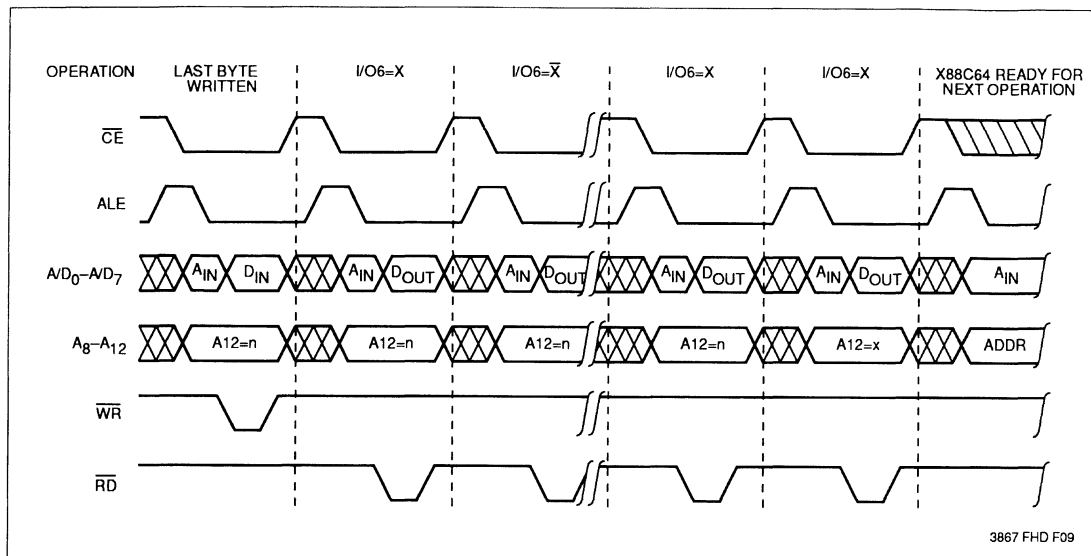
## X88C64

### TOGGLE BIT POLLING

Because the X88C64 typical write timing is less than the specified 5 ms, Toggle Bit Polling has been provided to determine the early end of write. During the internal programming cycle  $I/O_6$  will toggle from one to zero and zero to one on subsequent attempts to read the device.

When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations. Due to the dual plane architecture, reads for polling must occur in the plane that was written; that is, the state of  $A_{12}$  during write must match the state of  $A_{12}$  during polling.

### Toggle Bit Polling $\overline{RD}/\overline{WR}$ Control



# X88C64

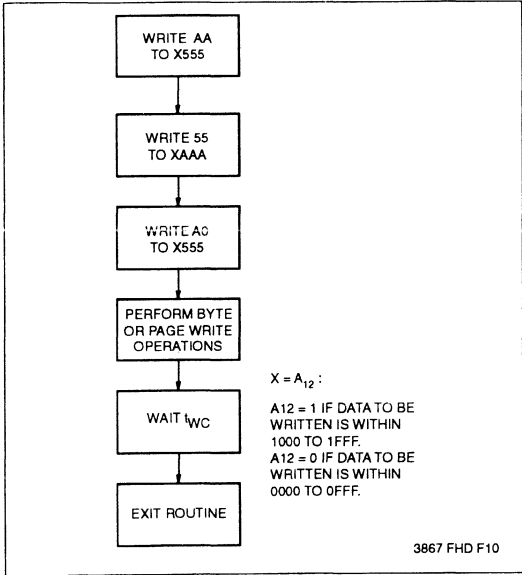
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## SOFTWARE DATA PROTECTION

Software data protection (SDP) is employed to protect the entire array against inadvertent writes. To write to the X88C64, a three byte command sequence must precede the byte(s) being written. All write operations, both the command sequence and any data write operations must conform to the page write timing requirements.

### Writing with SDP

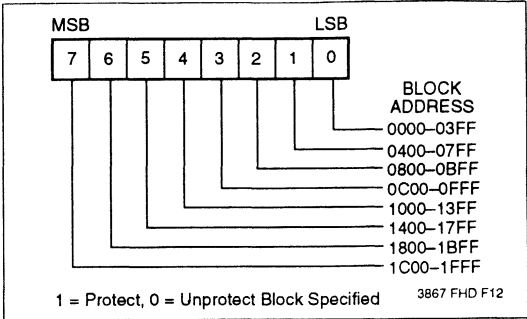


### Block Protect Write Lockout

The X88C64 provides a second level of data security referred to as Block Protect write lockout. This is accessed through an extension of the SDP command sequence. Block Protect allows the user to lock out writes to 1K x 8 blocks of memory. Unlike SDP which prevents inadvertent writes, but still allows easy system access to writing the memory, Block Protect will lock out all attempts unless it is specifically disabled by the host. This could be used to set a higher level of protection in a system where a portion of the memory is used for Program Store and another portion is used as Data Store.

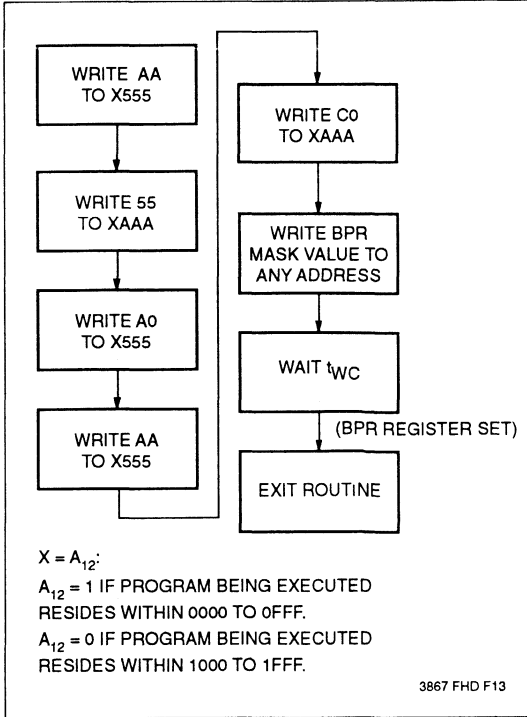
Setting write lockout is accomplished by writing a five byte command sequence opening access to the Block Protect Register (BPR). After the fifth byte is written the user writes to the BPR selecting which blocks to protect or unprotect. All write operations, both the command sequence and writing the data to the BPR, must conform to the page write timing requirements.

### Block Protect Register Format



5

### Setting BPR Sequence



## X88C64

### ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X88C64	–10°C to +85°C
X88C64I	–65°C to +135°C
Storage Temperature	–65°C to +150°C
Voltage on any Pin with Respect to $V_{SS}$	–1.0V to +7V
D.C. Output Current	5 mA
Lead Temperature (Soldering, 10 Seconds)	300°C

### \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3867 PGM T02

Supply Voltage	Limits
X88C64	5V ± 10%

3867 PGM T03

### D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
$I_{CC}$	$V_{CC}$ Current (Active)		60	mA	$\overline{CE} = \overline{RD} = V_{IL}$ , All I/O's = Open, Other Inputs = $V_{CC}$
$I_{SB1}(CMOS)$	$V_{CC}$ Current (Standby)		500	$\mu A$	$\overline{CE} = V_{CC} - 0.3V$ , All I/O's = Open, Other Inputs = $V_{CC} - 0.3V$ , $ALE = V_{IL}$
$I_{SB2}(TTL)$	$V_{CC}$ Current (Standby)		6	mA	$\overline{CE} = V_{IH}$ , All I/O's = Open, Other Inputs = $V_{IH}$ , $ALE = V_{IL}$
$I_{LI}$	Input Leakage Current		10	$\mu A$	$V_{IN} = GND$ to $V_{CC}$
$I_{LO}$	Output Leakage Current		10	$\mu A$	$V_{OUT} = GND$ to $V_{CC}$ , $RD = V_{IH} = PSEN$
$V_{IL}(3)$	Input Low Voltage	–1.0	0.8	V	
$V_{IH}(3)$	Input High Voltage	2.0	$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage		0.4	V	$I_{OL} = 2.1$ mA
$V_{OH}$	Output High Voltage	2.4		V	$I_{OH} = -400$ $\mu A$

3867 PGM T04

### CAPACITANCE $T_A = 25^\circ C$ , $F = 1.0$ MHZ, $V_{CC} = 5V$

Symbol	Test	Max.	Units	Conditions
$C_{I/O}(4)$	Input/Output Capacitance	10	pF	$V_{I/O} = 0V$
$C_{IN}(4)$	Input Capacitance	6	pF	$V_{IN} = 0V$

3867 PGM T05

### POWER-UP TIMING

Symbol	Parameter	Max.	Units
$t_{PUR}(4)$	Power-Up to Read	1	ms
$t_{PUW}(4)$	Power-Up to Write	5	ms

3867 PGM T06

Notes: (3)  $V_{IL}$  MIN and  $V_{IH}$  MAX are for reference only and are not tested.

(4) This parameter is periodically sampled and not 100% tested.

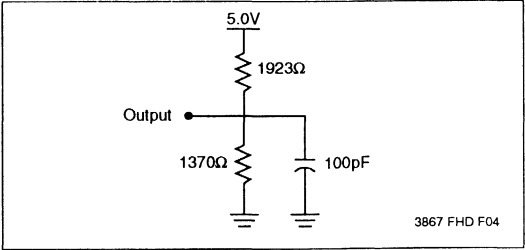
X88C64

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3867 PGM T07

EQUIVALENT A.C. TEST CIRCUIT



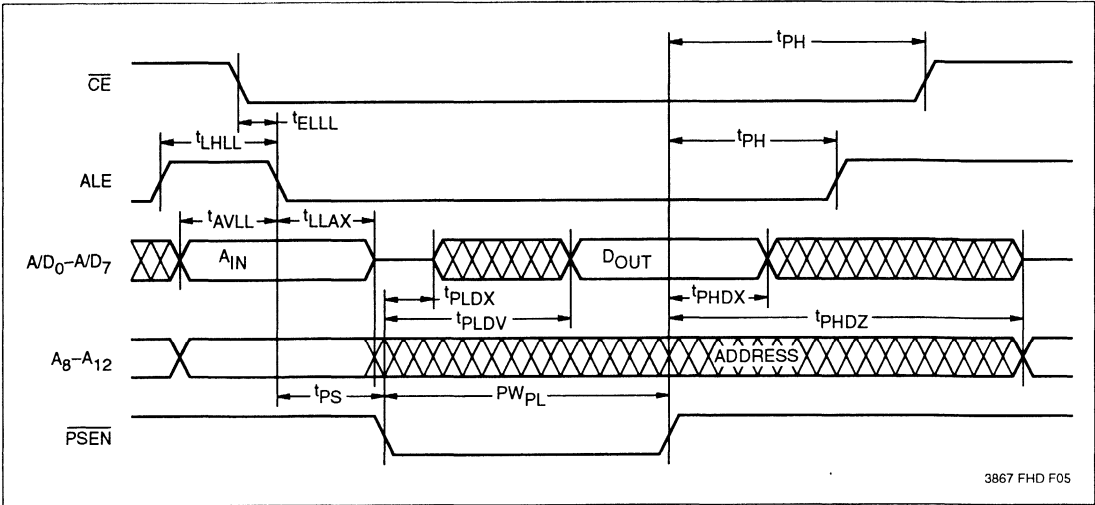
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

PSEN Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
tLHLL	ALE Pulse Width	80		ns
tAVLL	Address Setup Time	20		ns
tLLAX	Address Hold Time	30		ns
tPLDV	PSEN Read Access Time		120	ns
tPHDX	Data Hold Time	0		ns
tELLL	Chip Enable Setup Time	7		ns
PWPL	PSEN Pulse Width	150		ns
tPS	PSEN Setup Time	30		ns
tPH	PSEN Hold Time	20		ns
tPHDZ	PSEN Disable to Output in High Z		50	ns
tPLDX (5)	PSEN to Output in Low Z	10		ns

3867 PGM T09

PSEN Controlled Read Timing Diagram



Note: (5) This parameter is periodically sampled and not 100% tested.

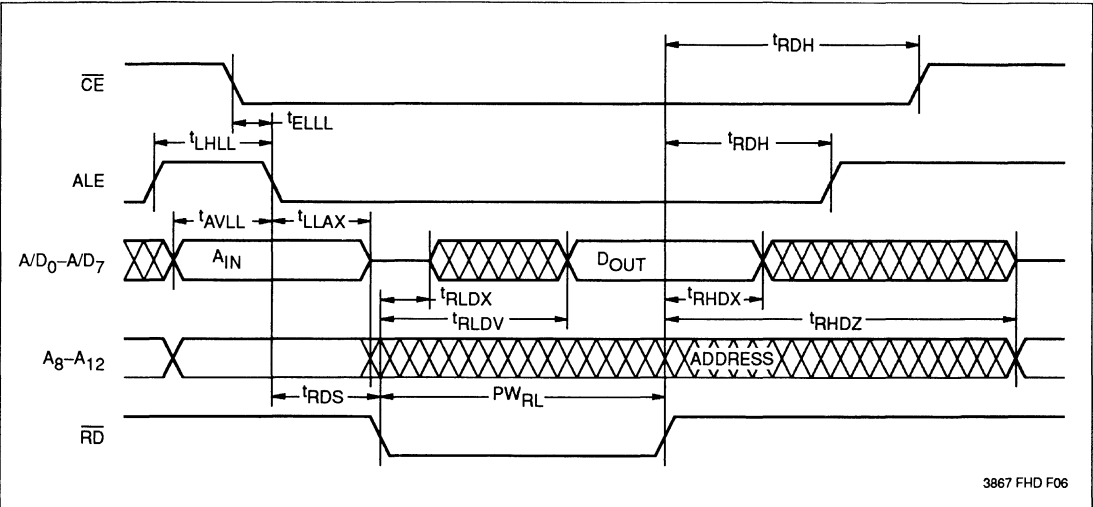
# X88C64

## $\overline{RD}$ Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
$t_{LHLL}$	ALE Pulse Width	80		ns
$t_{AVLL}$	Address Setup Time	20		ns
$t_{LLAX}$	Address Hold Time	30		ns
$t_{RLDV}$	RD Read Access Time		120	ns
$t_{RHDX}$	Data Hold Time	0		ns
$t_{ELLL}$	Chip Enable Setup Time	7		ns
$PW_{RL}$	RD Pulse Width	150		ns
$t_{RDS}$	RD Setup Time	30		ns
$t_{RDH}$	RD Hold Time	20		ns
$t_{RHDZ}$	RD Disable to Output in High Z		50	ns
$t_{RLDX}^{(6)}$	RD to Output in Low Z	0		ns

3867 PGM T10

## $\overline{RD}$ Controlled Read Timing Diagram



3867 FHD F06

**Note:** (6) This parameter is periodically sampled and not 100% tested.

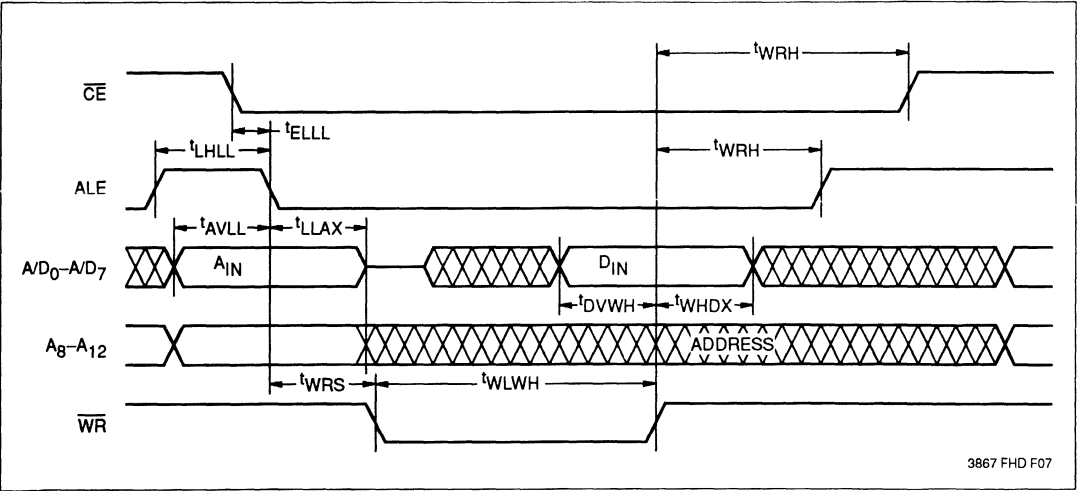
# X88C64

## WR Controlled Write Cycle

Symbol	Parameter	Min.	Max.	Units
$t_{LHLL}$	ALE Pulse Width	80		ns
$t_{AVLL}$	Address Setup Time	20		ns
$t_{LLAX}$	Address Hold Time	30		ns
$t_{DVWH}$	Data Setup Time	50		ns
$t_{WHDX}$	Data Hold Time	30		ns
$t_{ELLL}$	Chip Enable Setup Time	7		ns
$t_{WLWH}$	WR Pulse Width	120		ns
$t_{WRS}$	WR Setup Time	30		ns
$t_{WRH}$	WR Hold Time	20		ns
$t_{BLC}$	Byte Load Time (Page Write)	.3	100	$\mu$ s
$t_{WC}^{(7)}$	Write Cycle Time		5	ms

3867 PGM T11

## WR Controlled Write Timing Diagram



**Note:** (7)  $t_{WC}$  is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

**X88C64**

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**NOTES**

**Fact Sheet**  
**68XX Microcontroller Family Compatible**



**8K**

**X68C75**

**8192 x 8 Bit**

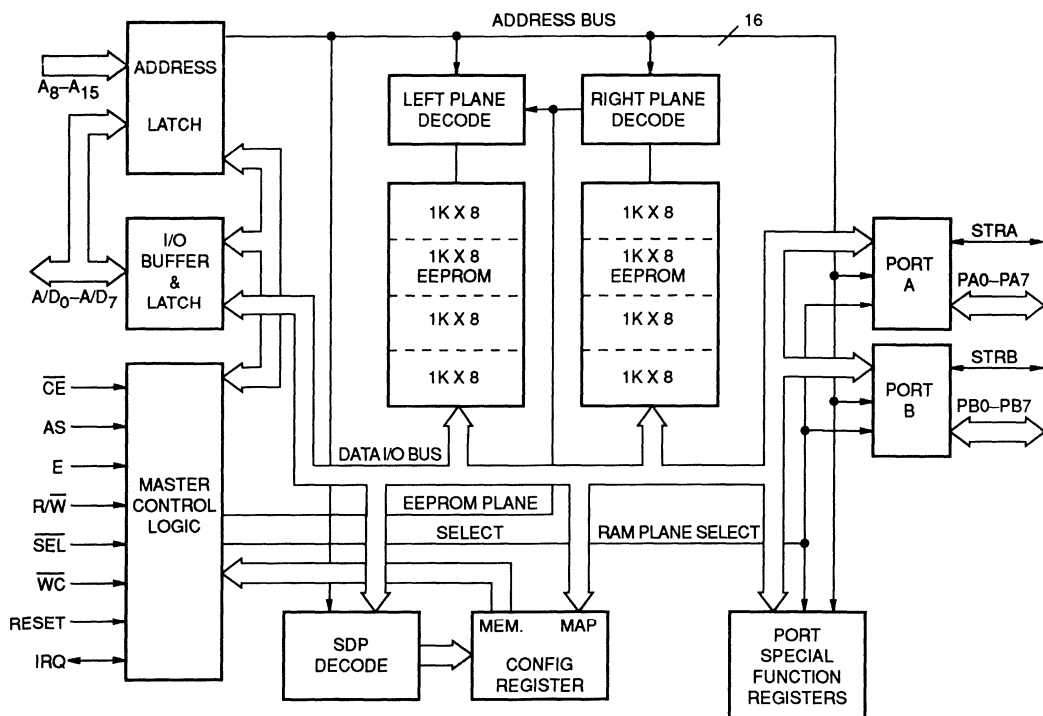
**Nonvolatile Program/Data Memory and I/O Port Expander**

**FEATURES**

- **Highly Integrated Microcontroller Peripheral**
  - 8K Bytes of 5-Volt Byte-Alterable Nonvolatile Memory
  - Nonvolatile Memory May Be Used for Program Storage, Data Storage or Both
  - Two General Purpose 8-Bit Bidirectional I/O Ports
  - Internal Programmable Address Decoding
- **CONCURRENT READ WRITE™**
  - Dual Plane Architecture
  - Isolates Read/Write Functions Between Planes
  - Allows Continuous Execution of Code from One Plane While Writing in the Other Plane
- **Multiplexed Address/Data Bus**
  - Direct Interface to Popular Microcontrollers
  - 68HC11 Family
- **High Performance CMOS**
  - Fast Access Time, 120 ns
  - Low Power
    - 40 mA Active
    - 100 uA Standby
- **Software Data Protection**
  - Protect Entire Array During Power-up/-down
- **Block Protect Register**
  - Set Write Lock Out in 1K Blocks
- **Toggle BIT**

**FUNCTIONAL DIAGRAM**

**5**



3828 FHD F01

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# X68C75

## DESCRIPTION

The X68C75 is a highly integrated peripheral for the 68HC11 family of microcontrollers. The device integrates 8K Bytes of 5-Volt byte-alterable nonvolatile memory, two Bidirectional 8-Bit Ports, programmable internal address decoding and a multiplexed Address and Data Bus.

The 5-Volt byte-alterable nonvolatile memory can be used as program storage, data storage or a combination of both. The memory array is separated into two 4K byte sections which allows read accesses to one-half while a write operation is taking place in the other half. The nonvolatile memory also features Software Data Protection to protect the contents during power transitions, and an advanced Block Protect Register which allows individual blocks of the memory to be configured as Read only or Read/Write.

Each bidirectional port consists of eight General Purpose I/O lines and one data strobe line. The ports also feature a configurable Interrupt Request output.

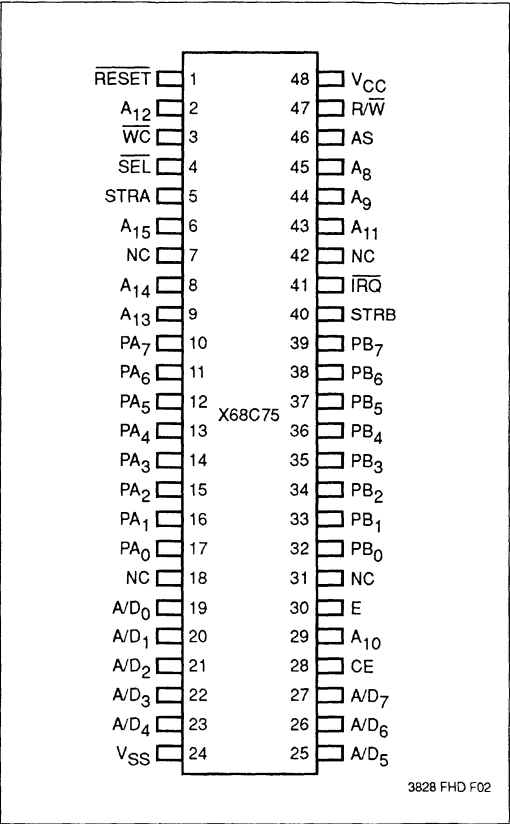
Access to the X68C75 is accomplished through the multiplexed Address/Data bus of the type controller. An internal programmable address decoder maps the internal memory and register locations into the desired address space.

## PIN NAMES

Symbol	Description
AS	Address Strobe
A/D <sub>0</sub> –A/D <sub>7</sub>	Address Inputs/Data I/O
A <sub>8</sub> –A <sub>15</sub>	Address Inputs
E	Enable Input
R/W	Read/Write Input
SEL	Device Select—Connect to V <sub>ss</sub>
WC	Write Control
CE	Chip Enable
PA <sub>0</sub> –PA <sub>7</sub>	Ports A I/O Lines
PB <sub>0</sub> –PB <sub>7</sub>	Port B I/O Lines
STRA;STRB	Port A and B Strobes
IRQ	Interrupt Request Output
RESET	System Reset Input
V <sub>ss</sub>	Ground
V <sub>cc</sub>	Supply Voltage

3828 PGM T01

## PIN CONFIGURATION



## X68C75

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### PIN DESCRIPTIONS

#### Address/Data (A/D<sub>0</sub>–A/D<sub>7</sub>)

Multiplexed low-order addresses and data. The addresses flow into the device while AS is HIGH. After AS transitions from a HIGH to LOW the addresses are latched. Once the addresses are latched these pins input data or output data depending on E, R/W, and CE.

#### Addresses (A<sub>8</sub>–A<sub>15</sub>)

High order addresses flow into the device when AS = V<sub>IH</sub> and are latched when AS goes low. In addition, A<sub>13</sub>, A<sub>14</sub> and A<sub>15</sub> are internally decoded to generate an Internal Chip Enable signal, thus eliminating the need for an external address decoder.

#### Chip Enable (CE)

The Chip Enable input must be HIGH to enable all read/write operations. When CE is LOW and AS is LOW, the X68C75 is placed in the low power standby mode.

#### Enable (E)

When used with a MC6801 or MC6803 the E input is tied directly to the E output of the microcontroller.

#### Read/Write (R/W)

When used with a MC6801 or MC6803 the R/W input is tied directly to the R/W output of the microcontroller.

#### Address Strobe (AS)

Addresses flow through the latches to address decoders when AS is HIGH and are latched when AS transitions from a HIGH to LOW.

#### Device Select (SEL)

Must be connected to V<sub>SS</sub>.

#### Write Control (WC)

The Write Control allows external circuitry to abort a page load cycle once it has been initiated. This input is useful in applications in which a power failure or processor RESET could interrupt a page load cycle. In this case, the microcontroller might drive all signals HIGH, causing bad data to be latched into the E<sup>2</sup>PROM. If the Write Control input is driven HIGH (t<sub>TBLC</sub> Max) after Read/Write (R/W) goes HIGH, the write cycle will be aborted. When WC is LOW (tied to V<sub>SS</sub>) the X68C75 will be enabled to perform write operations. When WC is HIGH normal read operations may be performed, but all attempts to write to the device will be disabled.

#### RESET (RESET)

The RESET input is used to reset the X68C75 to an initial state. Upon completion of the reset sequence, the X68C75 I/O ports will be configured as inputs, and all interrupts will be disabled.

#### Port A (PA<sub>0</sub>–PA<sub>7</sub>)

The PA<sub>0</sub>–PA<sub>7</sub> are the inputs or outputs of Port A.

#### Port B (PB<sub>0</sub>–PB<sub>7</sub>)

The PB<sub>0</sub>–PB<sub>7</sub> are the inputs or outputs of Port B.

#### Port Strobes A and B (STRA, STRB)

These signals are used to latch data either into or out of the respective Ports A and B.

#### Interrupt Request Output (IRQ)

The interrupt request output can be configured to generate an interrupt request to the microcontroller in the event of a valid transition on the STRA or STRB inputs.

# X68C75

## PRINCIPLES OF OPERATION

The X68C75 incorporates a specialized interface which utilizes the control signals and multiplexed Address/Data bus of the 8051 type of microcontroller to provide a "seamless" interface.

The control inputs on the X68C75 are configured such that it is possible to directly connect them to the proper interface signals of the 68HC11 type of microcontroller.

The falling edge of AS will latch the addresses for both a read and write operation. The state of R/W output determines the operation to be performed, with the E signal acting as a data strobe.

If R/W is HIGH and CE HIGH (read operation) data will be output on A/D<sub>0</sub>–A/D<sub>7</sub> after E transitions HIGH. If R/W is LOW and CE is HIGH (write operation) data presented at A/D<sub>0</sub>–A/D<sub>7</sub> will be strobed into the X68C64 on the HIGH to LOW transition of E.

The nonvolatile memory of the X68C75 is internally organized as two independent arrays of 4K bytes of memory with the A<sub>12</sub> input selecting which of the two blocks of memory are to be accessed. While the processor is executing code out of one block, write operations

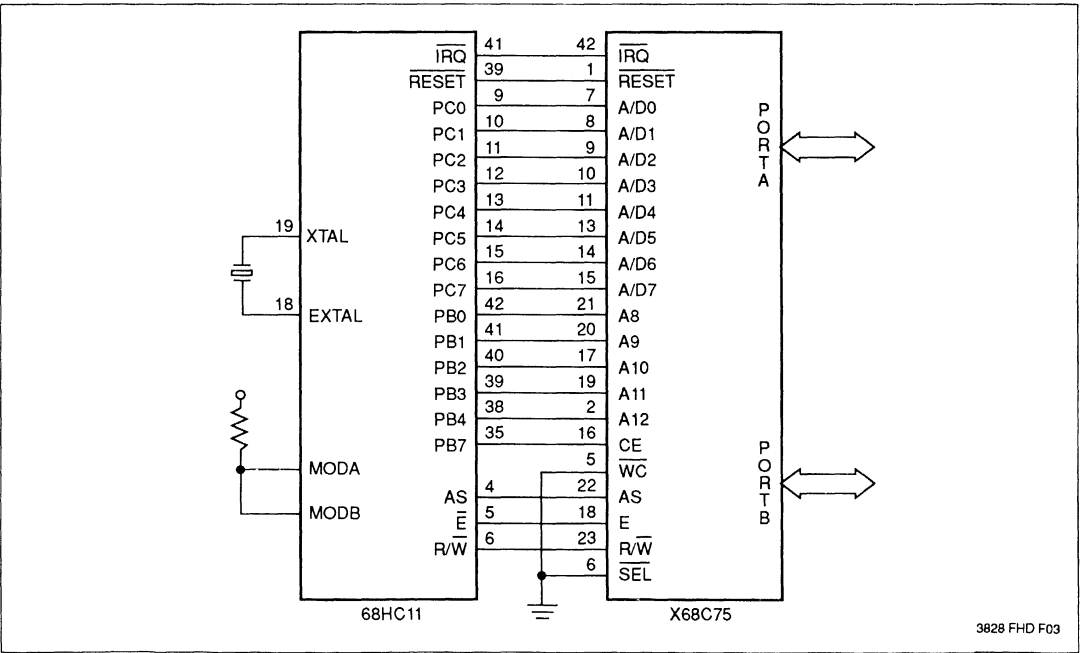
can take in the other block; allowing the processor to continue execution of code out of the X68C75 during a byte or page write to the device. This is called CONCURRENT READ WRITE™ feature.

The X68C75 also features an advanced implementation of the Software Data Protection scheme, called Block Protect, which allows the nonvolatile memory array to be broken into 8 independent sections of 1K Bytes Each of these sections can be independently enabled for write operations. This allows segmentation of the memory contents into writable and non-writable sections, thereby, allowing certain sections of the device to be secured so that updates can only occur in a controlled environment. (e.g. in an automotive application, only at an authorized service center). The block protect configuration is stored in a nonvolatile register, ensuring the configuration data will be maintained after the device is powered down.

The X68C75 also features a Write Control (WC) which serves as an external control over the completion of a previously initiated page load cycle.

The X68C75 also features the industry standard 5-volt E<sup>2</sup>PROM characteristics such as byte or page mode write and toggle-bit polling.

## Typical 68HC11/X68C75 System



**Fact Sheet**  
**8051 Microcontroller Family Compatible**



**8K**

**X88C75**

**8129 x 8 Bit**

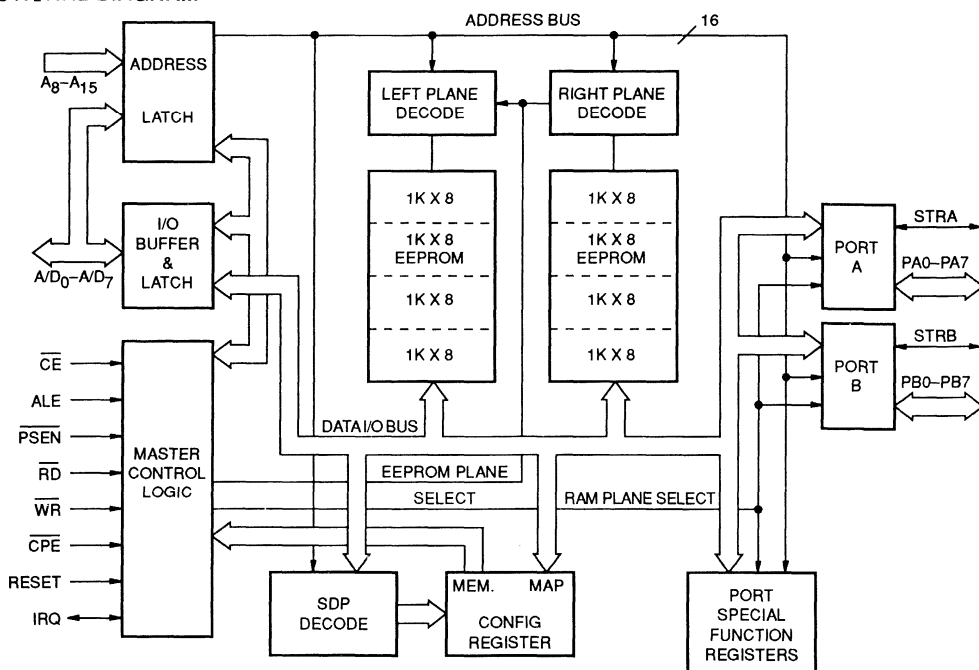
**Nonvolatile Program/Data Memory and I/O Port Expander**

**FEATURES**

- **Highly Integrated Microcontroller Peripheral**
  - 8K Bytes of 5-Volt Byte-Alterable Nonvolatile Memory
  - Nonvolatile Memory May Be Used for Program Storage, Data Storage or Both
  - Two General Purpose 8-Bit Bidirectional I/O Ports
  - Internal Programmable Address Decoding
- **CONCURRENT READ WRITE™**
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  - Isolates Read/Write Functions Between Planes
  - Allows Continuous Execution of Code from One Plane While Writing in the Other Plane
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  - Direct Interface to Popular Microcontrollers
  - 8051 Family
- **High Performance CMOS**
  - Fast Access Time, 120 ns
  - Low Power
    - 40 mA Active
    - 100 uA Standby
- **Software Data Protection**
  - Protect Entire Array During Power-up/-down
- **Block Protect Register**
  - Set write Lock Out in 1K Blocks
- **Toggle Bit**

**5**

**FUNCTIONAL DIAGRAM**



3820 FHD F01

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# X88C75

## DESCRIPTION

The X88C75 is a highly integrated peripheral for the 80C51 family of microcontrollers. The device integrates 8K bytes of 5 volt byte-alterable nonvolatile memory, two Bidirectional 8-Bit Ports, programmable internal address decoding and a multiplexed Address and Data Bus.

The 5 volt byte-alterable nonvolatile memory can be used as program storage, data storage or a combination of both. The memory array is separated into two 4K byte sections which allows read accesses to one-half while a write operation is taking place in the other half. The nonvolatile memory also features Software Data Protection to protect the contents during power transitions, and an advanced Block Protect Register which allows individual blocks of the memory to be configured as Read only or Read/Write.

Each bidirectional port consists of eight General Purpose I/O lines and one data strobe line. The ports also feature a configurable Interrupt Request output.

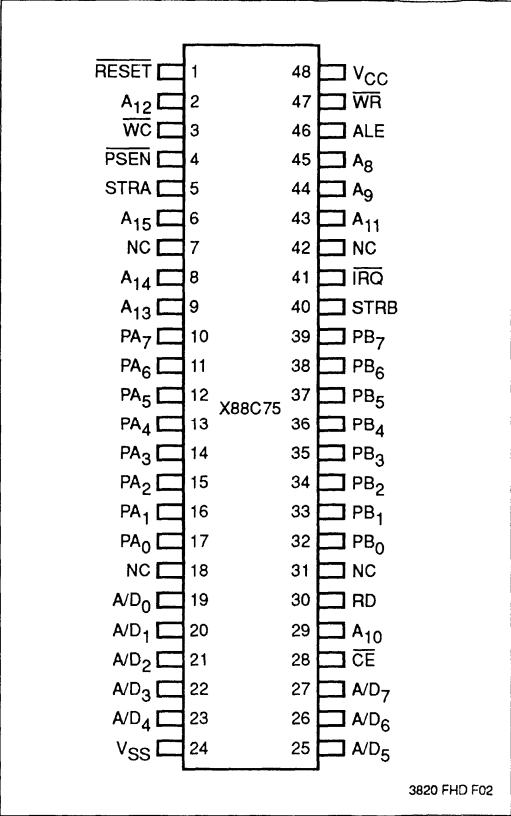
Access to the 88C75 is accomplished through the multiplexed Address/Data bus of the 80C51 type controller. An internal programmable address decoder maps the internal memory and register locations into the desired address space.

## PIN NAMES

Symbol	Description
ALE	Address Latch Enable
A/D <sub>0</sub> –A/D <sub>7</sub>	Address Inputs/Data I/O
A <sub>8</sub> –A <sub>15</sub>	Address Inputs
RD	Read Input
WR	Write Input
PSEN	Program Store Enable Input
WC	Write Control
CE	Chip Enable
PA <sub>0</sub> –PA <sub>7</sub>	Ports A I/O Lines
PB <sub>0</sub> –PB <sub>7</sub>	Port B I/O Lines
STRA,STRB	Port A and B Strobes
IRQ	Interrupt Request Output
RESET	System Reset Input
V <sub>ss</sub>	Ground
V <sub>cc</sub>	Supply Voltage

3820 PGM T01

## PIN CONFIGURATION



## X88C75

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### PIN DESCRIPTIONS

#### Address/Data ( $\overline{AD_0-AD_7}$ )

Multiplexed low-order addresses and data. The addresses flow into the device while ALE is HIGH. After ALE transitions from a HIGH to LOW the addresses are latched. Once the addresses are latched these pins input data or output data depending on  $\overline{RD}$ ,  $\overline{WR}$ ,  $\overline{PSEN}$  and  $\overline{CE}$ .

#### Addresses ( $A_8-A_{15}$ )

High order addresses flow into the device when ALE =  $V_{IH}$  and are latched when ALE =  $V_{IL}$ . In addition,  $A_{13}$ ,  $A_{14}$  and  $A_{15}$  are internally decoded to generate an Internal Chip Enable signal, thus eliminating the need for an external address decoder.

#### Chip Enable ( $\overline{CE}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH and ALE is HIGH, the X88C75 is placed in the low power standby mode.

#### Program Store Enable ( $\overline{PSEN}$ )

When the X88C75 is to be used in a MCS-51 based system,  $\overline{PSEN}$  is tied directly to the microcontroller's  $\overline{PSEN}$  output.

#### Read ( $\overline{RD}$ )

$\overline{RD}$  is tied directly to the microcontroller's  $\overline{RD}$  output.

#### Write ( $\overline{WR}$ )

$\overline{WR}$  is tied directly to the microcontroller's  $\overline{WR}$  output. The falling edge of  $\overline{WR}$  latches the high order addresses of the address to be written to. The rising edge of  $\overline{WR}$  latches the data to be written into the X88C75.

#### Address Latch Enable (ALE)

Addresses flow through the latches to address decoders when ALE is HIGH and are latched when ALE transitions from a HIGH to LOW.

#### Write Control ( $\overline{WC}$ )

The Write Control allows external circuitry to abort a page load cycle once it has been initiated. This input is useful in applications in which a power failure or processor RESET could interrupt a page load cycle. In this case, the microcontroller might drive all signals HIGH, causing bad data to be latched into the E<sup>2</sup>PROM. If the Write Control input is driven HIGH immediately after Write ( $\overline{WR}$ ) goes HIGH, the write cycle will be aborted. When  $\overline{WC}$  is LOW (tied to  $V_{SS}$ ) the X88C75 will be enabled to perform write operations. When  $\overline{WC}$  is HIGH normal read operations may be performed, but all attempts to write to the device will be disabled.

#### RESET ( $\overline{RESET}$ )

The RESET input is used to reset the X88C75 to an initial state. Upon completion of the reset sequence, the X88C75 I/O ports will be configured as inputs, and all interrupts will be disabled.

#### Port A ( $PA_0-PA_7$ )

The  $PA_0-PA_7$  are the inputs or outputs of Port A.

#### Port B ( $PB_0-PB_7$ )

The  $PB_0-PB_7$  are the inputs or outputs of Port B.

#### Port Strobes A and B (STRA, STRB)

These signals are used to latch data either into or out of the respective Ports A and B.

#### Interrupt Request Output ( $\overline{IRQ}$ )

The interrupt request output can be configured to generate an interrupt request to the microcontroller in the event of a valid transition on the STRA or STRB inputs.

# X88C75

## PRINCIPLES OF OPERATION

The X88C75 incorporates a specialized interface which utilizes the control signals and multiplexed Address/Data bus of the 8051 type of microcontroller to provide a "seamless" interface.

The control inputs on the X88C75 are configured such that it is possible to directly connect them to the proper interface signals of the 80C51 type of microcontroller. The reading of data from the chip is controlled either by the  $\overline{\text{PSEN}}$  or the  $\overline{\text{RD}}$  signal, which essentially maps the X88C75 into both the Program and the Data Memory address map.

Reading and writing of the nonvolatile memory array is analogous to executing the same operations to internal Static RAM of the 80C51 type microcontroller. During a write operation to either the nonvolatile memory or the control registers, ALE latches the address to be written into the X88C75. The falling edge of  $\overline{\text{WR}}$  latches the high order addresses, while the rising edge of  $\overline{\text{WR}}$  latches the data to be written.

The nonvolatile memory of the X88C75 is internally organized as two independent arrays of 4K bytes of memory with the  $\text{A}_{12}$  input selecting which of the two blocks of memory are to be accessed. While the proces-

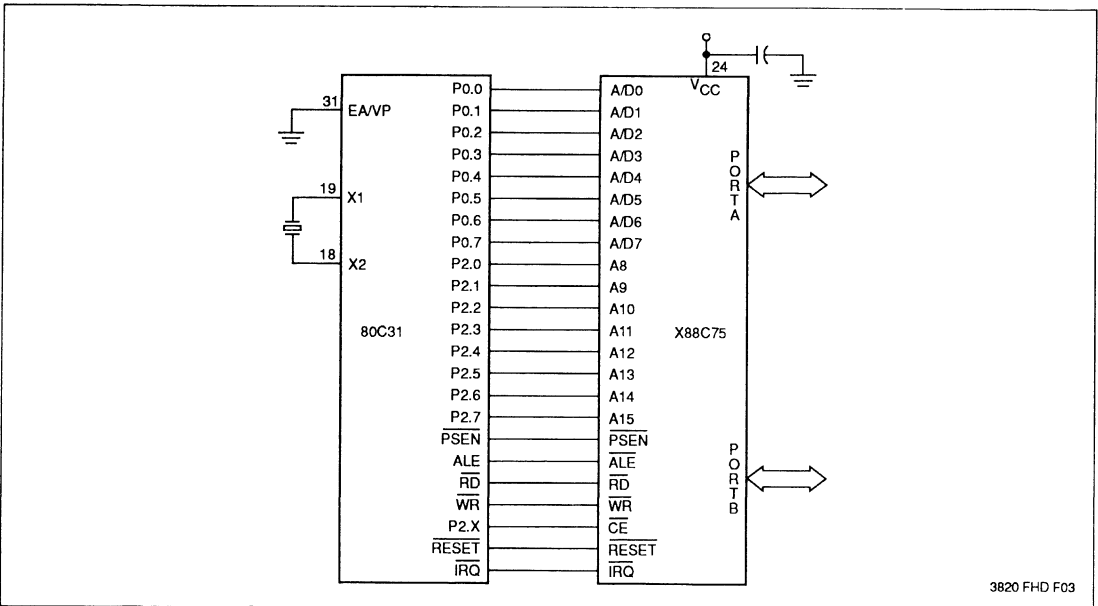
sor is executing code out of one block, write operations can take in the other block; allowing the processor to continue execution of code out of the X88C75 during a byte or page write to the device. This is called Concurrent Read Write™ feature.

The X88C75 also features an advanced implementation of the Software Data Protection scheme, called Block Protect, which allows the nonvolatile memory array to be broken into 8 independent sections of 1K Bytes. Each of these sections can be independently enabled for write operations. This allows segmentation of the memory contents into writable and non-writable sections, thereby, allowing certain sections of the device to be secured so that updates can only occur in a controlled environment. (e.g. in an automotive application, only at an authorized service center). The block protect configuration is stored in a nonvolatile register, ensuring the configuration data will be maintained after the device is powered down.

The X88C75 also features a Write Control ( $\overline{\text{WC}}$ ) which serves as an external control over the completion of a previously initiated page load cycle.

The X88C75 also features the industry standard 5 volt E<sup>2</sup>PROM characteristics such as byte or page mode write and toggle-bit polling.

## TYPICAL APPLICATION





<b>NOVRAM* Data Sheets</b>	<b>1</b>
<b>Serial Products Data Sheets</b>	<b>2</b>
<b>E<sup>2</sup>PROM Data Sheets</b>	<b>3</b>
<b>E<sup>2</sup>POT™ Data Sheets</b>	<b>4</b>
<b>Microcontroller Peripheral Products</b>	<b>5</b>
<b>Memory Subsystems</b>	<b>6</b>
<b>Military Products</b>	<b>7</b>
<b>Die Products</b>	<b>8</b>
<b>Application Notes and Briefs</b>	<b>9</b>
<b>Reliability</b>	<b>10</b>
<b>General Information</b>	<b>11</b>







## Preliminary Information

1 Megabit Module

**XM28C010**

128K x 8 Bit

**5 Volt, Byte Alterable E<sup>2</sup>PROM**

### TYPICAL FEATURES

- High Density 1 Megabit (128K x 8) E<sup>2</sup>PROM Module
- Access Time of 120 ns at -55°C to +125°C
- SIMPLE Byte and Page Write
  - Single 5 Volt Supply
  - No External High Voltages or V<sub>PP</sub> Control Circuits
- Self Timed
  - No Erase Before Write
  - No Complex Programming Algorithms
  - No Overerase Problem
- Base Memory Component: Xicor CMOS X28C256
- JEDEC Standard 32-Pin 600 MII Wide Ceramic Side Braze Package
- Pin Compatible with the X28C010 1Megabit Monolithic CMOS E<sup>2</sup>PROM

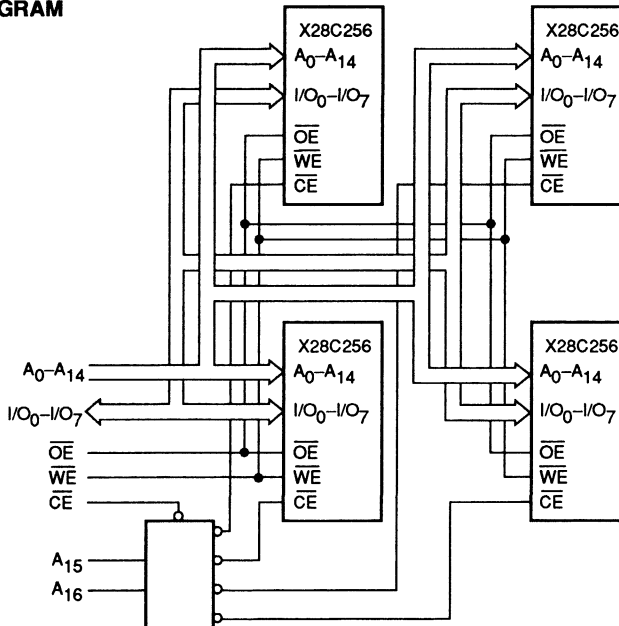
- Fast Write Cycle Times Supported by:
  - Internal Program Cycle 10 ms Max.
  - 64-byte Page
  - DATA Polling
  - Toggle Status Bit
- High Rel Module Available with:
  - 100% MIL-STD-883 Compliant Components
- Software Data Protection

### DESCRIPTION

The XM28C010 is a high density 1 Megabit E<sup>2</sup>PROM comprised of four X28C256 32K x 8 LCCs mounted on a co-fired multilayered ceramic substrate. The XM28C010 is configured 128K x 8 bit and features the JEDEC approved pinout for byte-wide memories, compatible with the monolithic X28C010.

6

### FUNCTIONAL DIAGRAM



3871 FHD F01

# XM28C010

## DESCRIPTION (Cont.)

The XM28C010 is available in commercial, industrial, and military temperature ranges. The High Rel module is built with MIL-STD-883 Class B microcircuit components. In addition, after being assembled all High Rel modules undergo 100% screening.

The XM28C010 supports a 64-byte page write operation, this, combined with DATA Polling or Toggle Bit testing, effectively provides a 78μs/byte write cycle, enabling the module memory array to be rewritten in 10 seconds.

The XM28C010 will also support Software Data Protection, a user-optional method of protecting data during power transitions.

The XM28C010 provides the same high endurance and data retention as the base memory components.

## PIN DESCRIPTIONS

### Addresses (A<sub>0</sub>–A<sub>16</sub>)

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{CE}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH, power consumption is reduced (see Note 4).

### Output Enable ( $\overline{OE}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

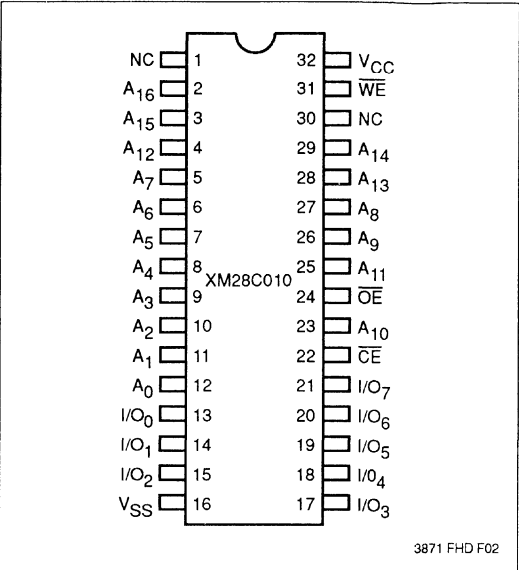
### Data In/Data Out (I/O<sub>0</sub>–I/O<sub>7</sub>)

Data is written to or read from the XM28C010 through the I/O pins.

### Write Enable ( $\overline{WE}$ )

The Write Enable input controls the writing of data to the XM28C010.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>16</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

3871 PGM T01

# XM28C010

## DEVICE OPERATION

### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The XM28C010 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms (see Note 4).

### Page Write Operation

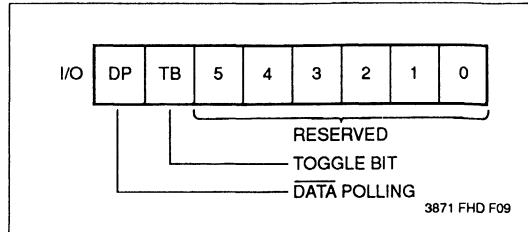
The page write feature of the XM28C010 allows the entire memory to be written in 10 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the XM28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address ( $A_6$  through  $A_{16}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100  $\mu$ s.

### Write Operation Status Bits

The XM28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



### DATA Polling (I/O<sub>7</sub>)

The XM28C010 features  $\overline{DATA}$  Polling as a method to indicate to the host system that the byte write or page write cycle has completed.  $\overline{DATA}$  Polling allows a simple bit test operation to determine the status of the XM28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O<sub>7</sub> (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O<sub>7</sub> will reflect true data. Note: If the XM28C010 is in the protected state and an illegal write operation is attempted  $\overline{DATA}$  Polling will not operate.

### Toggle Bit (I/O<sub>6</sub>)

The XM28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O<sub>6</sub> will toggle from one to zero and zero to one on subsequent attempts to read the last byte written. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

# XM28C010

DATA POLLING I/O<sub>7</sub>  
Figure 2. DATA Polling Bus Sequence

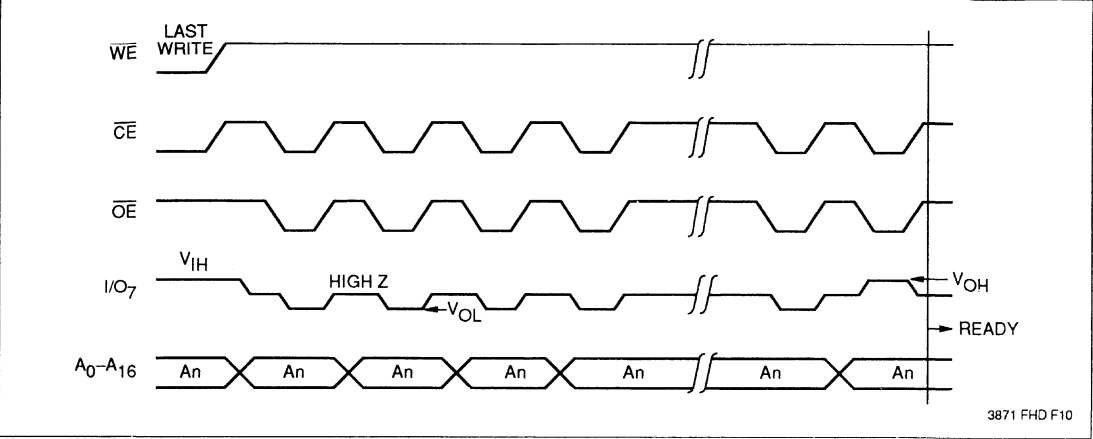
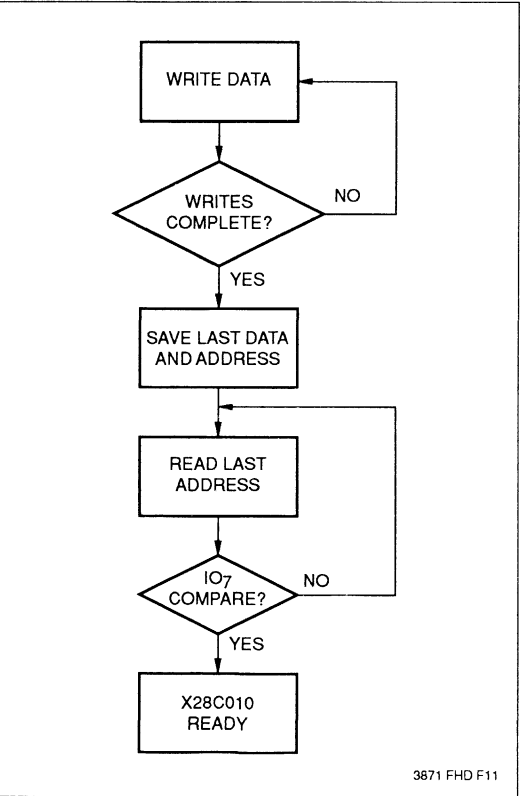


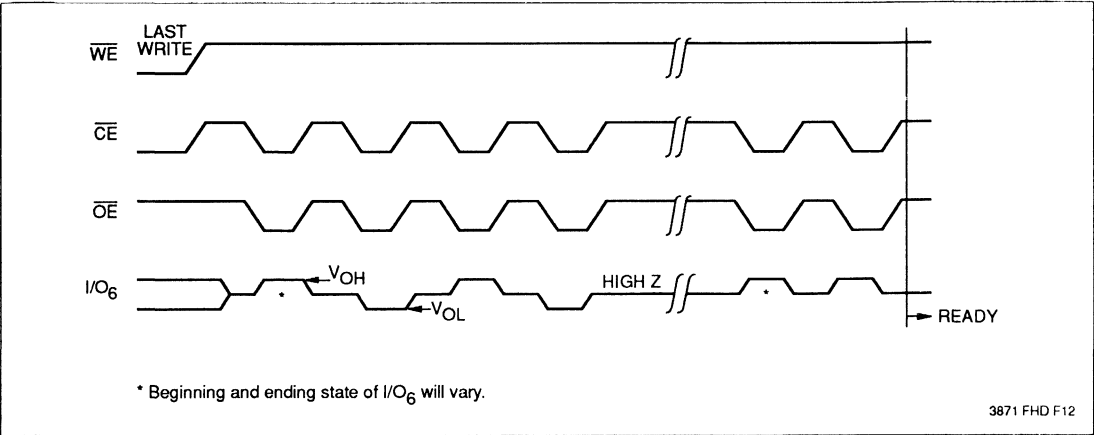
Figure 3. DATA Polling Software Flow



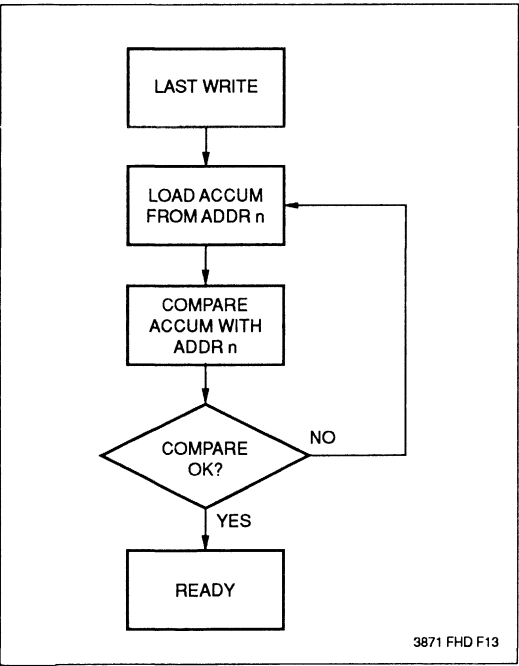
DATA Polling can effectively halve the time for writing to the XM28C010. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

**XM28C010**

**THE TOGGLE BIT I/O<sub>6</sub>**  
**Figure 4. Toggle Bit Bus Sequence**



**Figure 5. Toggle Bit Software Flow**



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple XM28C010 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

### HARDWARE DATA PROTECTION

The XM28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A  $\overline{WE}$  pulse less than 10 ns will not initiate a write cycle.
- Default  $V_{CC}$  Sense—All functions are inhibited when  $V_{CC}$  is  $\leq 3V$ .
- Write Inhibit—Holding  $\overline{OE}$  LOW will prevent an inadvertent write cycle during power-on and power-off.

### SOFTWARE DATA PROTECTION

The XM28C010 does provide the Software Data Protection (SDP) feature. Because the module is comprised of four discrete X28C256 LCCs, the algorithm will differ from the algorithm employed for the monolithic 1 Megabit X28C010.

The module is shipped from Xicor with the Software Data Protection NOT ENABLED; that is, the module will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host system will then have open read and write access of the module once  $V_{CC}$  is stable.

The module can be automatically protected during power-up/-down without the need for external circuits by employing the SDP feature. The internal SDP circuit is enabled after the first write operation utilizing the SDP command sequence.

When this feature is employed, it will be easiest to incorporate in the system software if the module is viewed as a subsystem composed of four discrete memory devices with an address decoder (see Func-

tional Diagram). In this manner, system memory mapping will extend onto the module. That is, the discrete memory ICs and decoder should be considered memory board components and SDP can be implemented at the component level as described in the next section.

### SOFTWARE COMMAND SEQUENCE

$A_{15}$  and  $A_{16}$  are used by the decoder to select one of the four LCCs. Therefore, only one of the four memory devices can be accessed at one time. In order to protect the entire module, the command sequence must be issued separately to each device.

Enabling the software data protection mode requires the host system to issue a series of three write operations: each write operation must conform to the data and address sequence illustrated in Figures 6 and 7. Because this involves writing to a nonvolatile bit the device will become protected after  $t_{WC}$  has elapsed. After this point in time devices will inhibit inadvertent write operations.

Once in the protected mode, authorized writes may be performed by issuing the same command sequence that enables SDP, immediately followed by the address/data combination desired. The command sequence opens the page write window enabling the host to write from one to sixty-four bytes of data. Once the data has been written, the device will automatically be returned to the protected state.

In order to facilitate testing of the devices the SDP mode can be deactivated. This is accomplished by issuing a series of six write operations: each write operation must conform to the data and address sequence illustrated in Figures 8 and 9. This is a nonvolatile operation, and the host will have to wait a minimum  $t_{WC}$  before attempting to write new data.

SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write

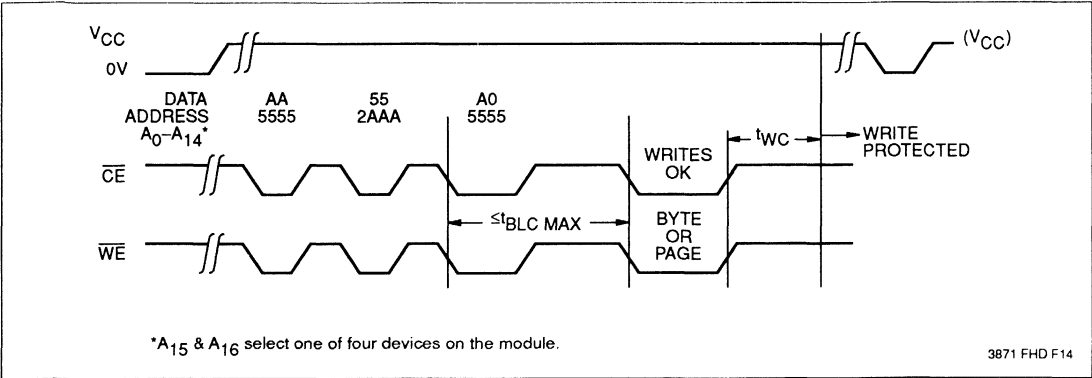
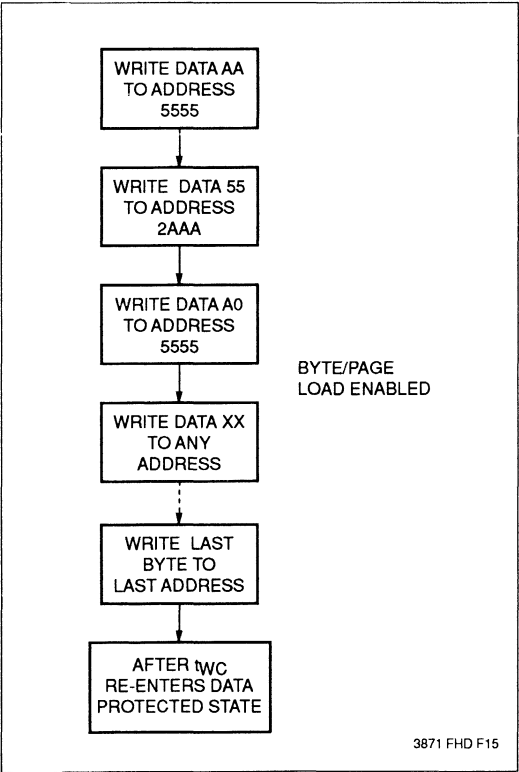


Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the device will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the device will be write protected during power-down and after any subsequent power-up.



RESETTING SOFTWARE DATA PROTECTION  
Figure 8. Reset Software Data Protection Timing Sequence

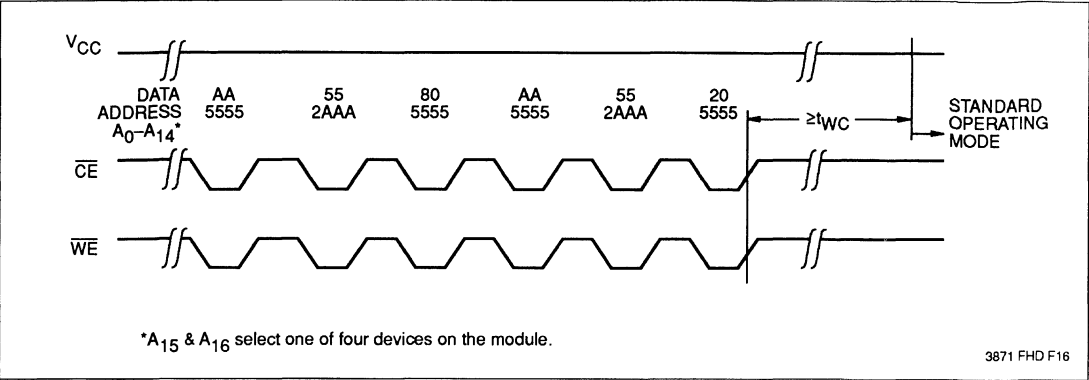
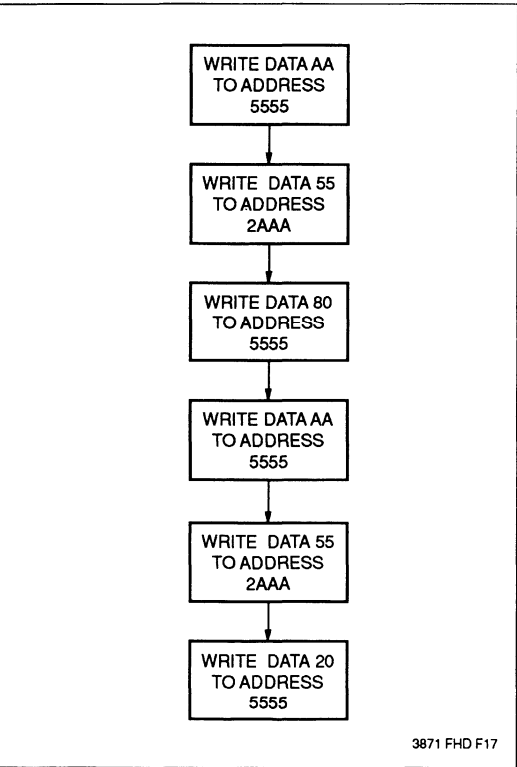


Figure 9. Software Sequence  
to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E<sup>2</sup>PROM programmer, the following six step algorithm will reset the internal protection circuit. After  $t_{WC}$ , the device will be in standard operating mode.

## XM28C010

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### SYSTEM CONSIDERATIONS

Because the XM28C010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the XM28C010 has two power modes, standby and active, proper decoupling of the memory array is of

prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu\text{F}$  high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7  $\mu\text{F}$  electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for every two modules employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

# XM28C010

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	-65°C to +135°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin with Respect to Ground .....	-1.0V to +7V
D.C. Output Current .....	5 mA
Lead Temperature (Soldering, 10 Seconds) .....	300°C

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. OPERATING CHARACTERISTICS

XM28C010  $T_A = 0^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{CC} = +5V \pm 10\%$ , unless otherwise specified.

XM28C010I  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +5V \pm 10\%$ , unless otherwise specified.

XM28C010M  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +5V \pm 10\%$ , unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
$I_{CC}$	$V_{CC}$ Current (Active) XM28C010-20-25		70	mA	$\overline{CE} = \overline{OE} = V_{IL}$ , $\overline{WE} = V_{IH}$ , All I/O's = Open, 1 Device Active Address Inputs = TTL Levels @ $f = 5\text{MHz}$
	XM28C010-12-15		90		
$I_{SB1}$	$V_{CC}$ Current (Standby) (TTL Inputs)		15	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = $V_{IH}$
$I_{SB2}$	$V_{CC}$ Current (Standby) -20-25 (CMOS Inputs) -12-15		800 2	$\mu\text{A}$ mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = $V_{CC}$
$I_{LI}$	Input Leakage Current		10	$\mu\text{A}$	$V_{IN} = \text{GND to } V_{CC}$
$I_{LO}$	Output Leakage Current		10	$\mu\text{A}$	$V_{OUT} = \text{GND to } V_{CC}$ , $\overline{CE} = V_{IH}$
$V_{IL}$	Input Low Voltage	-1.0	0.8	V	
$V_{IH}$	Input High Voltage	2.0	$V_{CC} + 1.0$	V	
$V_{OL}$	Output Low Voltage		0.4	V	$I_{OL} = 2.1\text{ mA}$
$V_{OH}$	Output High Voltage	2.4		V	$I_{OH} = -400\text{ }\mu\text{A}$

3871 PGM T02

## POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
$t_{PUR}^{(2)}$	Power-up to Read Operation	100	$\mu\text{s}$
$t_{PUW}^{(2)}$	Power-up to Write Operation	5	ms

3871 PGM T03

CAPACITANCE  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ ,  $V_{CC} = 5V$

Symbol	Test	Max.	Units	Test Conditions
$C_{I/O}^{(2)}$	Input/Output Capacitance	40	pF	$V_{I/O} = 0V$
$C_{IN}^{(2)}$	Input Capacitance	24	pF	$V_{IN} = 0V$

3871 PGM T04

Notes: (1) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.

(2) This parameter is periodically sampled and not 100% tested.

# XM28C010

## A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and $C_L = 100\text{pF}$

3871 PGM T05

## MODE SELECTION

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	I/O	Power
L	L	H	Read	DOUT	Active
L	H	L	Write	DIN	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3871 PGM T06

## A.C. CHARACTERISTICS

XM28C010  $T_A = 0^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

XM28C010I  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

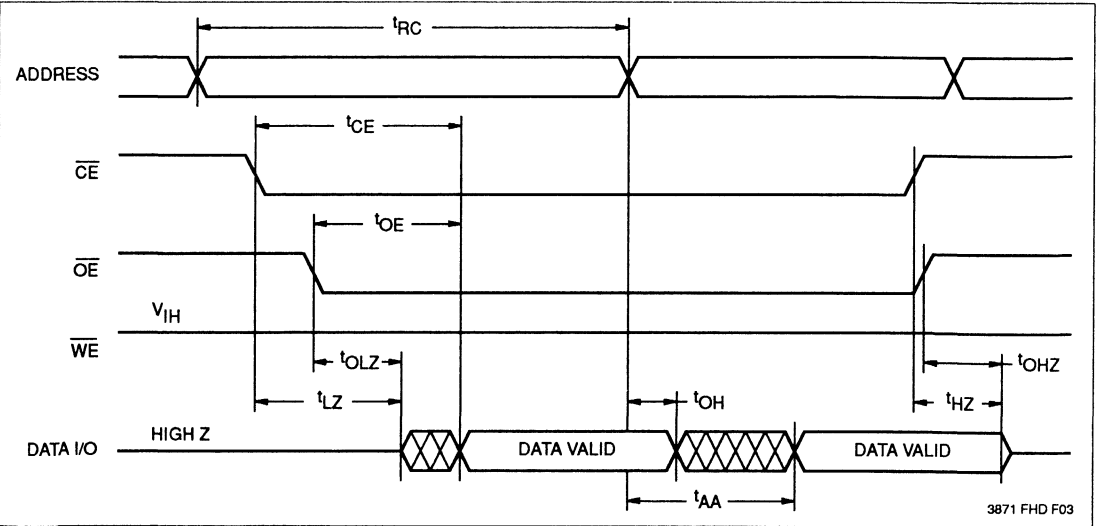
XM28C010M  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

### Read Cycle Limits

Symbol	Parameter	XM28C010-12		'-15		'-20		'-25		XM28C010		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	120		150		200		250		300		ns
$t_{CE}$	Chip Enable Access Time		120		150		200		250		300	ns
$t_{AA}$	Address Access Time		120		150		200		250		300	ns
$t_{OE}$	Output Enable Access Time		50		50		80		100		100	ns
$t_{LZ}^{(3)}$	CE Low to Active Output	0		0		0		0		0		ns
$t_{OLZ}^{(3)}$	OE Low to Active Output	0		0		0		0		0		ns
$t_{HZ}^{(4)}$	CE High to High Z Output		50		50		50		100		100	ns
$t_{OHZ}^{(4)}$	OE High to High Z Output		50		50		50		100		100	ns
$t_{OH}$	Output Hold from Address	0		0		0		0		0		ns

3871 PGM T07

### Read Cycle



Note: (3)  $t_{LZ}$  and  $t_{OLZ}$  are shown for reference only, they are periodically characterized and are not 100% tested.

(4)  $t_{HZ}$  and  $t_{OHZ}$  are measured from the point when  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

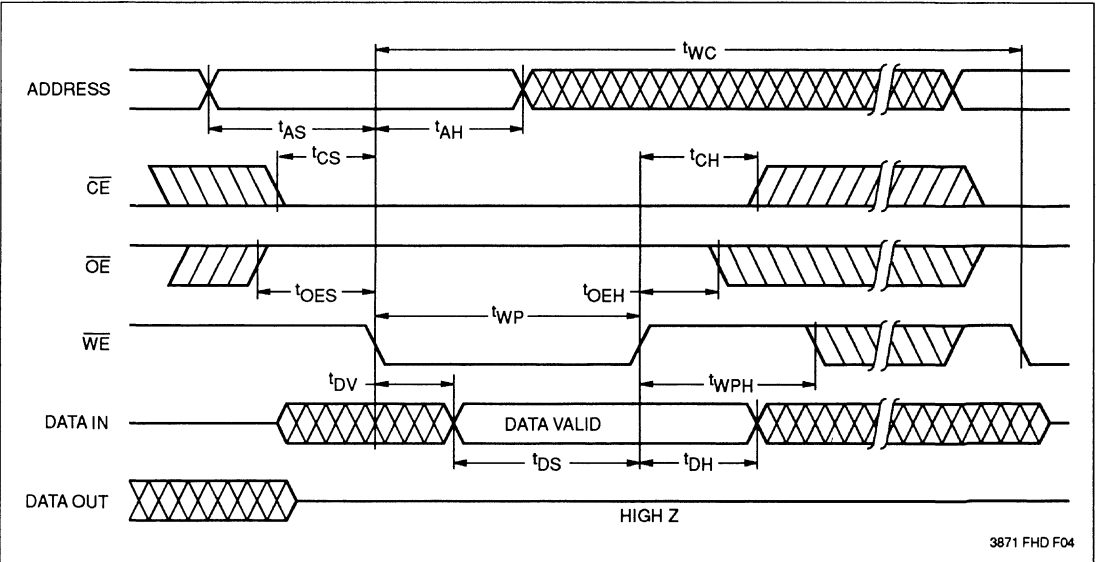
# **XM28C010**

## **Write Cycle Limits**

Symbol	Parameter	WE Controlled Write		CE Controlled Write <sup>(5)</sup>		Units
		Min.	Max.	Min.	Max.	
t <sub>WC</sub> <sup>(6)</sup>	Write Cycle Time		10		10	ms
t <sub>AS</sub>	Address Setup Time	0		0		ns
t <sub>AH</sub>	Address Hold Time	150		175		ns
t <sub>CS</sub>	Write Setup Time	25		0		ns
t <sub>CH</sub>	Write Hold Time	0		25		ns
t <sub>CW</sub>	CE Pulse Width	125		100		ns
t <sub>OES</sub>	OE High Setup Time	10		10		ns
t <sub>OEH</sub>	OE High Hold Time	10		35		ns
t <sub>WP</sub>	WE Pulse Width	100		125		ns
t <sub>WPH</sub>	WE High Recovery	1		1		μs
t <sub>DV</sub>	Data Valid		1		1	μs
t <sub>DS</sub>	Data Setup	50		50		ns
t <sub>DH</sub>	Data Hold	10		35		ns
t <sub>DW</sub>	Delay to Next Write	10		10		μs
t <sub>BLC</sub>	Byte Load Cycle	1	100	1	100	μs

3871 PGM T08

## **WE Controlled Write Cycle**

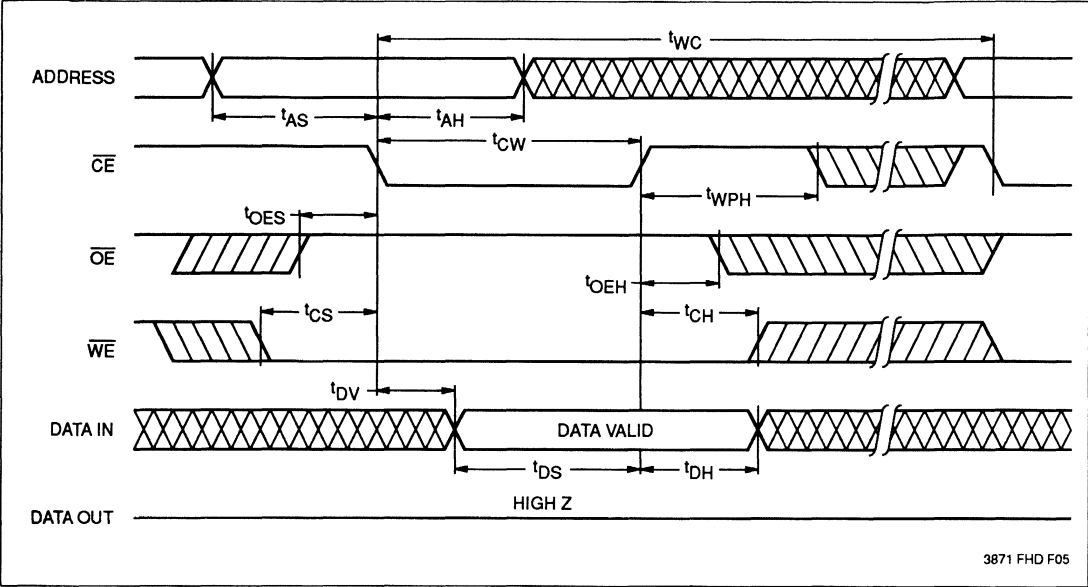


3871 FHD F04

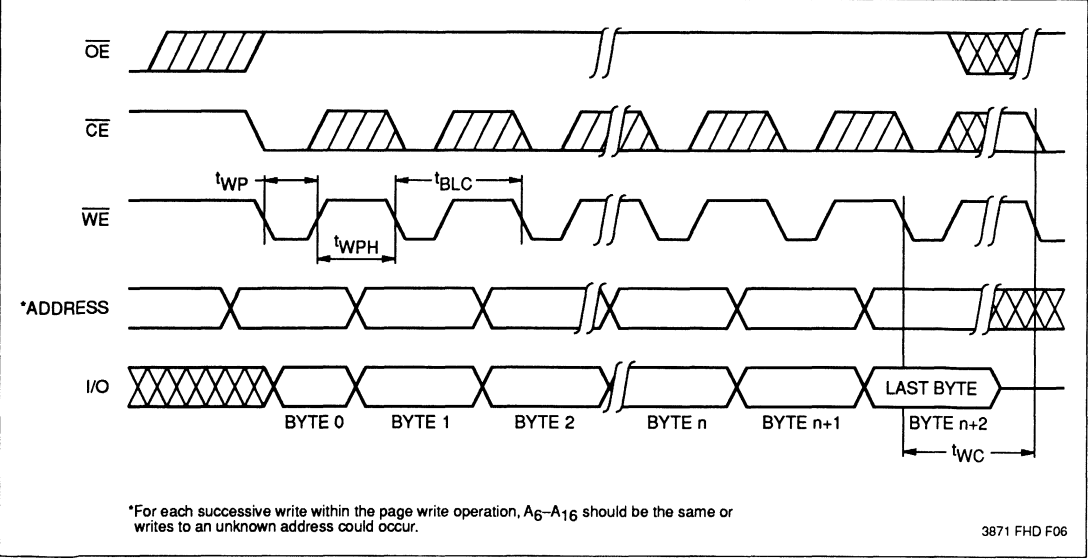
- Note:** (5) Due to the inclusion of the decoder IC on board the module the  $\overline{WE}$  and  $\overline{CE}$  write controlled timings will vary. When utilizing the  $\overline{CE}$  controlled write operation all the hold timings must be extended by the worst case propagation delay of the decoder. For a  $\overline{WE}$  controlled write operation  $\overline{CE}$  must be a minimum 125 ns to accommodate the additional setup time required.
- (6)  $t_{WC}$  is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete the interval write operation.

**XM28C010**

**$\overline{\text{CE}}$  Controlled Write Cycle**

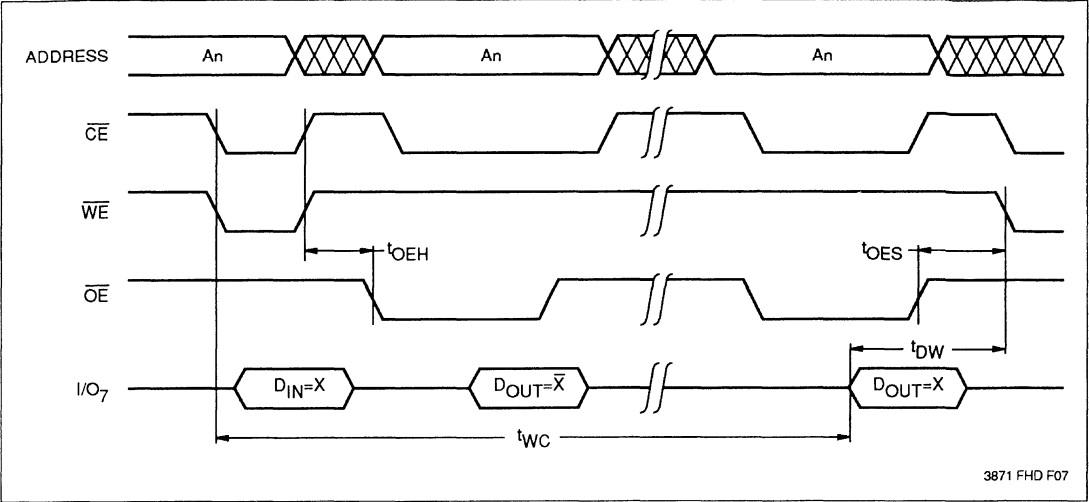


**Page Write Cycle**



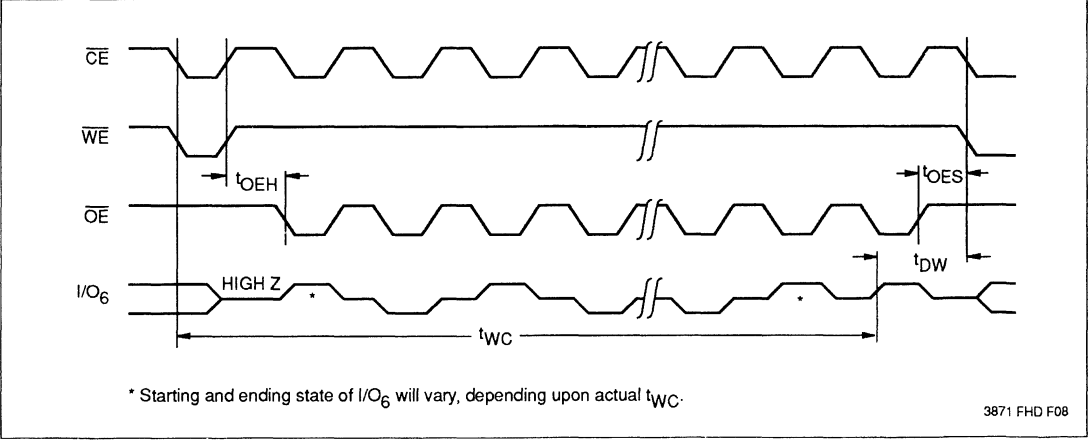
# **XM28C010**

**DATA Polling Timing Diagram**



3871 FHD F07






**Toggle Bit Timing Diagram**



\* Starting and ending state of  $I/O_6$  will vary, depending upon actual  $t_{WC}$ .

3871 FHD F08

**SYMBOL TABLE**

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance



**XM28C010**

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**NOTES**



## Advance Information

## 2 Megabit Module

## XM28C020

256K x 8 Bit

## 5 Volt, Byte Atterable E<sup>2</sup>PROM

### TYPICAL FEATURES

- High Density 2 Megabit (256K x 8) Module
- Access Time of 200ns at -55°C to +125°C
- Base Memory Component: Xicor X28C513
- Pinout conforms to JEDEC Standard for 2MEG E<sup>2</sup>PROM
- Fast Write Cycle Times
  - 128-byte Page Write
  - Byte or Page Write Cycle: 5ms Typical
  - Complete Memory Rewrite: 10 Seconds
- Early End of Write Detection
  - DATA Polling
  - Toggle Bit Polling
- Software Data Protection
- Three Temperature Ranges
  - Commercial: 0°C to +75°C
  - Industrial: -40° to +85°C
  - Military: -55° to +125°C
- High Rel Module
  - 100% MIL-STD-883 Compliant Components

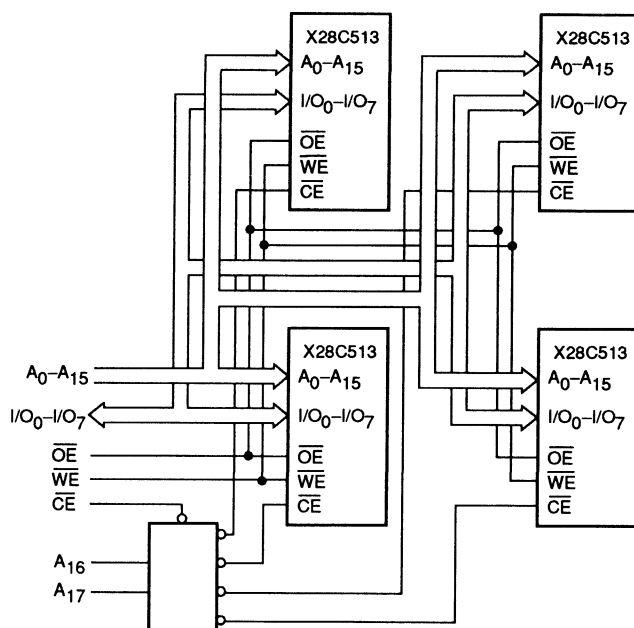
### DESCRIPTION

The XM28C020 is a high density 2 Megabit E<sup>2</sup>PROM comprised of four X28C513 64K x 8 LCCs mounted on a co-fired multilayered ceramic substrate. Individual components are 100% tested prior to assembly in module form and then 100% tested after assembly.

The XM28C020 is configured 256K x 8 bit. The module supports a 128-byte page write operation. This combined with DATA Polling or Toggle Bit Polling, effectively provides a 39μs/byte write cycle, enabling the entire array to be rewritten in 10 seconds.

The XM28C020 provides the same high endurance and data retention as the X28C513.

### FUNCTIONAL DIAGRAM



3872 FHD F01

# XM28C020

## PIN DESCRIPTIONS

### Addresses (A<sub>0</sub>–A<sub>17</sub>)

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{CE}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH, power consumption is reduced (see Note 4).

### Output Enable ( $\overline{OE}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

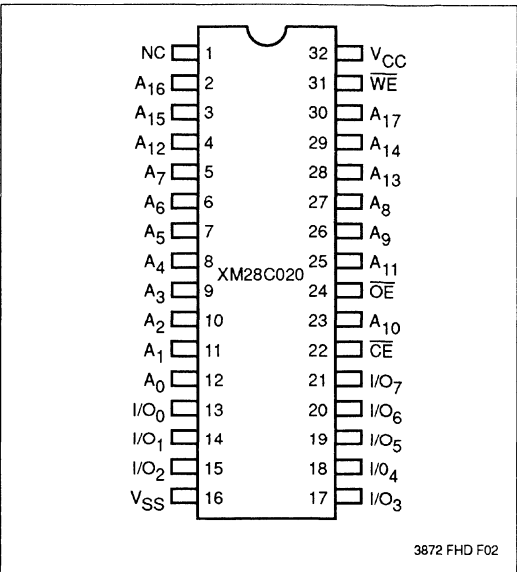
### Data In/Data Out (I/O<sub>0</sub>–I/O<sub>7</sub>)

Data is written to or read from the XM28C020 through the I/O pins.

### Write Enable ( $\overline{WE}$ )

The Write Enable input controls the writing of data to the XM28C020.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>17</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

3872 PGM T01

# XM28C020

## DEVICE OPERATION

### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The XM28C020 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms (see Note 4).

### Page Write Operation

The page write feature of the XM28C020 allows the entire memory to be written in 10 seconds. Page write allows two to 128 bytes of data to be consecutively written to the XM28C020 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address ( $A_7$  through  $A_{17}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

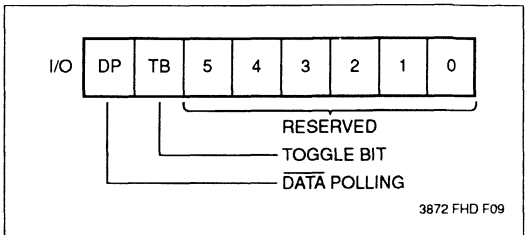
The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to 127 bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page

write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100  $\mu$ s.

### Write Operation Status Bits

The XM28C020 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



### DATA Polling (I/O<sub>7</sub>)

The XM28C020 features  $\overline{DATA}$  Polling as a method to indicate to the host system that the byte write or page write cycle has completed.  $\overline{DATA}$  Polling allows a simple bit test operation to determine the status of the XM28C020, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O<sub>7</sub> (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O<sub>7</sub> will reflect true data. Note: If the XM28C020 is in the protected state and an illegal write operation is attempted  $\overline{DATA}$  Polling will not operate.

### Toggle Bit (I/O<sub>6</sub>)

The XM28C020 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O<sub>6</sub> will toggle from one to zero and zero to one on subsequent attempts to read the last byte written. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

# XM28C020

## DATA POLLING I/O<sub>7</sub>

Figure 2. DATA Polling Bus Sequence

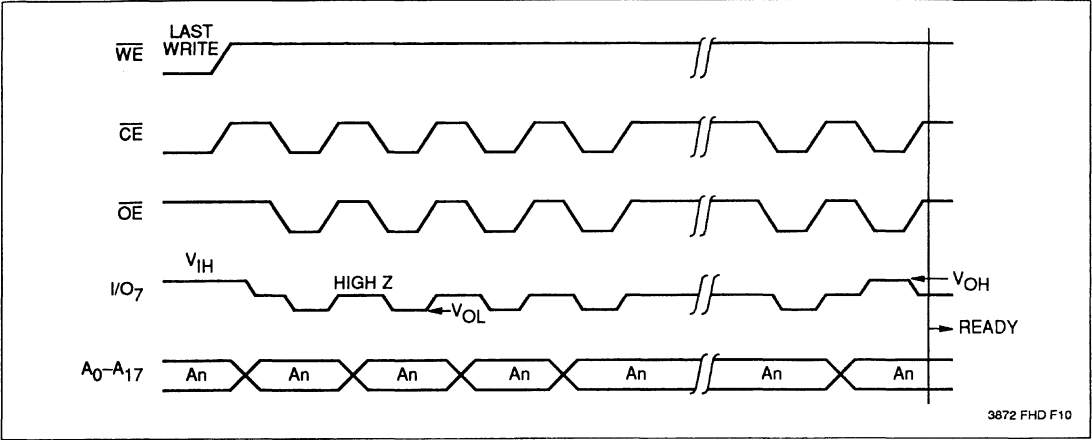
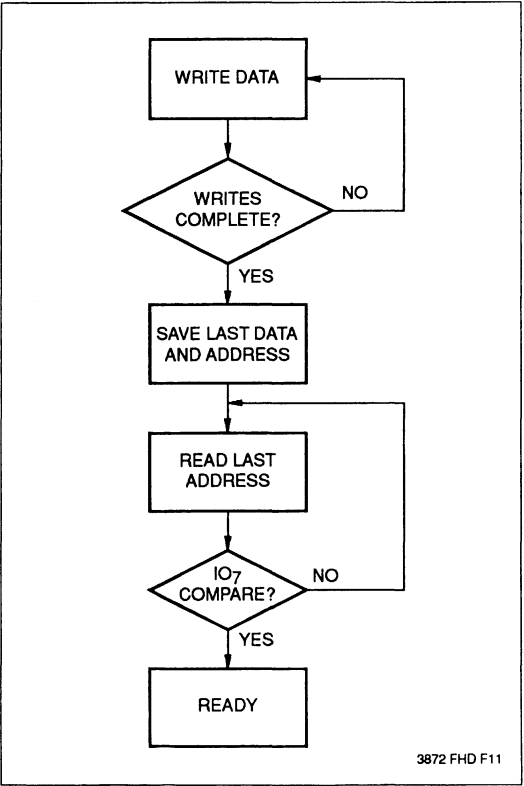


Figure 3. DATA Polling Software Flow

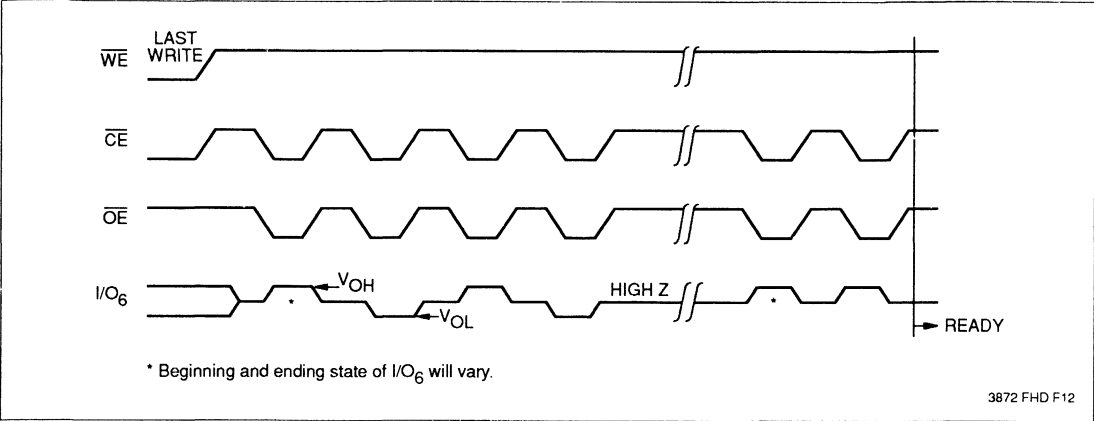


DATA Polling can effectively halve the time for writing to the XM28C020. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

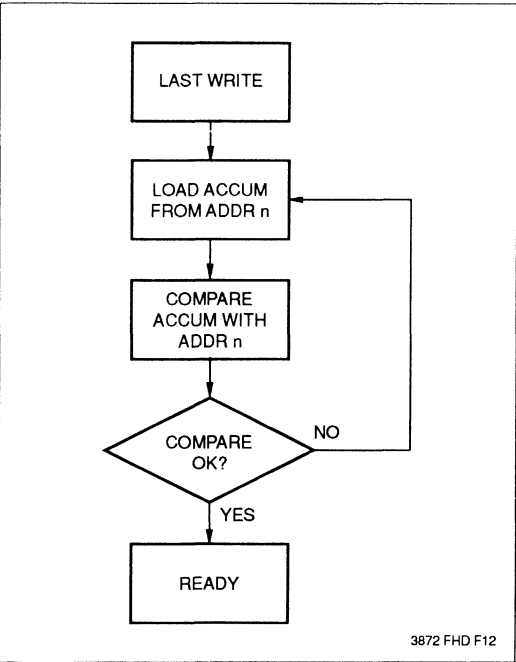
**XM28C020**

**THE TOGGLE BIT I/O<sub>6</sub>**

**Figure 4. Toggle Bit Bus Sequence**



**Figure 5. Toggle Bit Software Flow**



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple XM28C020 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

## XM28C020

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### HARDWARE DATA PROTECTION

The XM28C020 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A  $\overline{WE}$  pulse less than 10 ns will not initiate a write cycle.
- Default  $V_{CC}$  Sense—All functions are inhibited when  $V_{CC}$  is  $\leq 3V$ .
- Write Inhibit—Holding  $\overline{OE}$  LOW will prevent an inadvertent write cycle during power-on and power-off.

### SOFTWARE DATA PROTECTION

The XM28C020 does provide the Software Data Protection (SDP) feature.

The module is shipped from Xicor with the Software Data Protection NOT ENABLED; that is, the module will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host system will then have open read and write access of the module once  $V_{CC}$  is stable.

The module can be automatically protected during power-up/-down without the need for external circuits by employing the SDP feature. The internal SDP circuit is enabled after the first write operation utilizing the SDP command sequence.

When this feature is employed, it will be easiest to incorporate in the system software if the module is viewed as a subsystem composed of four discrete memory devices with an address decoder (see Functional Diagram). In this manner, system memory mapping will extend onto the module. That is, the discrete

memory ICs and decoder should be considered memory board components and SDP can be implemented at the component level as described in the next section.

### SOFTWARE COMMAND SEQUENCE

$A_{16}$  and  $A_{17}$  are used by the decoder to select one of the four LCCs. Therefore, only one of the four memory devices can be accessed at one time. In order to protect the entire module, the command sequence must be issued separately to each device.

Enabling the software data protection mode requires the host system to issue a series of three write operations: each write operation must conform to the data and address sequence illustrated in Figures 6 and 7. Because this involves writing to a nonvolatile bit the device will become protected after  $t_{WC}$  has elapsed. After this point in time devices will inhibit inadvertent write operations.

Once in the protected mode, authorized writes may be performed by issuing the same command sequence that enables SDP, immediately followed by the address/data combination desired. The command sequence opens the page write window enabling the host to write from one to 128 bytes of data. Once the data has been written, the device will automatically be returned to the protected state.

In order to facilitate testing of the devices the SDP mode can be deactivated. This is accomplished by issuing a series of six write operations: each write operation must conform to the data and address sequence illustrated in Figures 8 and 9. This is a nonvolatile operation, and the host will have to wait a minimum  $t_{WC}$  before attempting to write new data.





RESETTING SOFTWARE DATA PROTECTION  
Figure 8. Reset Software Data Protection Timing Sequence

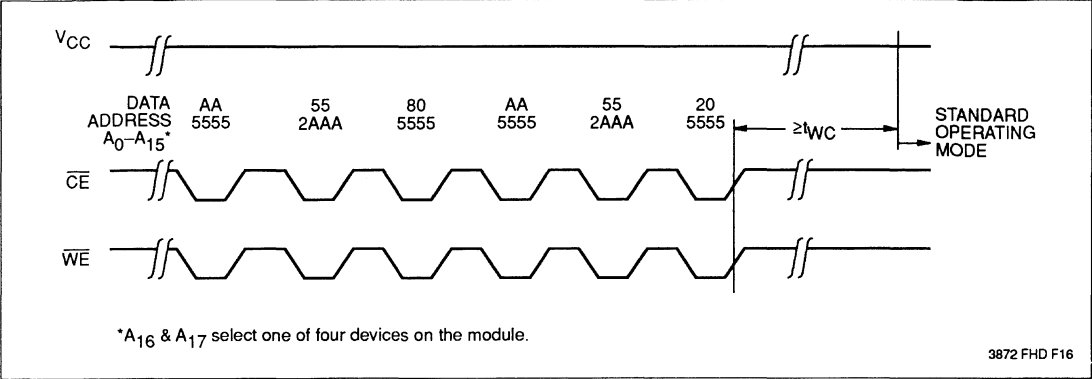
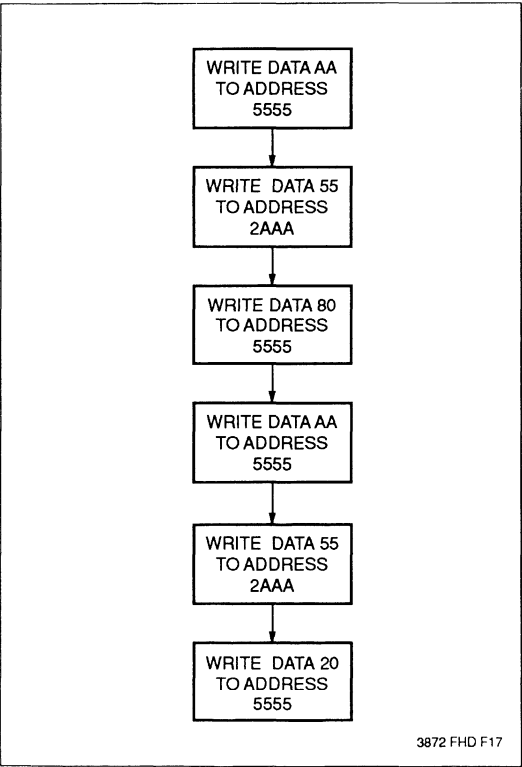


Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E<sup>2</sup>PROM programmer, the following six step algorithm will reset the internal protection circuit. After  $t_{WC}$ , the device will be in standard operating mode.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

## **XM28C020**

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### **SYSTEM CONSIDERATIONS**

Because the XM28C020 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the XM28C020 has two power modes, standby and active, proper decoupling of the memory array is of

prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu$ F high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7  $\mu$ F electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for every two modules employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

# XM28C020

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	-65°C to +135°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin with Respect to Ground .....	-1.0V to +7V
D.C. Output Current .....	5 mA
Lead Temperature (Soldering, 10 Seconds) .....	300°C

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. OPERATING CHARACTERISTICS

XM28C020  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +5V \pm 10\%$ , unless otherwise specified.

XM28C020I  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +5V \pm 10\%$ , unless otherwise specified.

XM28C020M  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +5V \pm 10\%$ , unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
$I_{CC}$	$V_{CC}$ Current (Active) (TTL Inputs)		60	mA	$\overline{CE} = \overline{OE} = V_{IL}$ , $\overline{WE} = V_{IH}$ , All I/O's = Open, 1 Device Active Address Inputs = TTL Levels @ $f = 5\text{MHz}$
$I_{SB1}$	$V_{CC}$ Current (Standby) (TTL Inputs)		15	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = $V_{IH}$
$I_{SB2}$	$V_{CC}$ Current (Standby) (CMOS Inputs)		5	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = $V_{CC}$
$I_{LI}$	Input Leakage Current		10	$\mu\text{A}$	$V_{IN} = \text{GND to } V_{CC}$
$I_{LO}$	Output Leakage Current		10	$\mu\text{A}$	$V_{OUT} = \text{GND to } V_{CC}$ , $\overline{CE} = V_{IH}$
$V_{IL}$	Input Low Voltage	-1.0	0.8	V	
$V_{IH}$	Input High Voltage	2.0	$V_{CC} + 1.0$	V	
$V_{OL}$	Output Low Voltage		0.4	V	$I_{OL} = 2.1\text{ mA}$
$V_{OH}$	Output High Voltage	2.4		V	$I_{OH} = -400\text{ }\mu\text{A}$

3856 PGM T02

## POWER-UP TIMING

Symbol	Parameter	Typ. <sup>(1)</sup>	Units
$t_{PUR}^{(2)}$	Power-up to Initiation of Read Operation	100	$\mu\text{s}$
$t_{PUW}^{(2)}$	Power-up to Initiation of Write Operation	5	ms

3872 PGM T03

**CAPACITANCE**  $T_A = 25^\circ\text{C}$ ,  $F = 1.0\text{ MHz}$ ,  $V_{CC} = 5V$

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}^{(2)}$	Input/Output Capacitance	50	pF	$V_{I/O} = 0V$
$C_{IN}^{(2)}$	Input Capacitance	50	pF	$V_{IN} = 0V$

3872 PGM T04

**Notes:** (1) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.

(2) This parameter is periodically sampled and not 100% tested.

XM28C020

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and $C_L = 100\text{pF}$

3872 PGM T05

MODE SELECTION

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	I/O	Power
L	L	H	Read	D <sub>OUT</sub>	Active
L	H	L	Write	D <sub>IN</sub>	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3872 PGM T06

A.C. CHARACTERISTICS

XM28C020  $T_A = 0^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

XM28C020I  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

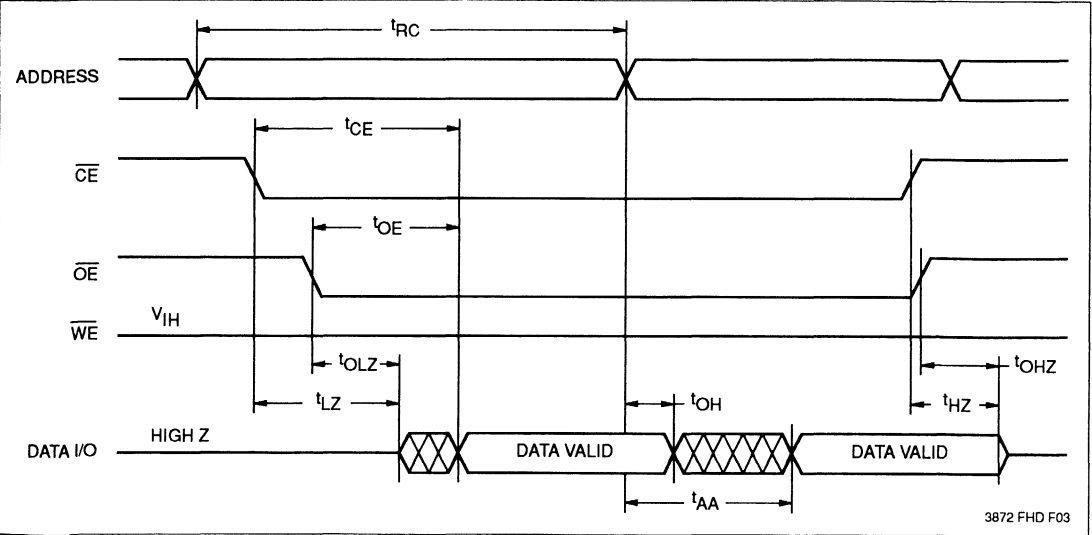
XM28C020M  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	XM28C020-20		XM28C020-25		XM28C020		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	200		250		300		ns
$t_{CE}$	Chip Enable Access Time		200		250		300	ns
$t_{AA}$	Address Access Time		200		250		300	ns
$t_{OE}$	Output Enable Access Time		80		100		100	ns
$t_{LZ}^{(3)}$	$\overline{\text{CE}}$ Low to Active Output	0		0		0		ns
$t_{OLZ}^{(3)}$	$\overline{\text{OE}}$ Low to Active Output	0		0		0		ns
$t_{HZ}^{(4)}$	$\overline{\text{CE}}$ High to High Z Output		100		100		100	ns
$t_{OHZ}^{(4)}$	$\overline{\text{OE}}$ High to High Z Output		100		100		100	ns
$t_{OH}$	Output Hold From Address Change	0		0		0		ns

3872 PGM T07

Read Cycle



3872 FHD F03

**Note:** (3)  $t_{LZ}$  and  $t_{OLZ}$  are shown for reference only, they are periodically characterized and are not 100% tested.

(4)  $t_{HZ}$  and  $t_{OHZ}$  are measured from the point when  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

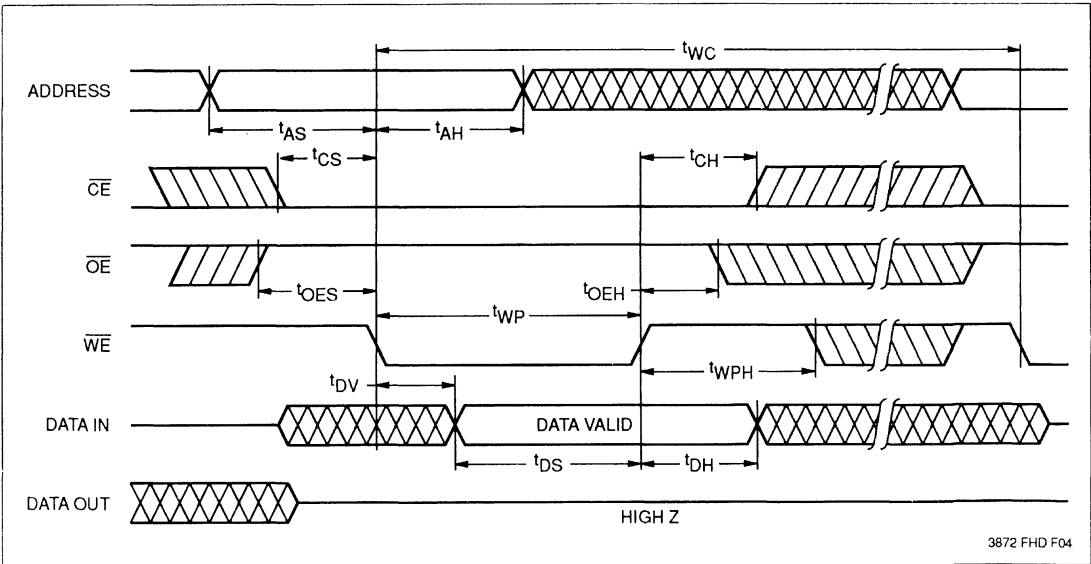
**XM28C020**

**Write Cycle Limits**

Symbol	Parameter	WE Controlled Write		CE Controlled Write <sup>(4)</sup>		Units
		Min.	Max.	Min.	Max.	
tWC	Write Cycle Time		10		10	ms
tAS	Address Setup Time	0		0		ns
tAH	Address Hold Time	125		125		ns
tCS	Write Setup Time	25		0		ns
tCH	Write Hold Time	0		25		ns
tCW	CE Pulse Width	125		100		ns
tOES	OE High Setup Time	10		10		ns
tOEH	OE High Hold Time	10		35		ns
tWP	WE Pulse Width	100		125		ns
tWPH	WE High Recovery	100		100		ns
tDV	Data Valid		1		1	μs
tDS	Data Setup	50		50		ns
tDH	Data Hold	10		35		ns
tDW	Delay to Next Write	10		10		μs
tBLC	Byte Load Cycle	.3	100	.3	100	μs

3872 PGM T08

**WE Controlled Write Cycle**

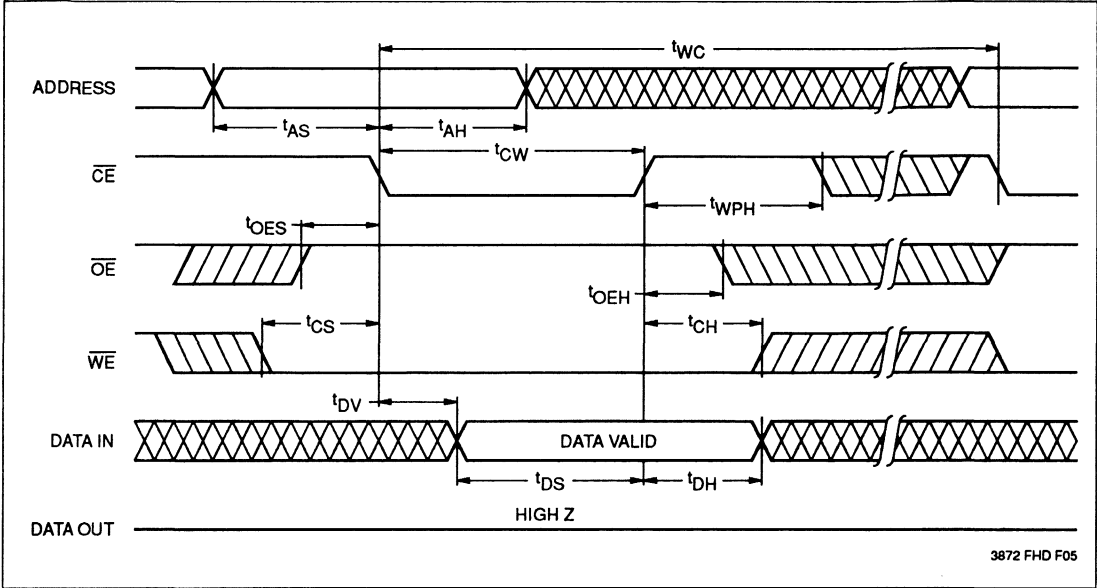


3872 FHD F04

**Note:** (4) Due to the inclusion of the decoder IC on board the module the WE and CE write controlled timings will vary. When utilizing the CE controlled write operation all the hold timings must be extended by the worst case propagation delay of the decoder. For a WE controlled write operation CE must be a minimum 125 ns to accommodate the additional setup time required.

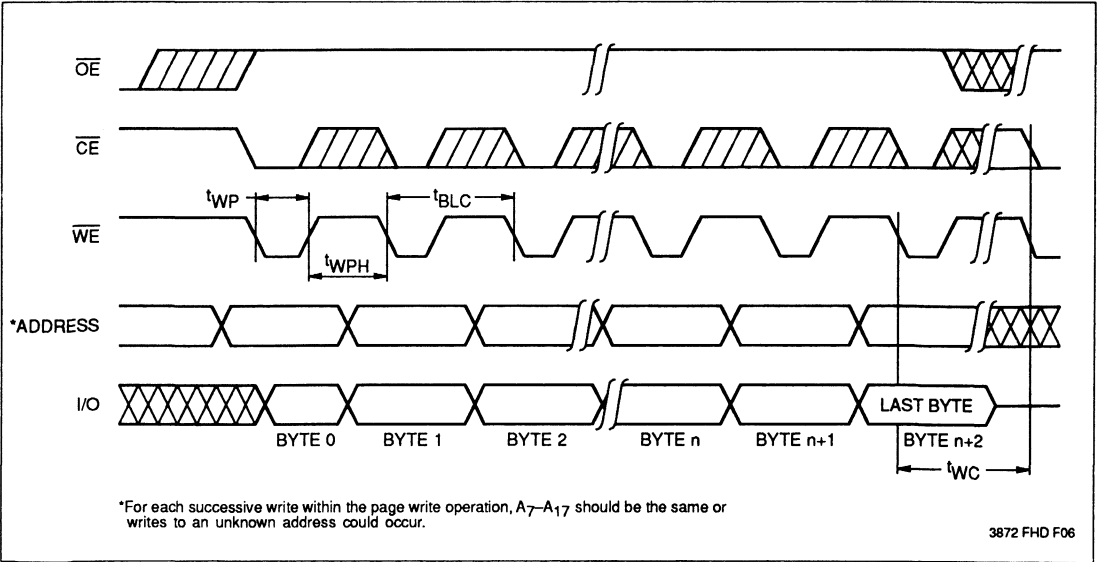
**XM28C020**

**$\overline{\text{CE}}$  Controlled Write Cycle**



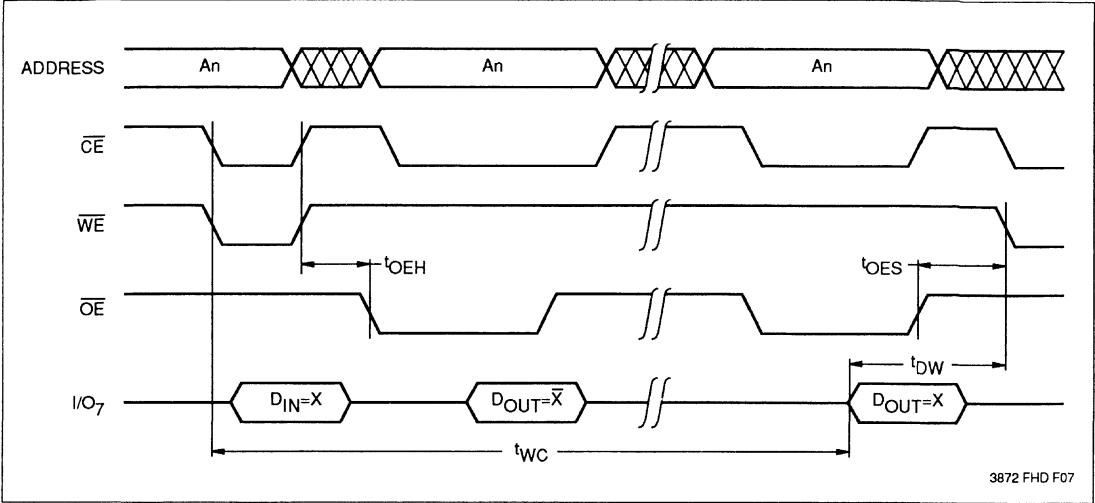
6

**Page Write Cycle**

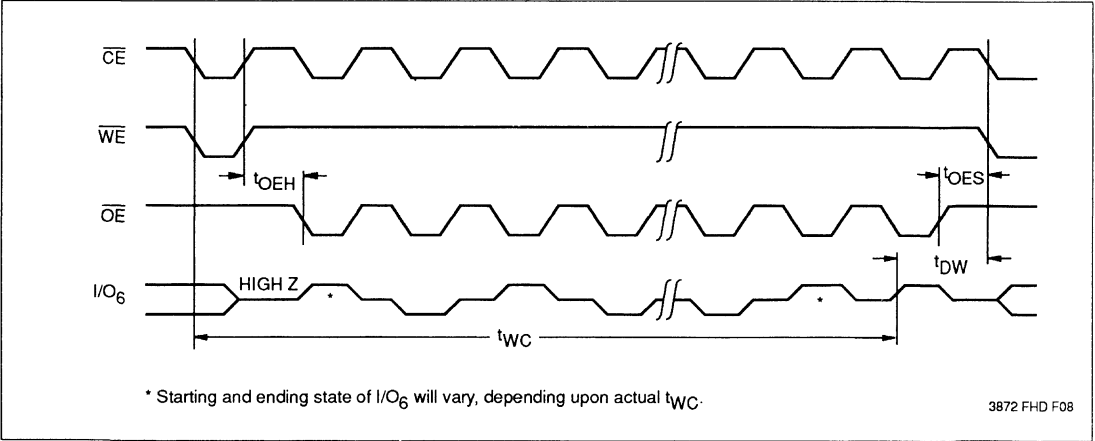


**XM28C020**

**DATA Polling Timing Diagram**



**Toggle Bit Timing Diagram**





## 4 Megabit Module

## XM28C040

512K x 8 Bit

5 Volt, Byte Alterable E<sup>2</sup>PROM

## TYPICAL FEATURES

- High Density 4 Megabit (512K x 8) Module
- Access Time of 200ns at -55°C to +125°C
- Base Memory Component: Xicor X28C010
- Pinout Conforms to JEDEC Standard for 4MEG E<sup>2</sup>PROM
- Fast Write Cycle Times
  - 256-byte Page Write
- Early End of Write Detection
  - DATA Polling
  - Toggle Bit Polling
- Software Data Protection
- Three Temperature Ranges
  - Commercial: 0°C to +75°C
  - Industrial: -40° to +85°C
  - Military: -55° to +125°C
- High Rel Modules all Components are MIL-STD-883 Compliant

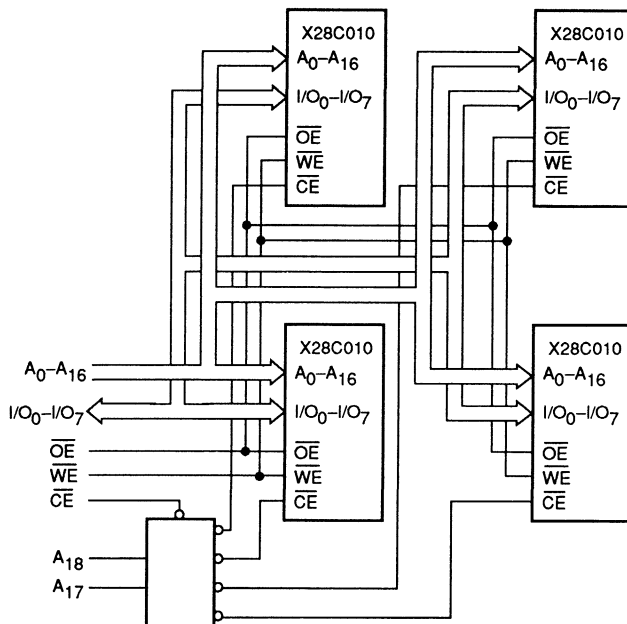
## DESCRIPTION

The XM28C040 is a high density 4 Megabit E<sup>2</sup>PROM comprised of four X28C010's mounted on a co-fired multilayered ceramic substrate. Individual components are 100% tested prior to assembly in module form and then 100% tested after assembly.

The XM28C040 is configured 512K x 8 bit. The module supports a 256-byte page write operation. This combined with DATA Polling or Toggle Bit Polling, effectively provides a 39μs/byte write cycle, enabling the entire array to be rewritten in 10 seconds.

The XM28C040 provides the same high endurance and data retention as the X28C010.

## FUNCTIONAL DIAGRAM



3873 FHD F01



# XM28C040

## PIN DESCRIPTIONS

### Addresses (A<sub>0</sub>–A<sub>18</sub>)

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{\text{CE}}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{\text{CE}}$  is HIGH, power consumption is reduced (see Note 4).

### Output Enable ( $\overline{\text{OE}}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

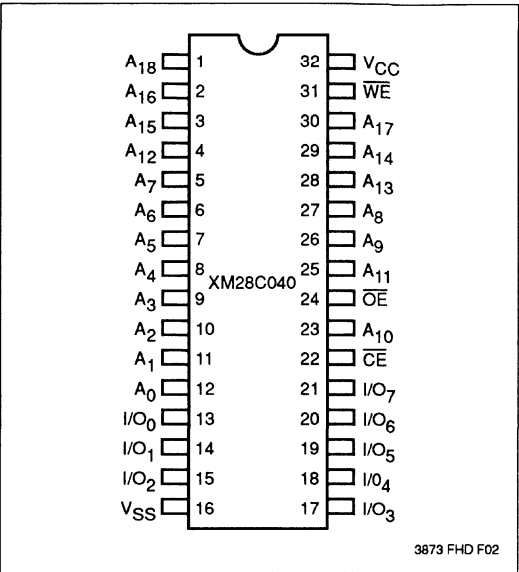
### Data In/Data Out (I/O<sub>0</sub>–I/O<sub>7</sub>)

Data is written to or read from the XM28C040 through the I/O pins.

### Write Enable ( $\overline{\text{WE}}$ )

The Write Enable input controls the writing of data to the XM28C040.

## PIN CONFIGURATION



## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>18</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>8</sub>	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

3873 PGM T01

# XM28C040

## DEVICE OPERATION

### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The XM28C040 supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms (see Note 4).

### Page Write Operation

The page write feature of the XM28C040 allows the entire memory to be written in 10 seconds. Page write allows two to 256 bytes of data to be consecutively written to the XM28C040 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address ( $A_8$  through  $A_{18}$ ) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to 255 bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 100  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 100  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host

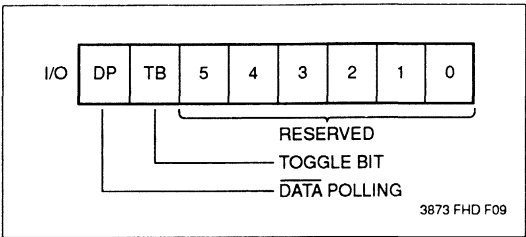
continues to access the device within the byte load cycle time of 100  $\mu$ s.

### Write Operation Status Bits

The XM28C040 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

### DATA Polling (I/O<sub>7</sub>)

Figure 1. Status Bit Assignment



The XM28C040 features  $\overline{DATA}$  Polling as a method to indicate to the host system that the byte write or page write cycle has completed.  $\overline{DATA}$  Polling allows a simple bit test operation to determine the status of the XM28C040, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O<sub>7</sub> (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O<sub>7</sub> will reflect true data. Note: If the XM28C040 is in the protected state and an illegal write operation is attempted  $\overline{DATA}$  Polling will not operate.

### Toggle Bit (I/O<sub>6</sub>)

The XM28C040 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O<sub>6</sub> will toggle from one to zero and zero to one on subsequent attempts to read the last byte written. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

# XM28C040

DATA POLLING I/O<sub>7</sub>  
Figure 2. DATA Polling Bus Sequence

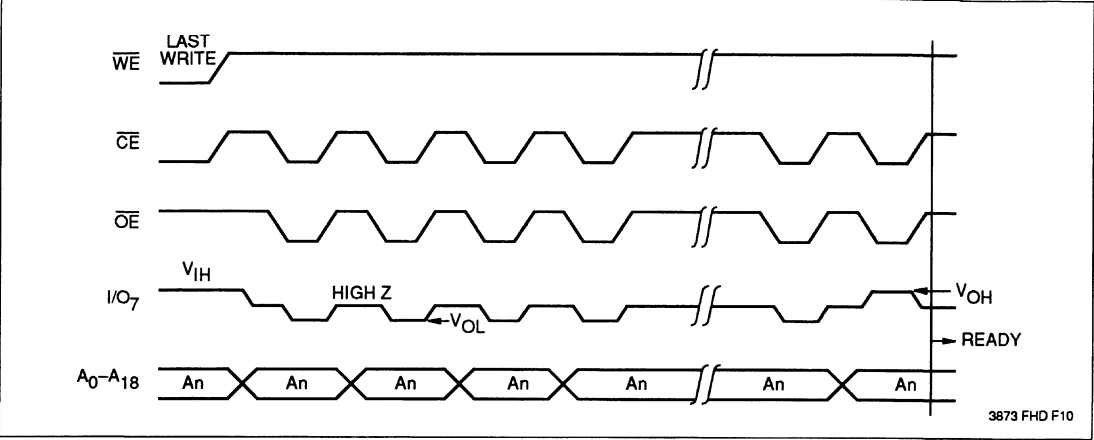
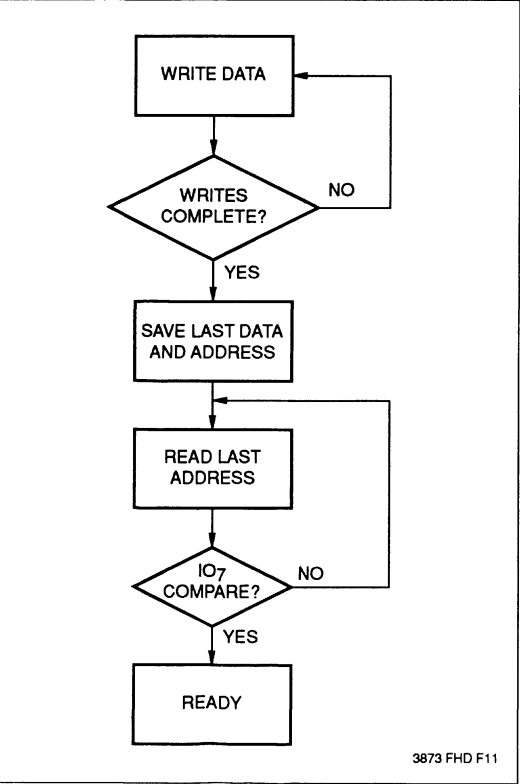


Figure 3. DATA Polling Software Flow



DATA Polling can effectively halve the time for writing to the XM28C040. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

XM28C040

THE TOGGLE BIT I/O<sub>6</sub>  
Figure 4. Toggle Bit Bus Sequence

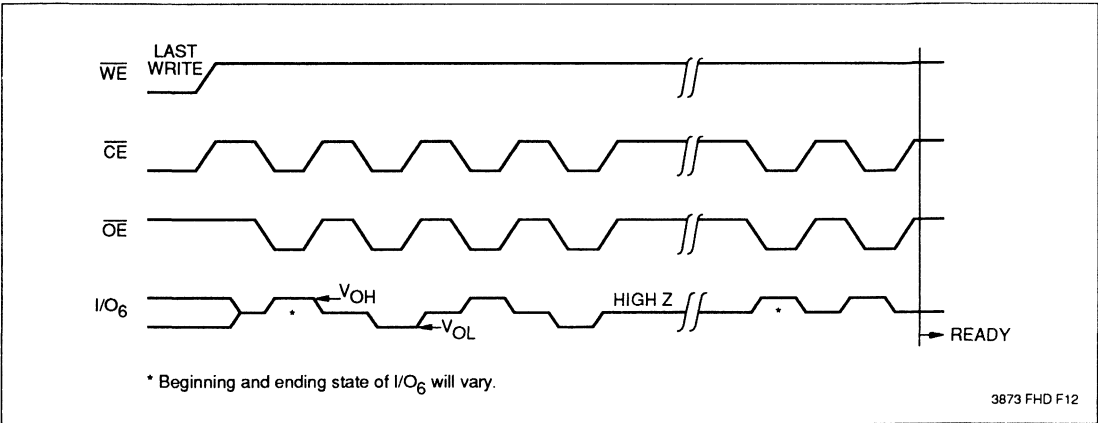
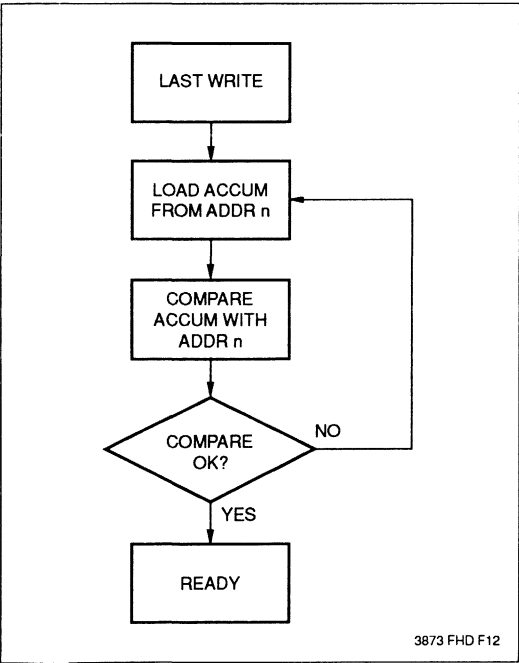


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple XM28C040 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

## XM28C040

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### HARDWARE DATA PROTECTION

The XM28C040 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A  $\overline{WE}$  pulse less than 10 ns will not initiate a write cycle.
- Default  $V_{CC}$  Sense—All functions are inhibited when  $V_{CC}$  is  $\leq 3V$ .
- Write Inhibit—Holding  $\overline{OE}$  LOW will prevent an inadvertent write cycle during power-on and power-off.

### SOFTWARE DATA PROTECTION

The XM28C040 does provide the Software Data Protection (SDP) feature.

The module is shipped from Xicor with the Software Data Protection NOT ENABLED; that is, the module will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host system will then have open read and write access of the module once  $V_{CC}$  is stable.

The module can be automatically protected during power-up/-down without the need for external circuits by employing the SDP feature. The internal SDP circuit is enabled after the first write operation utilizing the SDP command sequence.

When this feature is employed, it will be easiest to incorporate in the system software if the module is viewed as a subsystem composed of four discrete memory devices with an address decoder (see Functional Diagram). In this manner, system memory mapping will extend onto the module. That is, the discrete

memory ICs and decoder should be considered memory board components and SDP can be implemented at the component level as described in the next section.

### SOFTWARE COMMAND SEQUENCE

$A_{17}$  and  $A_{18}$  are used by the decoder to select one of the four LCCs. Therefore, only one of the four memory devices can be accessed at one time. In order to protect the entire module, the command sequence must be issued separately to each device.

Enabling the software data protection mode requires the host system to issue a series of three write operations: each write operation must conform to the data and address sequence illustrated in Figures 6 and 7. Because this involves writing to a nonvolatile bit the device will become protected after  $t_{WC}$  has elapsed. After this point in time devices will inhibit inadvertent write operations.

Once in the protected mode, authorized writes may be performed by issuing the same command sequence that enables SDP, immediately followed by the address/data combination desired. The command sequence opens the page write window enabling the host to write from one to 256 bytes of data. Once the data has been written, the device will automatically be returned to the protected state.

In order to facilitate testing of the devices the SDP mode can be deactivated. This is accomplished by issuing a series of six write operations: each write operation must conform to the data and address sequence illustrated in Figures 8 and 9. This is a nonvolatile operation, and the host will have to wait a minimum  $t_{WC}$  before attempting to write new data.

# XM28C040

## SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write

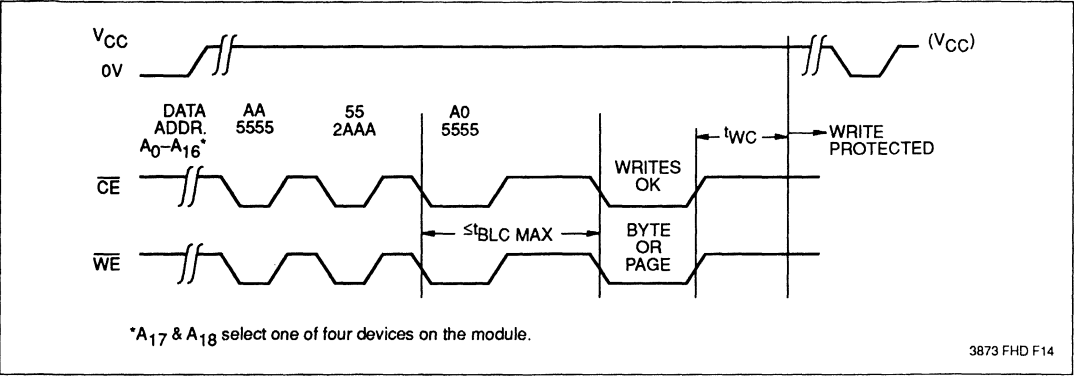
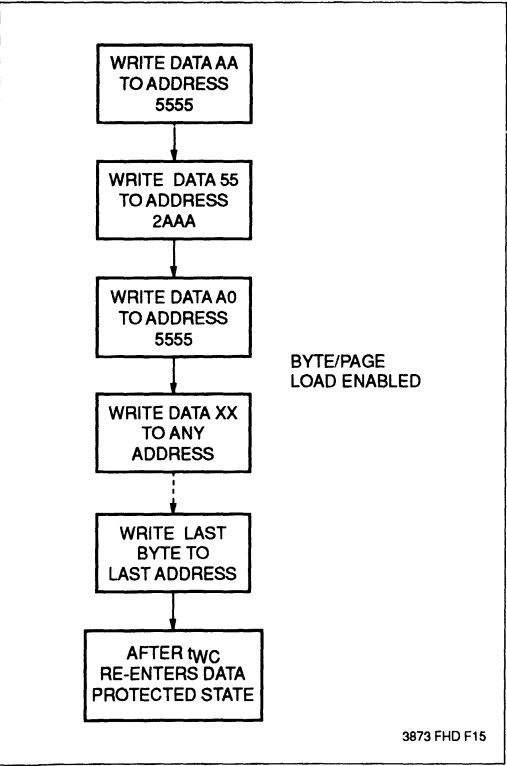


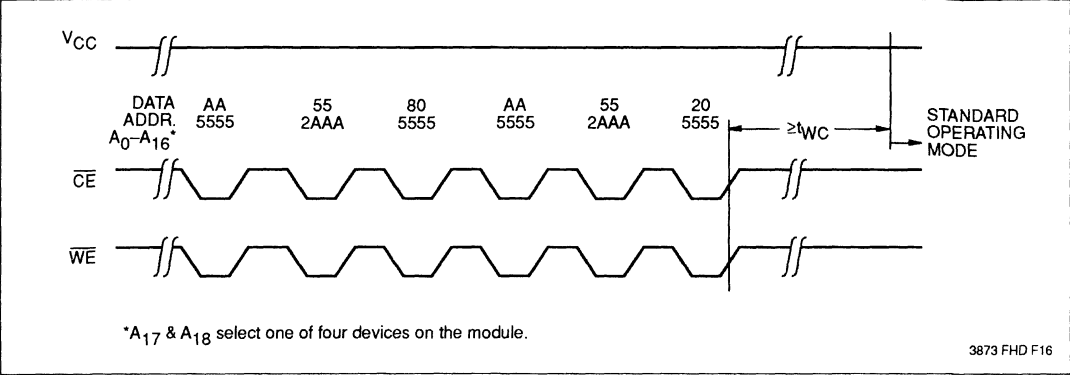
Figure 7. Write Sequence for Software Data Protection



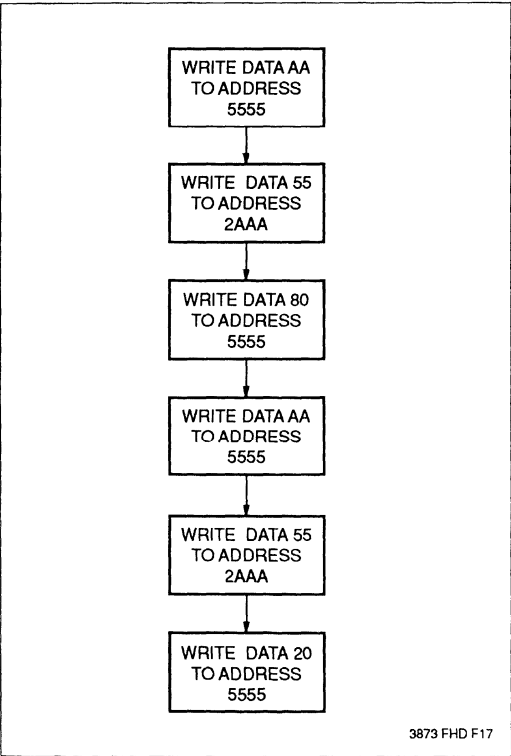
Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the device will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the device will be write protected during power-down and after any subsequent power-up.

**RESETTING SOFTWARE DATA PROTECTION**

**Figure 8. Reset Software Data Protection Timing Sequence**



**Figure 9. Software Sequence to Deactivate Software Data Protection**



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E<sup>2</sup>PROM programmer, the following six step algorithm will reset the internal protection circuit. After  $t_{WC}$ , the device will be in standard operating mode.

## XM28C040

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### SYSTEM CONSIDERATIONS

Because the XM28C040 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the XM28C040 has two power modes, standby and active, proper decoupling of the memory array is of

prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu\text{F}$  high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7  $\mu\text{F}$  electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for every two modules employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.



# XM28C040

### ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	-65°C to +135°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin with Respect to Ground .....	-1.0V to +7V
D.C. Output Current .....	5 mA
Lead Temperature (Soldering, 10 Seconds) .....	300°C

### \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### D.C. OPERATING CHARACTERISTICS

XM28C040 T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = +5V ± 10%, unless otherwise specified.  
XM28C040I T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = +5V ± 10%, unless otherwise specified.  
XM28C040M T<sub>A</sub> = -55°C to +125°C, V<sub>CC</sub> = +5V ± 10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Current (Active) (TTL Inputs)		80	mA	$\overline{CE} = \overline{OE} = V_{IL}$ , $\overline{WE} = V_{IH}$ , All I/O's = Open, 1 Device Active Address Inputs = TTL Levels @ f = 5MHz
I <sub>SB</sub>	V <sub>CC</sub> Current (Standby)		5	mA	$\overline{CE}$ , A <sub>17</sub> , A <sub>18</sub> = V <sub>CC</sub> - 0.3V All other inputs = V <sub>IH</sub> All I/Os = OPEN
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , $\overline{CE} = V_{IH}$
V <sub>IL</sub>	Input Low Voltage	-1.0	0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> + 1.0	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -400 μA

3873 PGM T02

### POWER-UP TIMING

Symbol	Parameter	Typ. <sup>(1)</sup>	Units
t <sub>PUR</sub> <sup>(2)</sup>	Power-up to Initiation of Read Operation	100	ms
t <sub>PUW</sub> <sup>(2)</sup>	Power-up to Initiation of Write Operation	5	ms

3873 PGM T03

### CAPACITANCE

Symbol	Parameter	Max.	Units	Test Conditions
C <sub>I/O</sub> <sup>(2)</sup>	Input/Output Capacitance	50	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> <sup>(2)</sup>	Input Capacitance	50	pF	V <sub>IN</sub> = 0V

3873 PGM T04

Notes: (1) Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage.  
(2) This parameter is periodically sampled and not 100% tested.

# XM28C040

## A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and $C_L = 100\text{pF}$

3873 PGM T05

## MODE SELECTION

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	I/O	Power
L	L	H	Read	DOUT	Active
L	H	L	Write	DIN	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3873 PGM T06

## A.C. CHARACTERISTICS

XM28C040  $T_A = 0^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

XM28C040I  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

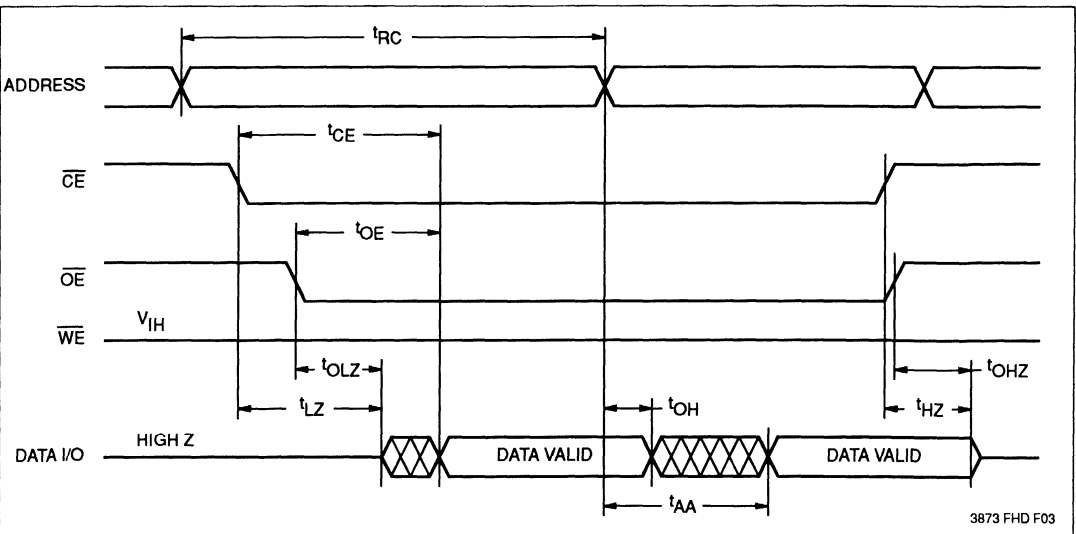
XM28C040M  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

### Read Cycle Limits

Symbol	Parameter	XM28C040-20		XM28C040-25		XM28C040		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	200		250		300		ns
$t_{CE}$	Chip Enable Access Time		200		250		300	ns
$t_{AA}$	Address Access Time		200		250		300	ns
$t_{OE}$	Output Enable Access Time		80		100		100	ns
$t_{LZ}^{(4)}$	$\overline{\text{CE}}$ Low to Active Output	0		0		0		ns
$t_{OLZ}^{(4)}$	$\overline{\text{OE}}$ Low to Active Output	0		0		0		ns
$t_{HZ}^{(4)}$	$\overline{\text{CE}}$ High to High Z Output		100		100		100	ns
$t_{OHZ}^{(4)}$	$\overline{\text{OE}}$ High to High Z Output		100		100		100	ns
$t_{OH}$	Output Hold From Address Change	0		0		0		ns

3873 PGM T07

### Read Cycle



**Note:** (3)  $t_{HZ}$  and  $t_{OHZ}$  are measured from the point when  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

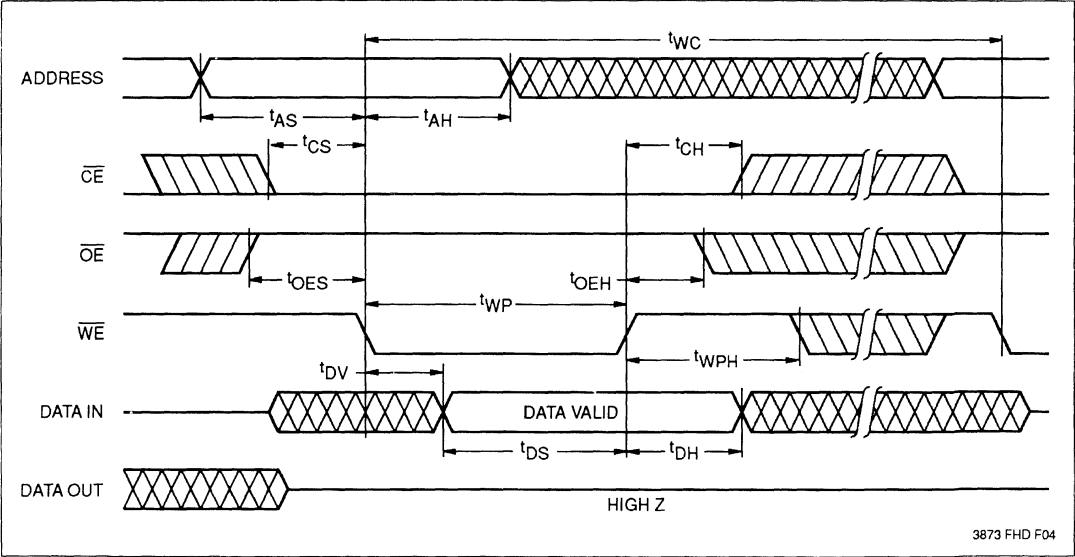
XM28C040

Write Cycle Limits

Symbol	Parameter	WE Controlled Write		CE Controlled Write <sup>(4)</sup>		Units
		Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time		10		10	ms
t <sub>AS</sub>	Address Setup Time	0		0		ns
t <sub>AH</sub>	Address Hold Time	125		125		ns
t <sub>CS</sub>	Write Setup Time	25		0		ns
t <sub>CH</sub>	Write Hold Time	0		25		ns
t <sub>CW</sub>	CE Pulse Width	125		100		ns
t <sub>OES</sub>	OE High Setup Time	10		10		ns
t <sub>OEH</sub>	OE High Hold Time	10		35		ns
t <sub>WP</sub>	WE Pulse Width	100		125		ns
t <sub>WPH</sub>	WE High Recovery	100		100		ns
t <sub>DV</sub>	Data Valid		1		1	μs
t <sub>DS</sub>	Data Setup	50		50		ns
t <sub>DH</sub>	Data Hold	10		35		ns
t <sub>DW</sub>	Delay to Next Write	10		10		μs
t <sub>BLC</sub>	Byte Load Cycle	.3	100	.3	100	μs

3873 PGM T08

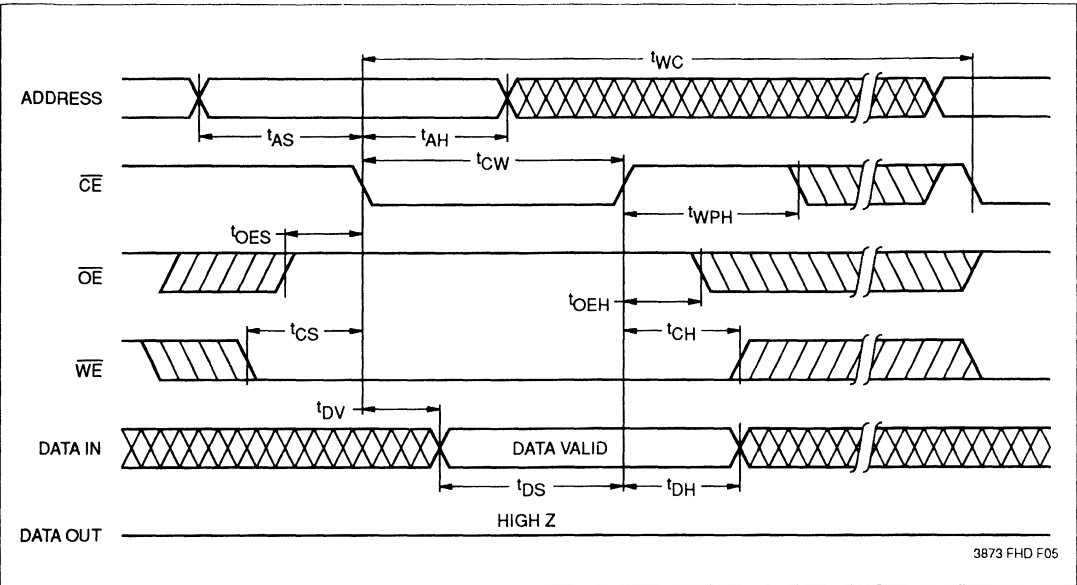
WE Controlled Write Cycle



**Note:** (4) Due to the inclusion of the decoder IC on board the module the  $\overline{WE}$  and  $\overline{CE}$  write controlled timings will vary. When utilizing the  $\overline{CE}$  controlled write operation all the hold timings must be extended by the worst case propagation delay of the decoder. For a  $\overline{WE}$  controlled write operation  $\overline{CE}$  must be a minimum 125 ns to accommodate the additional setup time required.

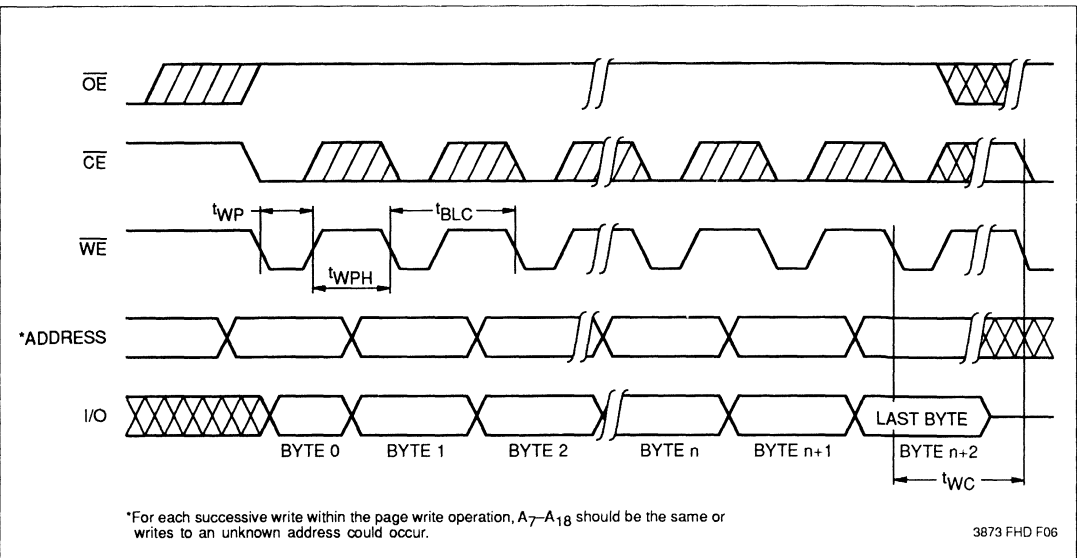
# **XM28C040**

## **$\overline{\text{CE}}$ Controlled Write Cycle**



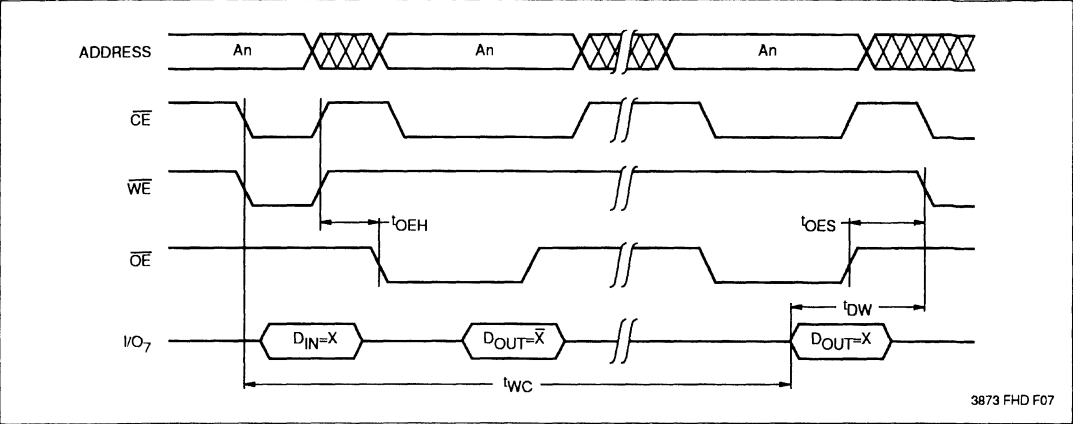
6

## **Page Write Cycle**

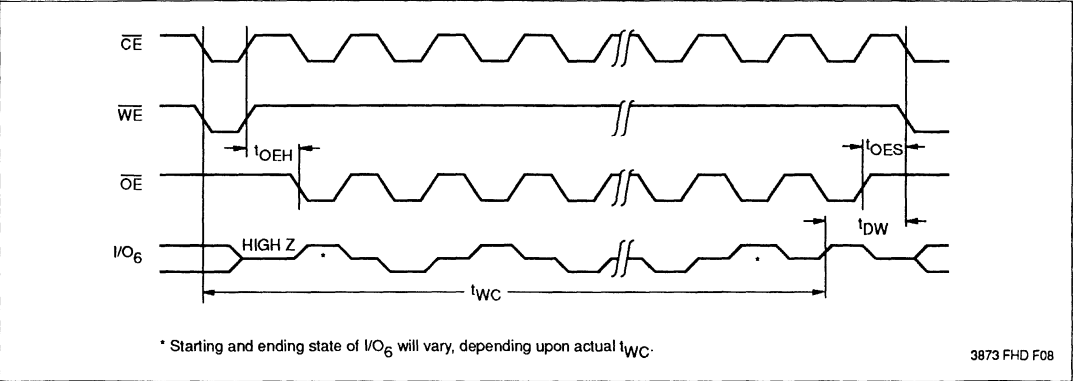


**XM28C040**

**DATA Polling Timing Diagram**



**Toggle Bit Timing Diagram**



**SYMBOL TABLE**

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

# XM28C040

## MultiPlane Architecture

The design of the XM28C040 has implemented a multiplane architecture. That is, there are four independent 128K x 8 memory spaces or planes, each selected by its own chip enable input via the on-board decoder chip. This architecture can be utilized in a number of ways.

## Separate Data and Program Memory Spaces

The multiplane concept allows the system to write to one plane of the module and still be able to read (continue executing code) from the module, utilizing any plane not performing a write operation.

This concept of separated data and program spaces can be expanded by providing a simple off-module circuit that will disable writes to predetermined portions of memory. A very basic version is shown in the Functional Diagram. Whenever A<sub>18</sub> is high, the WE input is forced high, write protecting one half the module. This half

would be reserved for read only program store while the other half would be available for read and write data store.

## Expanded Sequential Page Lengths

A standard system implementation would be decoding externally the module's chip enable and then wiring each address of the module to its corresponding address line in the system. This would effectively provide the system a memory organized as four separate memory planes with a sequential page address space of 256 bytes.

In an application such as data logging, the most efficient method of logging the data is in a sequential manner. If the data come in bursts that exceed 256 bytes in length a longer page might be desirable. By swapping address lines externally the effective page length can be expanded to 1024 bytes. Refer to the table below for a matrix illustrating the various page length options.

TABLE 1. ADDRESS TRANSLATION MATRIX

	Module Address Inputs				Page Size	Effective No. of Planes
	A <sub>0</sub> -A <sub>7</sub>	A <sub>8</sub> -A <sub>16</sub>	A <sub>17</sub>	A <sub>18</sub>		
System Address Lines	A0-A7	A8-A16	A17	A18	256	4
	A0-A7	A9-A17	A8	A18	512	2
	A0-A7	A10-A18	A8	A9	1024	1

Note: The user should be aware the overall I<sub>CC</sub> of the module will increase as more individual components on the module are activated.

**XM28C040**

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**NOTES**

## FEATURES

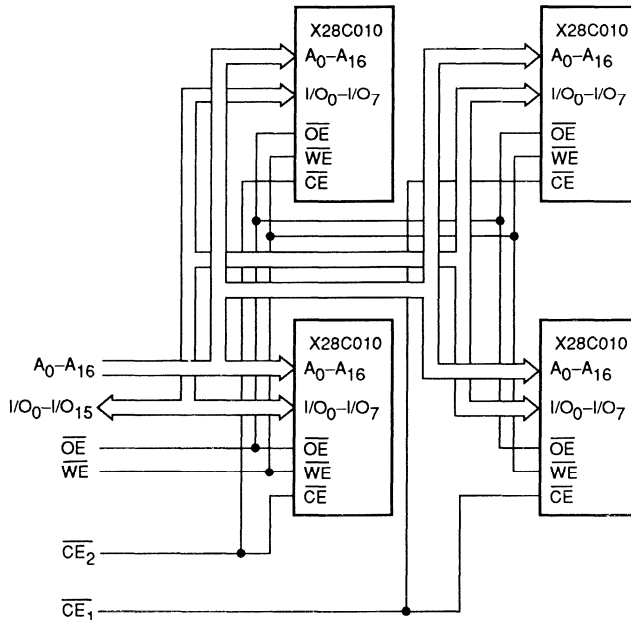
- High Density 4 Megabit (256K x 16) E<sup>2</sup>PROM Module
- Low Power CMOS technology
  - Active—Less than 100mA
  - Standby—Less than 2mA
- Access Time of 150ns
- Base memory Component: Xicor X28C010F
- Fast Write Cycle Times
- 256 Word Page
- Early end of write
  - DATA Polling
  - Toggle Bit Polling
- Software Data Protection
- User Accessible Redundant Rows
- Dual Plane™ Memory Architecture

## DESCRIPTION

The XM28C4096 is a high density 4Megabit E<sup>2</sup>PROM comprised of four X28C010 128K x 8 E<sup>2</sup>PROMs mounted on a FR-4 substrate. The XM28C4096 is configured 256K x 16 and features two separate Chip Enable inputs to select between two 128K x 16 banks of memory.

The two chip enable inputs provide the interface mechanism for user selection on the implementation of the memory: e.g. Dual plane, concurrent read while write; expanded page, external mapping providing a 512 word page.

## FUNCTIONAL DIAGRAM





# XM28C4096

## PIN DESCRIPTIONS

### Addresses (A<sub>0</sub>–A<sub>16</sub>)

The Address inputs select an 16-bit memory location during a read or write operation.

### Chip Enable 1 ( $\overline{\text{CE1}}$ ) and

### Chip Enable 2, ( $\overline{\text{CE2}}$ )

The XM28C4096 has two chip enable inputs.  $\overline{\text{CE1}}$  enables one device pair and  $\overline{\text{CE2}}$  enables the other device pair. These are active LOW inputs.

### Output Enable ( $\overline{\text{OE}}$ )

The output enable input is active LOW and when asserted turns on the output buffers.

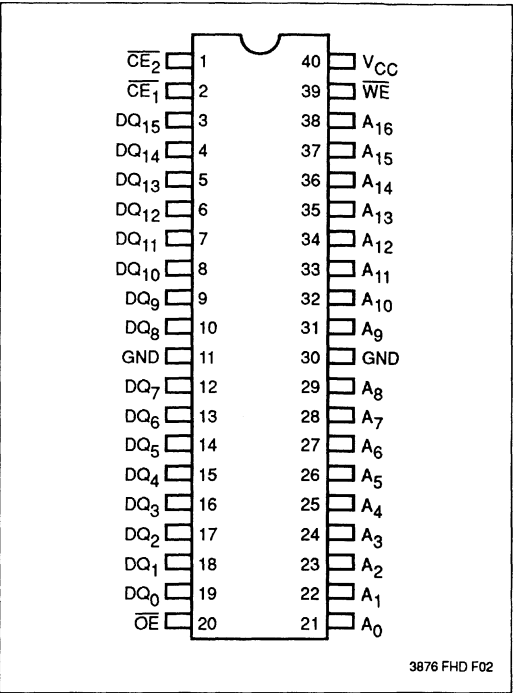
### Data In/Data Out (I/O<sub>0</sub>–I/O<sub>15</sub>)

Data is read from or written to the XM28C4096 through the I/O pins.

### Write Enable ( $\overline{\text{WE}}$ )

The write enable input controls the writing of data to the XM28C4096. Addresses are latched on the high to low transition of  $\overline{\text{WE}}$  and data in is latched on the low to high edge of  $\overline{\text{WE}}$ .

## PIN CONFIGURATION



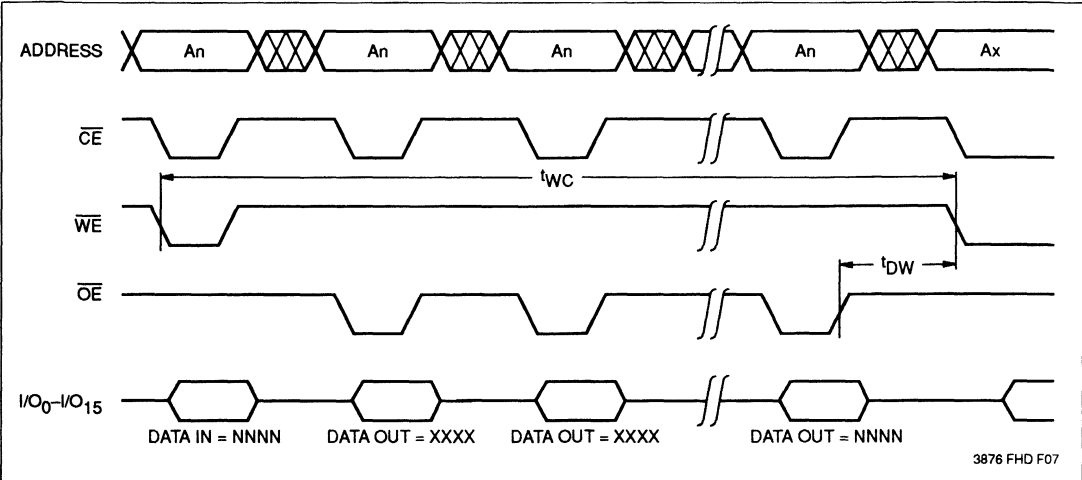
## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>16</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable

3876 PGM T01

# **XM28C4096**

## **Polling Operation Timing**



3876 FHD F07

## **DEVICE OPERATION**

### **Read**

Read operations are initiated when both  $\overline{OE}$  and  $\overline{CE}$  (either  $\overline{CE1}$  or  $\overline{CE2}$ , not both) are LOW. The XM28C4096 will output data from the memory location pointed to by the address inputs. The data bus will be in a high impedance state when either  $\overline{OE}$  or both  $\overline{CE}$  inputs are HIGH.

### **Write**

Write operations are initiated when both  $\overline{WE}$  and  $\overline{CE}$  (either  $\overline{CE1}$  or  $\overline{CE2}$ ) are LOW and  $\overline{OE}$  is HIGH. The XM28C4096 supports both a  $\overline{WE}$  and  $\overline{CE}$  controlled write operation. That is, the address is latched by the falling edge of either  $\overline{WE}$  or  $\overline{CE}$ , whichever occurs last. The data is latched by the rising edge of either  $\overline{WE}$  or  $\overline{CE}$ , whichever occurs first. A word write operation, once initiated will continue to completion, typically within 10ms.

## **Page Write Operation**

A page write operation provides for the host system a means for writing from two to two-hundred fifty-six words sequentially. A page write, no matter how many words are written, will take no longer than 10ms to complete.

## **Polling Operations**

E<sup>2</sup>PROM memories can be written quickly in the write page mode. However, once the data is latched into the memory, the internal write operation can take up to 10ms. The typical write cycle is somewhat less than 10ms and the host system can take advantage of the shorter write cycle time by polling the memory. Polling is performed by the host reading the last location written. When the read data compares true with the data written, the internal cycle is complete and the memory is ready for normal read or write operations to resume. Refer to the Polling Operation figure shown above.

# XM28C4096

## Software Data Protection

The memory components on the module support Software Data Protection (SPD). SPD, when enabled by the host system, will protect the memory contents from inadvertent write operations during power-up and power-down.

## Setting SPD

The host system must write a three word command sequence to the module, wait  $t_{WC}$  and the device will be protected. Because this module is composed of discrete memory components both memory pairs (CE1 and CE2) will have to be enabled separately. Once SPD is set, the memory will ignore all standard attempts to alter its contents. The host can still access the memory but

must first reissue the three word command sequence immediately followed by the word or page write operation. Refer to Table 1 for a detailed description of the sequence.

## Resetting SPD

In the event the user needs to reset SPD for testing they may issue a six word command sequence. After  $t_{WC}$  the memory will be returned to the standard operating mode. Refer to Table 2 for a detailed description of the operation.

The modules are shipped from the factory unprotected; that is, the module will be in the standard operating mode. If the user decides not to employ SPD, it is recommended they provide external protection circuitry.

TABLE 1. SOFTWARE DATA PROTECTION SEQUENCE

Step	Operation	Address	Data	Comments
1	Write	15555	AAAA	Only Addressing of same device pair (Chip enable is the same for all accesses) is allowed.
2	Write	0AAAA	5555	
3	Write	15555	A0A0	
4	Write	XXXXX	XXXX	Optional write operation(s) after opening access.

3876 PGM T02

*Note: Step 4 is optional. The system may exit the routine after step 3 and the device will enter a write cycle and set the nonvolatile SPD bit. This is a nonvolatile write*

*operation and will take a maximum 10ms to complete. If the system enters step 4, it may write from 1 to 256 words.*

TABLE 2. RESET SOFTWARE DATA PROTECTION SEQUENCE

Step	Operation	Address	Data	Comments
1	Write	15555	AAAA	Interruption of the sequence during any one of these steps and the device pair being accessed will remain protected
2	Write	0AAAA	5555	
3	Write	15555	8080	
4	Write	15555	AAAA	
5	Write	0AAAA	5555	
6	Write	15555	2020	After $t_{wc}$ , the device pair will return to the unprotected state.

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# XM28C4096

## Dual Plane Memory

The design of the XM28C4096 has implemented a dual plane memory architecture. That is, there are two independent 128K x 16 memory spaces, each selected by its own Chip Enable input. This architecture can be utilized in numerous ways.

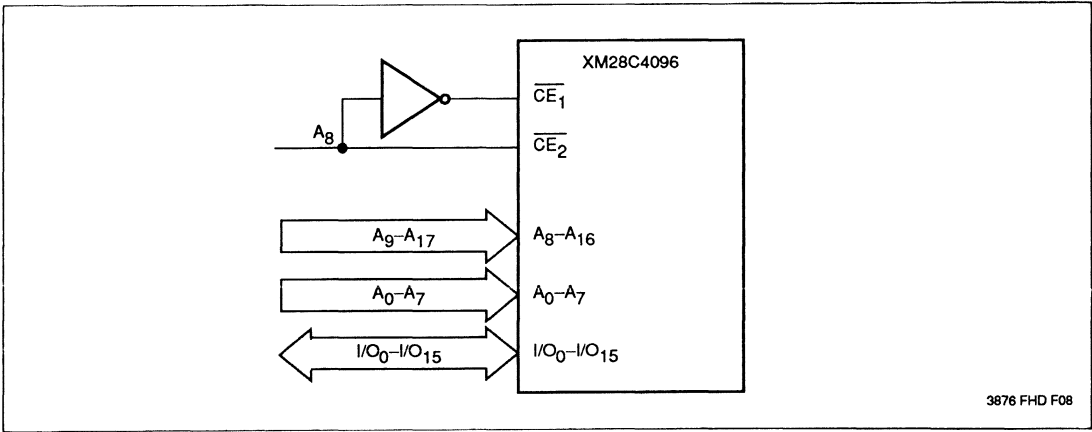
The standard implementation would externally decode  $\overline{CE1}$  and  $\overline{CE2}$  from the host addresses and place both pair of memories in contiguous 128K memory spaces.

A second alternative might be to separate the spaces, dedicating one 128K block to program storage require-

ments. This would be a space never written during normal system operation. The other 128K block could then be employed for data logging or system monitoring data storage. In an application such as this, the dual plane architecture also provides the ability to write to the data memory and continue to operate (read instructions) from the program memory.

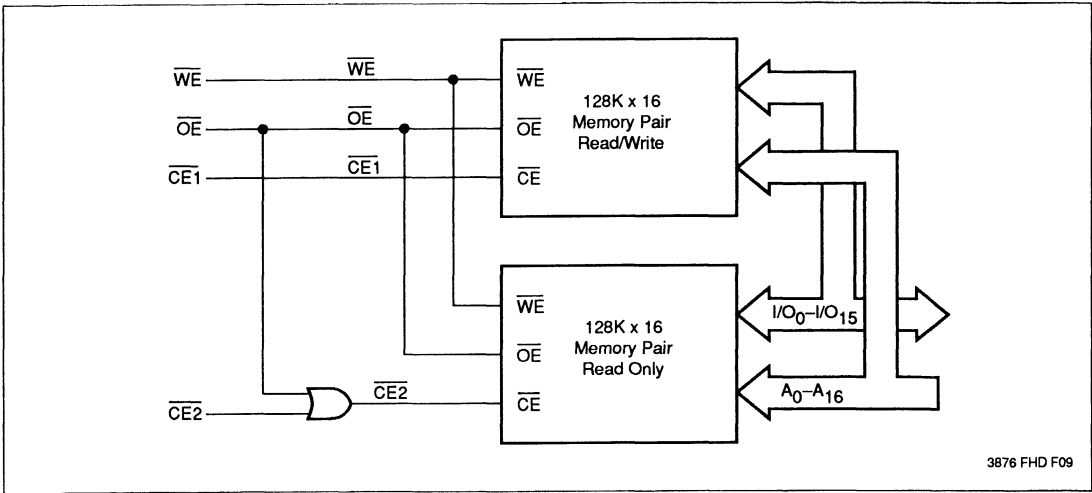
A third alternative might be implemented where an extremely fast rewrite of the module is required. By assigning the system's A8 as the  $\overline{CE1}/\overline{CE2}$  chip enable, the page length can effectively be doubled from 256 words to 512 words.

## 512 Word Page Implementation



6

## Separated Program and Data Memory



# XM28C4096

### ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....-10°C to +85°C  
Storage Temperature .....-55°C to +125°C  
Terminal Voltage with  
    Respect to Ground .....-0.1V to +7.0V  
D.C. Output Current .....5 mA

### \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the Module components. This is a stress rating only and the functional operation of the module at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### D.C. OPERATING CHARACTERISTICS

XM28C4096 T<sub>A</sub> = 0°C to +75°C, V<sub>CC</sub> = +5V ± 10%, Unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Current (Active) Mode 1		100	mA	$\overline{CE}$ (1 or 2) = $\overline{OE}$ = V <sub>IL</sub> , $\overline{WE}$ = V <sub>IH</sub> , All I/O's = Open, 2 Devices Active, 2 Devices Inactive
I <sub>CC</sub>	V <sub>CC</sub> Current (Active) Mode 2		200	mA	$\overline{CE}$ (1 or 2) = $\overline{OE}$ = $\overline{WE}$ = V <sub>IH</sub> , All I/Os = Open, 2 Devices Active Writing (twc), 2 Devices Active Read
I <sub>CC</sub>	V <sub>CC</sub> Current (Active) Mode 3		200	mA	$\overline{CE}$ (1 or 2) = $\overline{OE}$ = $\overline{WE}$ = V <sub>IH</sub> , All I/Os = Open, 4 Devices Active Writing (twc)
I <sub>SB</sub>	V <sub>CC</sub> Current (Standby)		2	mA	$\overline{CE1}$ and $\overline{CE2}$ = V <sub>CC</sub> -0.3V, All I/O's = Open, All Other Inputs = Don't Care
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , $\overline{CE}$ = V <sub>IH</sub>
V <sub>IL</sub> <sup>(1)</sup>	Input Low Voltage	-1.0	0.8	V	
V <sub>IH</sub> <sup>(1)</sup>	Input High Voltage	2.0	V <sub>CC</sub> + 1.0	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2.1mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -400mA

3876 PGM T07

### POWER-UP TIMING

Symbol	Parameter	Max.	Units
t <sub>PUR</sub> <sup>(2)</sup>	Power-up to Read Valid	100	μs
t <sub>PUW</sub> <sup>(2)</sup>	Power-up to Write Valid	5	ms

3876 PGM T08

CAPACITANCE T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 5V

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> <sup>(2)</sup>	Input/Output Capacitance	40	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> <sup>(2)</sup>	Input Capacitance	24	pF	V <sub>IN</sub> = 0V

3876 PGM T09

Note: (1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.

# XM28C4096

### A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Input and Output Timing Reference Levels	1.5V
Equivalent Output Load	1 TTL Gate and $C_L = 100\text{pF}$

## OPERATION SELECTION

CE1	CE2	OE	WE	Operation	I/O
L	H	L	H	Read Bank1	DOUT
L	H	H	L	Write Bank 1	DIN
H	L	L	H	Read Bank2	DOUT
H	L	H	L	Write Bank2	DIN
H	H	X	X	Standby/Write Inhibit	–
X	X	L	X	Write Inhibit	–
X	X	X	H	Write Inhibit	–

3876 PGM T11

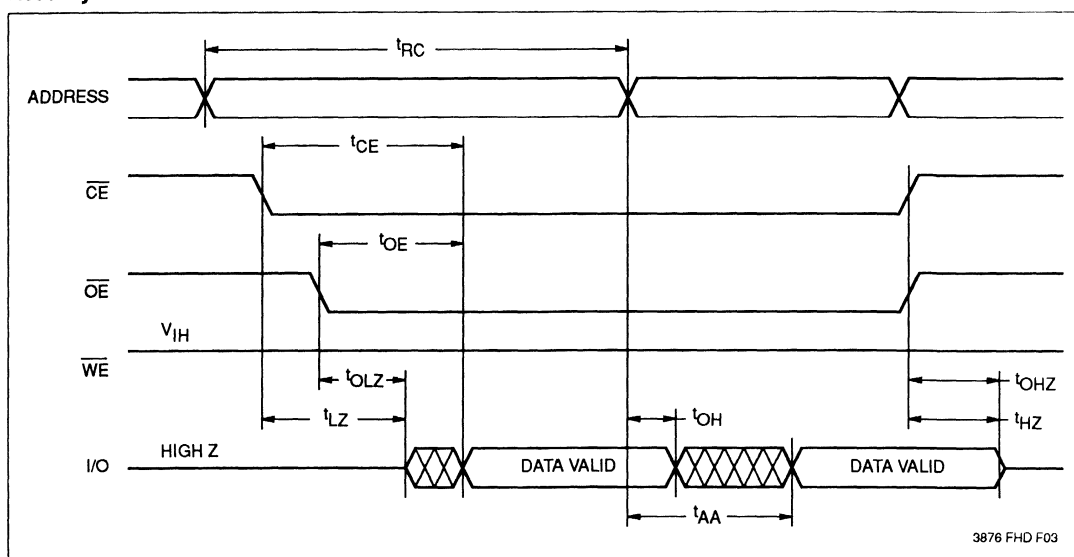
**A.C. CHARACTERISTICS**  $T_A = 0^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , Unless otherwise specified

### Read Cycle Limits

Symbol	Parameter	XM28C4096-15		XM28C4096-20		XM28C4096-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	150		200		250		ns
t <sub>CE</sub>	CE Access Time		150		200		250	ns
t <sub>AA</sub>	Address Access Time		150		200		250	ns
t <sub>OE</sub>	OE Access Time		50		50		50	ns
t <sub>LZ</sub>	CE LOW to Active Output	0		0		0		ns
t <sub>OLZ</sub>	CE LOW to Active Output	0		0		0		ns
t <sub>HZ</sub>	CE HIGH to High Z Output		50		50		50	ns
t <sub>OHZ</sub>	OE HIGH to High Z Output		50		50		50	ns
t <sub>OH</sub>	Output Hold	0		0		0		ns

3876 PGM T12

### Read Cycle



3876 FHD F03

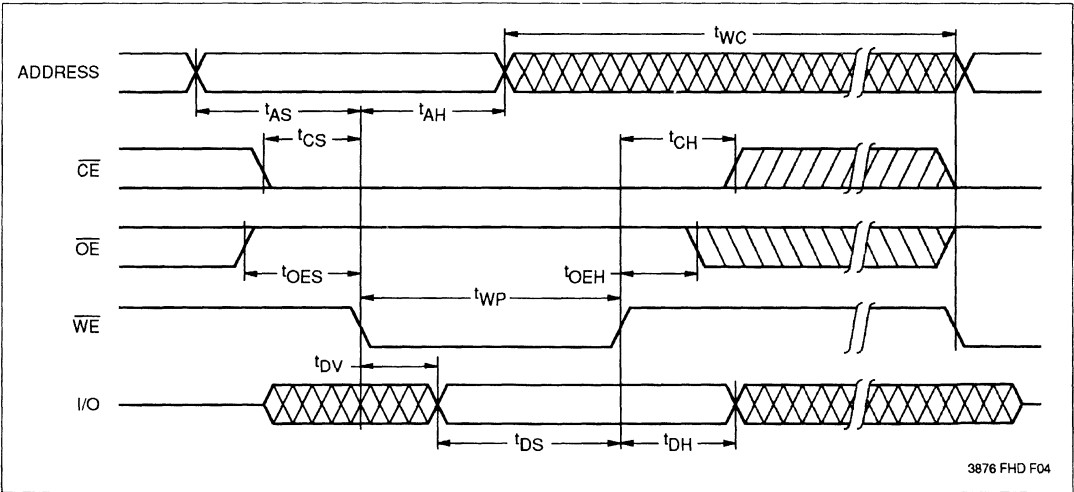
**XM28C4096**

**Write Cycle Limits**

Symbol	Parameter	Min.	Max.	Units
$t_{WC}$	Write Cycle Time		10	ms
$t_{AS}$	Address Setup Time	0		ns
$t_{AH}$	Address Hold Time	50		ns
$t_{CS}$	Write Setup Time	0		ns
$t_{CH}$	Write Hold Time	0		ns
$t_{CW}$	Chip Enable Pulse Width	100		ns
$t_{OES}$	OE High Setup Time	10		ns
$t_{OEH}$	OE High Hold Time	10		ns
$t_{WP}$	WE Pulse Width	100		ns
$t_{WPH}$	WE High Recovery	100		ns
$t_{DV}$	Data Valid		1	$\mu$ s
$t_{DS}$	Data Setup	50		ns
$t_{DH}$	Data Hold	10		ns
$t_{DW}$	Delay to Next Write	1		$\mu$ s
$t_{BLC}$	Byte Load Cycle	0.20	200	$\mu$ s

3876 PGM T13

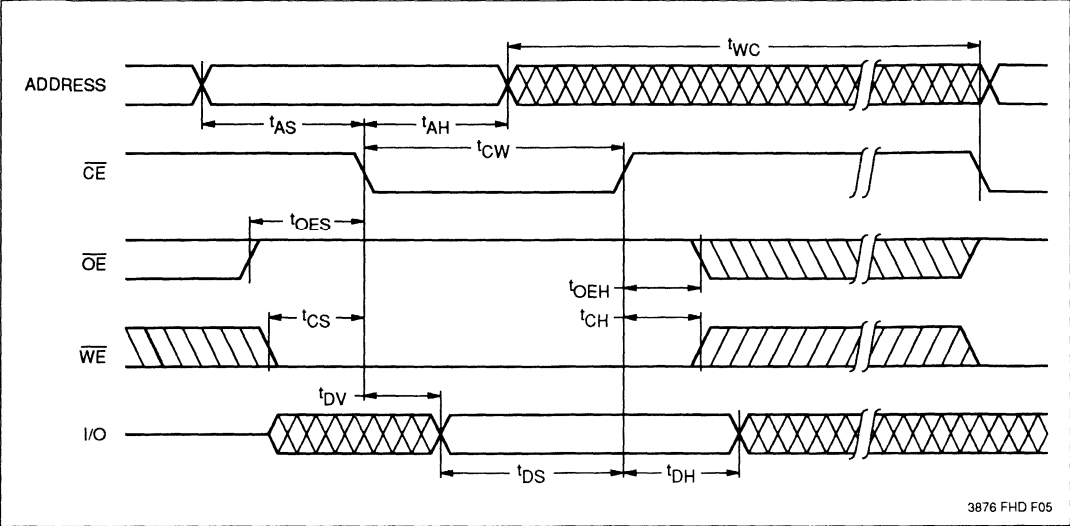
**$\overline{WE}$  Controlled Write Cycle**



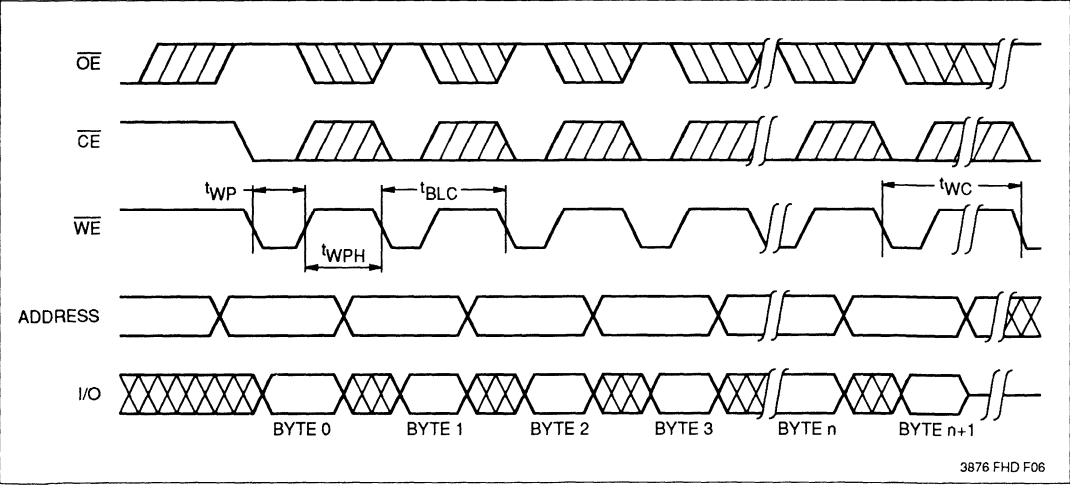
3876 FHD F04

**XM28C4096**

**$\overline{\text{CE}}$  Controlled Write Cycle**



**Page Write Cycle**





**XM28C4096**

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**NOTES**



Advance Information

8 Megabit Module

**XM28C080S**

1 Meg x 8

**5 Volt, Byte Alterable E<sup>2</sup>PROM SIP Module**

## FEATURES

- High Density 8 Megabit SIP Module
- Industrial Standard 36 PIN SRAM SIP Pinout
- Low Power CMOS Technology
  - Active – Less Than 60mA
  - Standby – Less Than 4mA
- Fully Decoded Addresses
- Access Time of 180ns
- Fast Write Cycle Times
- Standard 256 Byte Page
  - User Configurable to 512, 1024 or 2048 Bytes
- Software Data Protection
- MultiPlane™ Memory Architecture
  - Concurrent Read Write™

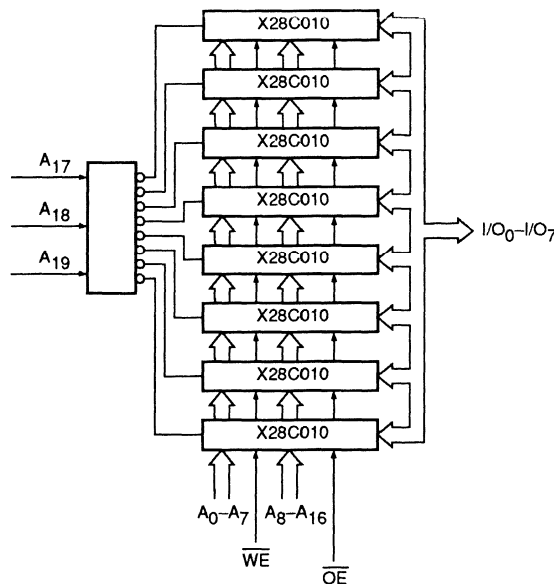
## DESCRIPTION

The XM28C080S is a high density 8 Megabit E<sup>2</sup>PROM module comprised of eight X28C010 128K x 8 E<sup>2</sup>PROMs mounted on a FR-4 substrate. The XM28C080S is configured 1 Meg x 8 and is fully decoded. The module is a 36 Pin SIP conforming to the industry standard SRAM pinouts.

The individual memory components are Xicor's X28C010 1 Megabit E<sup>2</sup>PROMs, featuring the highly reliable Direct Write™ memory cell. All components are fully tested prior to assembly and then the completed module is 100% electrically tested.

The MultiPlane™ memory architecture allows reading of the module while a write operation is currently underway.

## FUNCTIONAL DIAGRAM



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3877 FHD F08

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Characteristics subject to change without notice

3877-1

# XM28C080S

## PIN DESCRIPTIONS

### Address ( $A_0$ – $A_{19}$ )

The address inputs selects 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{CE}$ )

A LOW on the  $\overline{CE}$  input enables read or write operations.

### Output Enable ( $\overline{OE}$ )

The output enable input is active LOW and when asserted turns on the output buffers of the selected memory component.

### Write Enable ( $\overline{WE}$ )

The write enable input controls the writing of data to the XM28C080S. Addresses are latched on the high to low transition of  $\overline{WE}$  and data is latched on the low to high edge of  $\overline{WE}$ .

### Input/Output ( $I/O_0$ – $I/O_7$ )

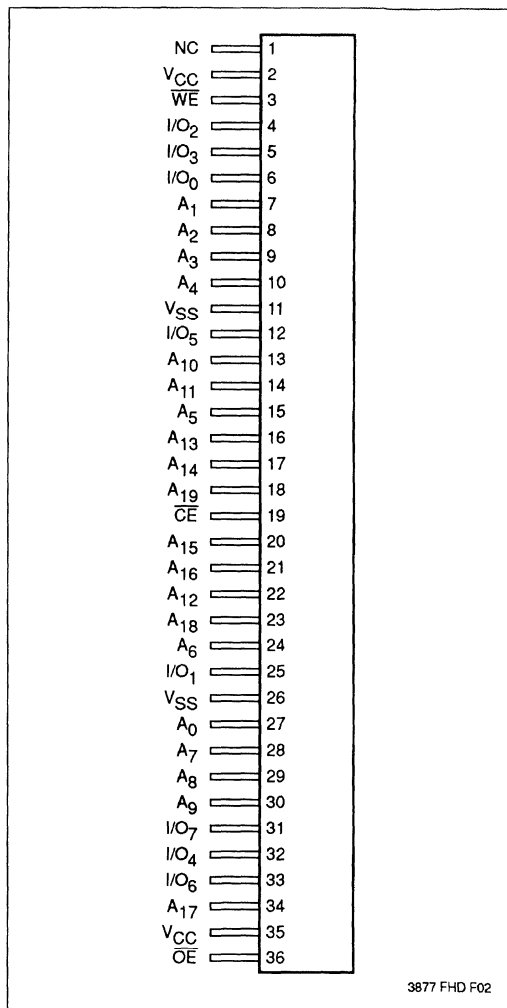
Data is read from or written to the XM28C080S through the I/O pins.

## PIN NAMES

Symbol	Description
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$I/O_0$ – $I/O_7$	Data Input/Output
$A_0$ – $A_{19}$	Addresses Inputs
$V_{CC}$	+5V
$V_{SS}$	Ground

3877 PGM T01

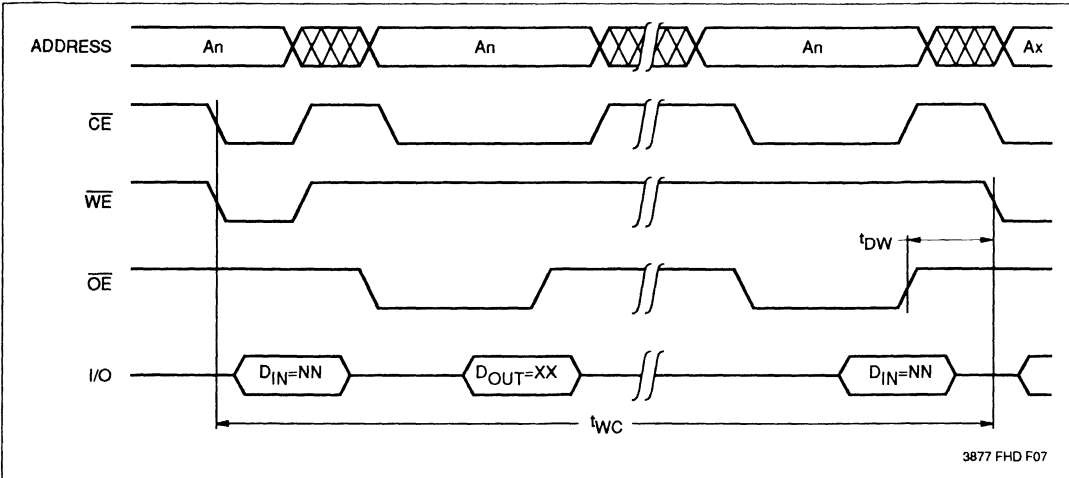
## PIN CONFIGURATION



3877 FHD F02

# XM28C080S

## Polling Operation Timing



## DEVICE OPERATION

### Read

Read operations are initiated when both  $\overline{OE}$  and  $\overline{CE}$  are LOW. Data will be output from the memory location pointed to by the address inputs. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  inputs are HIGH.

### Write

Write operations are initiated when both  $\overline{WE}$  and  $\overline{CE}$  are LOW and  $\overline{OE}$  is HIGH. The module supports both a  $\overline{WE}$  and a  $\overline{CE}$  controlled write operation. That is, the address latched by the falling edge of either  $\overline{WE}$  or  $\overline{CE}$ , whichever occurs last. The data is latched by the rising edge of either  $\overline{WE}$  or  $\overline{CE}$ , whichever occurs first. A write operation, once initiated, will continue to completion within 10ms.

## Page Write Operation

A page write operation provides for the system a means for writing from two to two-hundred fifty-six bytes sequentially. A page write, no matter how many bytes written, will take no longer than 10ms to complete.

## Polling Operations

E<sup>2</sup>PROM memories can be written quickly in the write page mode. However, once the data is latched into the memory, the internal write operation can take up to 10ms. The typical write cycle is somewhat less than 10ms and the host system can take advantage of the shorter write cycle time by polling the memory. Polling is performed by the host reading the *last* location written. When the read data compares true with the data written, the internal cycle is complete and the memory is ready for normal read or write operations to resume. Refer to the timing diagram above.

# XM28C080S

## Software Data Protection (SDP)

The memory components on the module support SDP. SDP, when enabled by the host system, will protect the memory contents from inadvertent writes during the power-up and power-down cycles.

## Setting SDP

The host system must write a three byte command sequence to the module **for each memory component to be protected**. Once SDP is set, the memory will ignore all standard attempts to alter its contents. The host can still write the memory but must first reissue the three byte command sequence immediately followed by the byte or page write operation.

## Resetting SDP

In the event the user needs to reset SDP for testing, they may issue a six byte command sequence. After  $t_{WC}$  the memory component will be returned to the standard operating mode. **This operation must be repeated for each component being reset.**

The modules are shipped from Xicor with SDP reset; that is, the module will be in the standard operating mode. If the user decides not to employ the SDP, it is recommended they provide external inadvertent write protection circuitry.

TABLE 1. SOFTWARE DATA PROTECTION SEQUENCE

Step	Operation	A <sub>0</sub> –A <sub>16</sub>	Data Pattern	Comments
1	Write	15555	AA	A <sub>17</sub> , A <sub>18</sub> , and A <sub>19</sub> must be the same for the entire command sequence and any subsequent write operation.
2	Write	0AAAA	55	
3	Write	15555	A0	
4	Write	XXXXX	XX	Optional write operation (byte or page) after opening access.

3877 PGM T32

**Note:** Step 4 is optional. The system may exit the routine after step 3 and the device will enter a write cycle and set the nonvolatile SDP bit. This is a nonvolatile write operation and will take a maximum 10ms to com-

plete. If the system enters step 4 (within  $t_{BLC}$ ) it may write from 1 to 256 bytes to the device addressed by the command sequence.

TABLE 2. RESET SOFTWARE DATA PROTECTION SEQUENCE

Step	Operation	A <sub>0</sub> –A <sub>16</sub>	Data Pattern	Comments
1	Write	15555	AA	A <sub>17</sub> , A <sub>18</sub> , and A <sub>19</sub> must be the same for the entire command sequence.
2	Write	0AAAA	55	
3	Write	15555	80	
4	Write	15555	AA	
5	Write	0AAAA	55	
6	Write	15555	20	After $t_{WC}$ , the selected component will return to the unprotected state.

3877 PGM T03

# XM28C080S

## MultiPlane Architecture

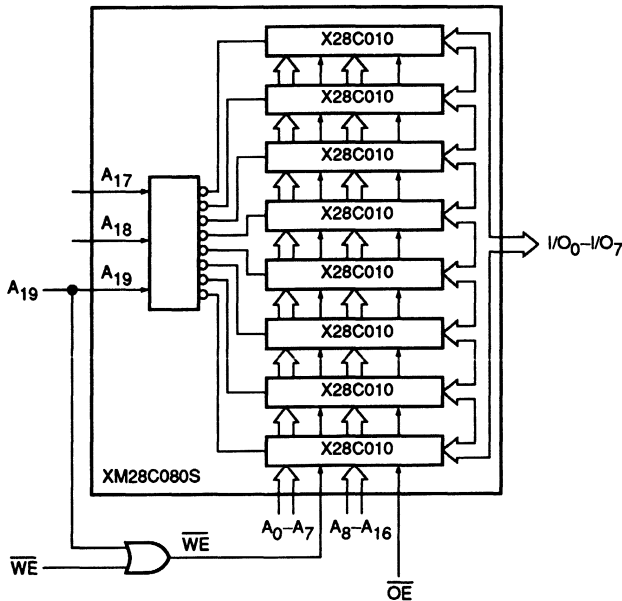
The design of the XM28C080S has implemented a multiplane architecture. That is, there are eight independent 128K x 8 memory spaces or planes, each selected by its own chip enable input via the on-board decoder chip. This architecture can be utilized in a number of ways.

## Separate Data and Program Memory Spaces

The multiplane concept allows the system to write to one plane of the module and still be able to read (continue

executing code) from the module, utilizing any plane not performing a write operation.

This concept of separated data and program spaces can be expanded by providing a simple off-module circuit that will disable writes to predetermined portions of memory. A very basic version is shown in the Functional Diagram. Whenever A<sub>19</sub> is high, the WE input is forced high, write protecting one half the module. This half would be reserved for read only program store while the other half would be available for read and write data store.



# XM28C080S

## Expanded Sequential Page Lengths

A standard system implementation would be decoding externally the module's chip enable and then wiring each address of the module to its corresponding address line in the system. This would effectively provide the system a memory organized as eight separate memory planes with a sequential page address space of 256 bytes.

In an application such as data logging, the most efficient method of logging the data is in a sequential manner. If the data come in bursts that exceed 256 bytes in length a longer page might be desirable. By swapping address lines externally the effective page length can be expanded to 2048 bytes. Refer to Table 3 for matrix illustrating the various page length options.

TABLE 3. ADDRESS TRANSLATION MATRIX

	Module Address Inputs					Page Size	Effective No. of Planes
	A <sub>0</sub> –A <sub>7</sub>	A <sub>8</sub> –A <sub>16</sub>	A <sub>17</sub>	A <sub>18</sub>	A <sub>19</sub>		
System Address Lines	A <sub>0</sub> –A <sub>7</sub>	A <sub>8</sub> –A <sub>16</sub>	A <sub>17</sub>	A <sub>18</sub>	A <sub>19</sub>	256	8
	A <sub>0</sub> –A <sub>7</sub>	A <sub>9</sub> –A <sub>17</sub>	A <sub>8</sub>	A <sub>18</sub>	A <sub>19</sub>	512	4
	A <sub>0</sub> –A <sub>7</sub>	A <sub>10</sub> –A <sub>18</sub>	A <sub>8</sub>	A <sub>9</sub>	A <sub>19</sub>	1024	2
	A <sub>0</sub> –A <sub>7</sub>	A <sub>11</sub> –A <sub>19</sub>	A <sub>8</sub>	A <sub>9</sub>	A <sub>10</sub>	2048	1

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**Note:** The user should be aware the overall I<sub>CC</sub> of the module will increase as more individual components on

the module are activated. Refer to I<sub>CC</sub> Active, MultiMode on Page 2.

**XM28C080S**

**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias .....	−10°C to +85°C
Storage Temperature .....	−55°C to +125°C
Voltage on any Pin with Respect to Ground .....	−0.5V to +6.0V
D.C. Output Current .....	5 mA

**\*COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

Temperature	Min.	Max.	Supply Voltage	Limits
Commercial	0°C	70°C	XM28C080S	5V ± 10%

**D.C. OPERATING CHARACTERISTICS** (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Current (Active)		60	mA	$\overline{CE} = \overline{OE} = V_{IL}$ , $\overline{WE} = V_{IH}$ , All I/Os = Open, one memory active, all other memories on standby
I <sub>CC</sub>	V <sub>CC</sub> Current (Active) MultiMode		55 + (50 x n)	mA	$\overline{CE} = \overline{OE} = V_{IL}$ , $\overline{WE} = V_{IH}$ , All I/Os = Open, n memories active (either being read or in write cycle), all other memories standby
I <sub>SB</sub>	V <sub>CC</sub> Current (Standby)		5	mA	$\overline{CE} = V_{CC} - 0.3V$ , All I/Os = Open, All Other Inputs = Don't Care
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = GND to V <sub>CC</sub> , $\overline{CE} = V_{IH}$
V <sub>IL</sub>	Input Low Voltage		0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0		V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2.1mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = −400mA

**POWER-UP TIMING**

Symbol	Parameter	Max.	Units
t <sub>PUR</sub>	Power-up to Read Delay	100	μs
t <sub>PW</sub>	Power-up to Write Delay	5	ms

**CAPACITANCE** T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 5V

Symbol	Parameter	Max.	Units	Test Conditions
C <sub>I/O</sub> (1)	Input/Output Capacitance	80	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (1)	Input Capacitance	48	pF	V <sub>IN</sub> = 0V

**Note:** (1) These parameters are periodically sampled and not 100% tested.



**XM28C080S**

**A.C. CONDITIONS OF TEST**

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Levels	1.5V

3877 PGM T10

**MODE SELECTION**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D <sub>OUT</sub>	Active
L	H	L	Write	D <sub>IN</sub>	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3877 PGM T11

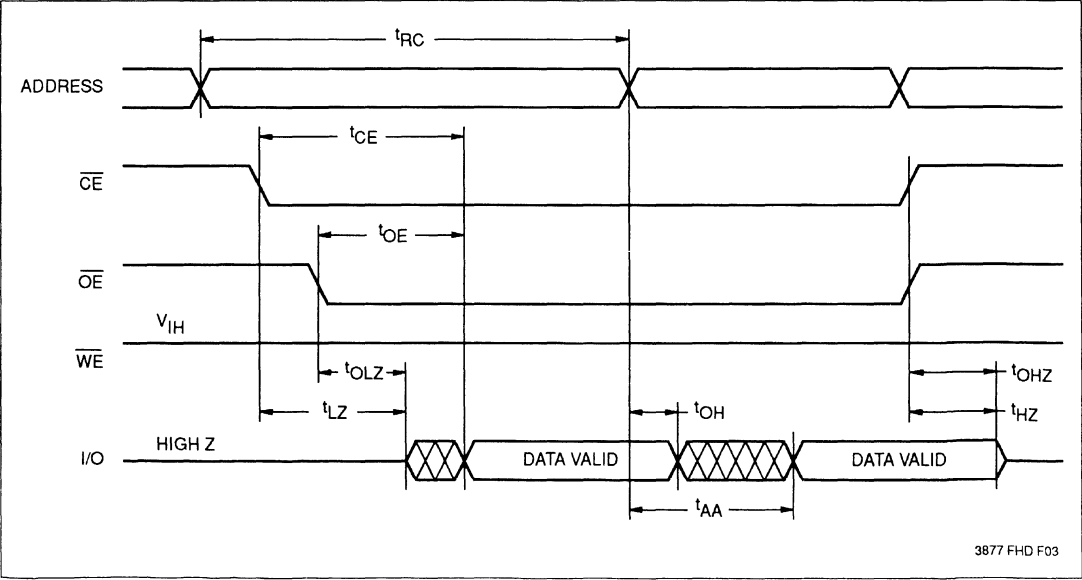
**A.C. CHARACTERISTICS** (Over the recommended operating conditions unless otherwise specified.)

**Read Cycle Limits**

Symbol	Parameter	XM28C080S-18		XM28C080S-25		Units
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	180		250		ns
t <sub>CE</sub>	$\overline{CE}$ Access Time		180		250	ns
t <sub>AA</sub>	Address Access Time		180		250	ns
t <sub>OE</sub>	$\overline{OE}$ Access Time		65		65	ns
t <sub>LZ</sub>	$\overline{CE}$ LOW to Active Output	0		0		ns
t <sub>OLZ</sub>	$\overline{OE}$ LOW to Active Output	0		0		ns
t <sub>HZ</sub>	$\overline{CE}$ HIGH to High Z Delay		65		65	ns
t <sub>OHZ</sub>	$\overline{OE}$ HIGH to High Z Delay		65		65	ns
t <sub>OH</sub>	Output Hold	0		0		ns

3877 PGM T12

**Figure Title**



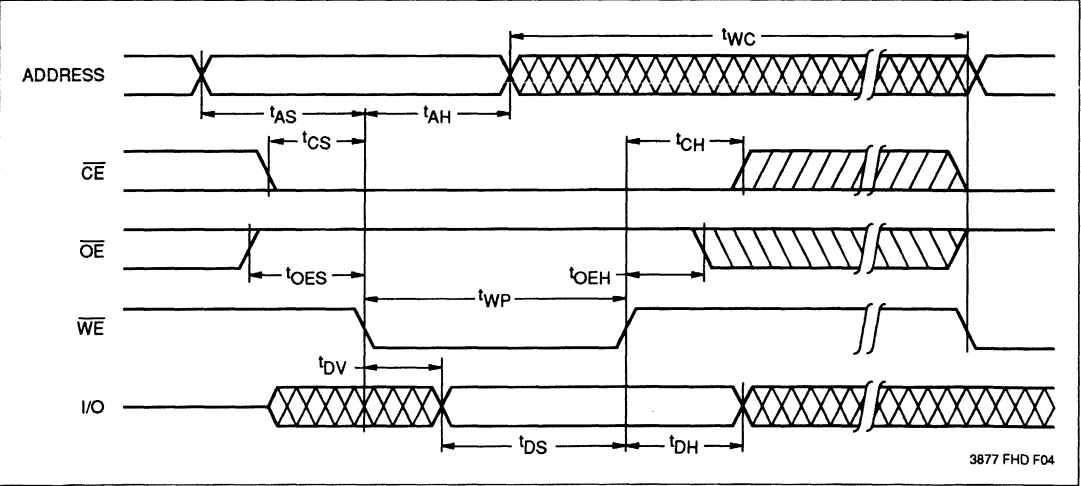
**XM28C080S**

**Write Cycle Limits**

Symbol	Parameter	Min.	Max.	Units
t <sub>WC</sub>	Write Cycle Time		10	ms
t <sub>AS</sub>	Address Setup Time	0		ns
t <sub>AH</sub>	Address Hold Time	50		ns
t <sub>CS</sub>	Write Setup Time	15		ns
t <sub>CH</sub>	Write Hold Time	0		ns
t <sub>CW</sub>	Chip Enable Pulse Width	100		ns
t <sub>OES</sub>	OE High Setup Time	10		ns
t <sub>OEH</sub>	OE High Hold Time	10		ns
t <sub>WP</sub>	WE Pulse Width	100		ns
t <sub>WPH</sub>	WE High Recovery	100		ns
t <sub>DV</sub>	Data Valid		1	μs
t <sub>DS</sub>	Data Setup	50		ns
t <sub>DH</sub>	Data Hold	10		ns
t <sub>DW</sub>	Delay to Next Write	1		μs
t <sub>BLC</sub>	Byte Load Cycle	0.20	200	μs

3877 PGM T13

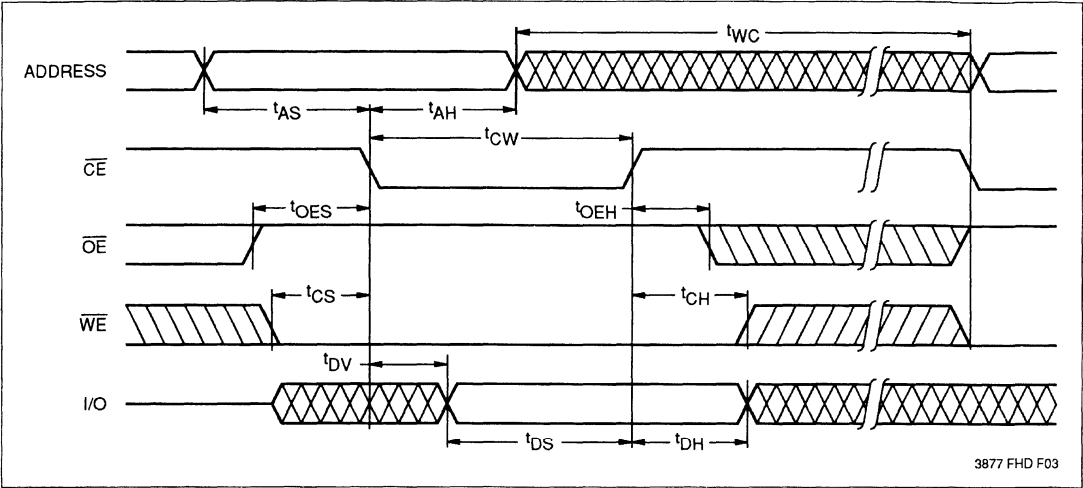
**WE Controlled Write Cycle**



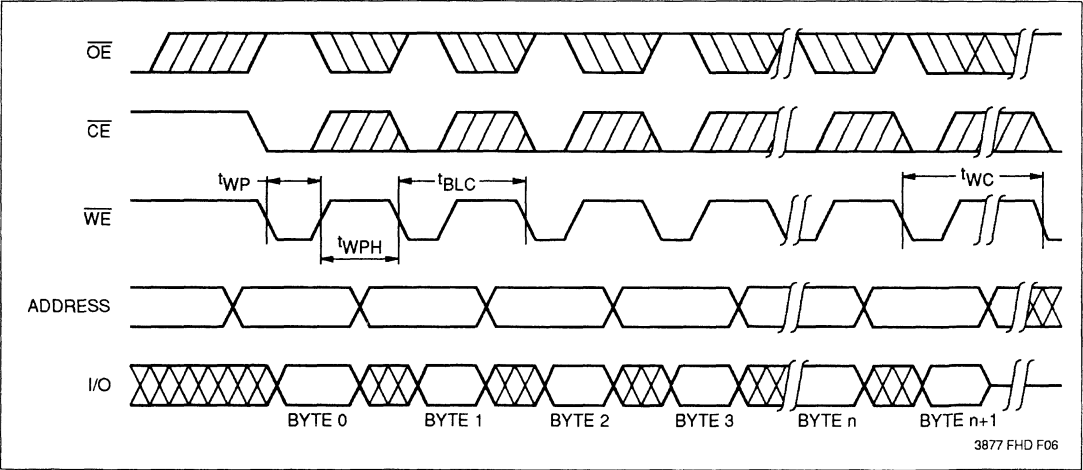
3877 FHD F04

# XM28C080S

## $\overline{\text{CE}}$ Controlled Write Cycle








## Page Write Cycle



**XM28C080S**

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**SYMBOL TABLE**

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**XM28C080S**

---

**NOTES**



64K

XM20C64

8K x 8

## High Speed AUTOSTORE™ NOVRAM

## FEATURES

- High Speed:  $t_{AA} = 55$  ns
- NO! Batteries!!
- Low Power CMOS
- AUTOSTORE™ NOVRAM
  - Automatically Stores RAM data to E<sup>2</sup>PROM upon Power-fall Detection
- Open Drain AUTOSTORE Output Pin
  - Provides Interrupt or Status Information
  - Linkable to System Reset Circuitry
- Auto Recall
  - Automatically Recalls E<sup>2</sup>PROM Data During Power-on
- Fully Decoded Module
- Full Military Temperature Range
  - $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- High Reliability
  - Endurance: 1,00,000 Store Cycles
  - Data Retention: 100 Years
- ESD Protection
  - $\geq 2\text{KV}$  All Pins

## DESCRIPTION

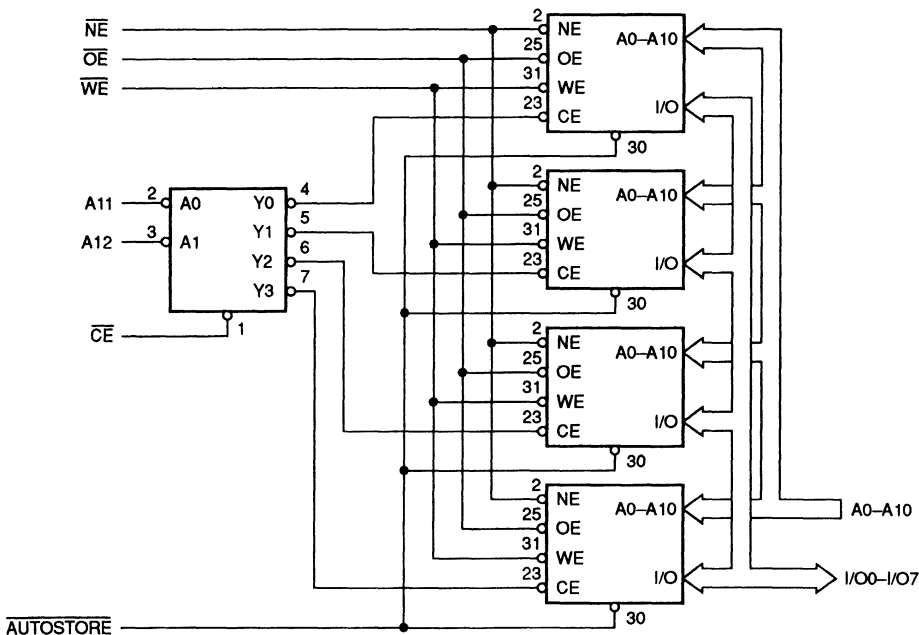
The XM20C64 is a high speed nonvolatile RAM Module. It is comprised of four Xicor X20C16 high speed NOVRAMs, a high speed "ACT" decoder and decoupling capacitors mounted on a FR-4 substrate. The XM20C64 is configured 8K x 8 and is fully decoded. The module is a 28-lead DIP conforming to the industry standard pinout for SRAMs. All the memory components and decoder are fully compliant with MIL-STD-883.

The XM20C64 fully supports the AUTOSTORE feature, providing hands-off automatic storing of RAM data into E<sup>2</sup>PROM when  $V_{CC}$  falls below the AUTOSTORE threshold.

The XM20C64 is a highly reliable memory component, supporting unlimited writes to RAM, a minimum 1,000,000 store cycles and a minimum 100 year data retention.

6

## FUNCTIONAL DIAGRAM



AUTOSTORE™ NOVRAM is a trademark of Xicor, Inc.

3874 FHD F01

# XM20C64

## PIN DESCRIPTIONS

### Addresses ( $A_0$ - $A_{12}$ )

The address inputs select an 8-bit memory location during read and write operations.

### Chip Enable ( $\overline{CE}$ )

The chip enable input must be LOW to enable all read, write and user requested nonvolatile operations.

### Output Enable ( $\overline{OE}$ )

During normal RAM operations  $\overline{OE}$  controls the data output buffers. If a hardware nonvolatile operation is selected ( $\overline{NE} = \overline{CE} = \text{LOW}$ ) and  $\overline{OE}$  strobes LOW a recall operation will be initiated.

$\overline{OE}$  LOW will always disable a STORE operation regardless of the state of  $\overline{NE}$ ,  $\overline{WE}$ , and  $\overline{CE}$  so long as the internal transfer has not commenced.

### Write Enable ( $\overline{WE}$ )

During normal RAM operations  $\overline{WE} = \overline{CE} = \text{LOW}$  will cause data to be written to the RAM address pointed to by the  $A_0$ - $A_{12}$  inputs.

### Nonvolatile Enable ( $\overline{NE}$ )

The nonvolatile input controls the transfer of data from the E<sup>2</sup>PROM array to the RAM array, when strobed LOW in conjunction with  $\overline{CE} = \overline{OE} = \text{LOW}$ .

### Data In/Data Out ( $I/O_0$ - $I/O_7$ )

Data is written to or read from the X20C64 through the I/O pins. The I/O pins are placed in the high impedance state when either  $\overline{CE}$  or  $\overline{OE}$  is HIGH or when  $\overline{NE}$  is LOW.

### AUTOSTORE Output ( $\overline{AS}$ )

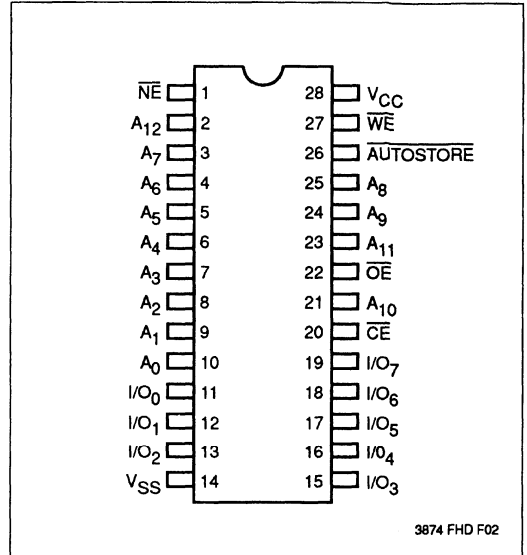
$\overline{AS}$  is an open drain output. When it is asserted (driving LOW) it indicates  $V_{CC}$  has fallen below the AUTOSTORE threshold and an internal store operation has been initiated. Because AS is an open drain output it may be wire-ORed with multiple open drain outputs and used as an interrupt input or as an input to a power on reset circuit.

## DEVICE OPERATION

RAM operations are identical to those of a standard SRAM. When  $\overline{OE}$  and  $\overline{CE}$  are asserted data is presented at the I/Os from the address location pointed to by the  $A_0$ - $A_{12}$  inputs.

RAM write operations are initiated and the address input is latched by the HIGH to LOW transition of  $\overline{CE}$  or  $\overline{WE}$ ,

## PIN CONFIGURATION



whichever occurs last. Data are latched on the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first.

An array recall, E<sup>2</sup>PROM data transferred to RAM, is initiated whenever  $\overline{OE} = \overline{NE} = \overline{CE} = \text{LOW}$ . A recall is also performed automatically upon power up.

## Command Sequence Operations

The X20C64 employs a version of the industry standard Software Data Protection (SDP). The end user can select various options for transferring data from RAM into the E<sup>2</sup>PROM array.

All command sequences are comprised of three specific data/address write operations performed with  $\overline{NE}$  LOW. A Store operation can be directly selected by issuing an Immediate Store command. The user may also enable and disable the AUTOSTORE function through the software data protection sequence. Refer to Table 1 below for a complete description of the command sequence.

## Operational Notes

The X20C64 should be viewed as a subsystem when writing software for the various store operations. The module contains four discrete components each needing to be set to the required state individually. The two high order address bits ( $A_{11}$ , and  $A_{12}$ ) select only one of the four components.

**XM20C64**

**TABLE 1**

Step	Operation	A <sub>0</sub> –A <sub>10</sub> *	Data Pattern
1	Write	555	AA
2	Write	2AA	55
3	Write	555	Command

3874 Pgm T11

\* It should be noted, the high order addresses should remain stable during the operations. It should also be noted that these commands are not global, that is only one device on the module will be affected by each command operation.

**TABLE 2**

Command [Hex]	Function
CC	Enable Autostore
CD	Disable Autostore
33	Perform Immediate Store

3874 Pgm T12

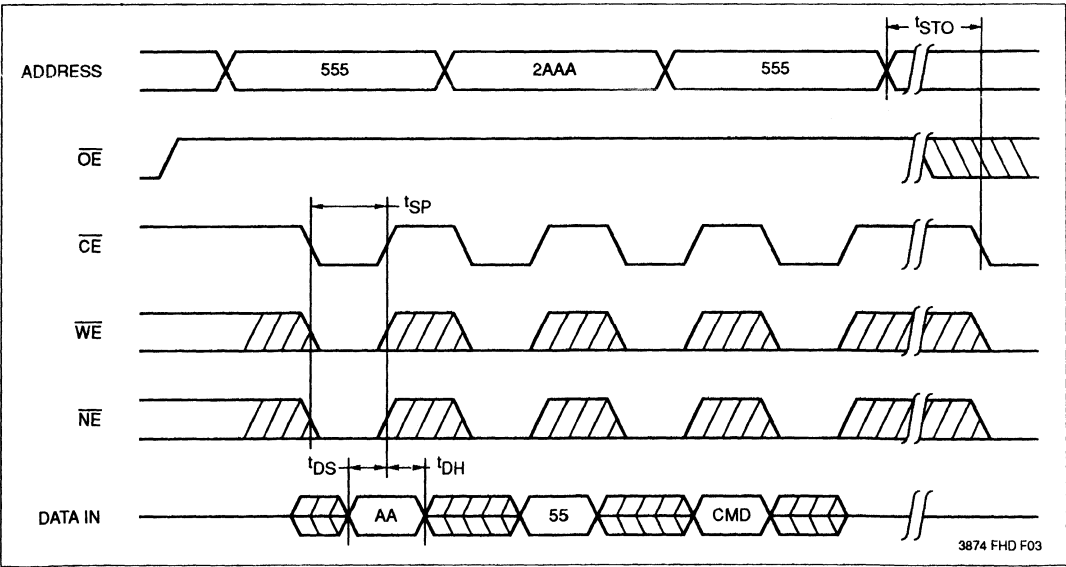
**Command Sequence Timing Limits**

Symbol	Parameter	Limits		Units
		Min.	Max.	
t <sub>STO</sub>	Store Time		5	ns
t <sub>SP</sub>	Command Write Pulse Width	50		ns
t <sub>SPH</sub>	Inter Command Delay	55		ns

**Note:** All Write Command Sequence timings must conform to the standard write timing requirements.

3874 PGM T01

**Command Write Sequence**



3874 FHD F03



# XM20C64

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	–65°C to +125°C
Storage Temperature .....	–65°C to +125°C
Voltage on any Pin with Respect to Ground .....	–1.0V to +7V

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the module. This is a stress rating only and the functional operation of the module at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect module reliability.

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Military	–55°C	+125°C

3874 PGM T06

Supply Voltage	Limits
XM20C64	5V ±10%

3874 PGM T07

## D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I <sub>CC1</sub>	V <sub>CC</sub> Active Current		100	mA	$\overline{NE} = \overline{WE} + V_{IH}$ , $\overline{CE} = \overline{OE} = V_{IL}$ , Address Inputs = TTL Inputs @ f = 20MHz All I/Os = Open
I <sub>CC2</sub>	V <sub>CC</sub> Active Current (AUTOSTORE)		10	mA	All Inputs = V <sub>IH</sub> , All I/Os = Open
I <sub>SB</sub>	V <sub>CC</sub> Standby Current		1.5	mA	All Inputs = V <sub>CC</sub> –0.3V All I/Os = Open
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub> , $\overline{CE} = V_{IH}$
V <sub>IL</sub> (1)	Input Low Voltage	–0.5	0.8	V	
V <sub>IH</sub> (1)	Input High Voltage	2.0	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 5mA
V <sub>OLAS</sub>	AUTOSTORE Output Voltage		0.4	V	I <sub>OLAS</sub> = 1mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = –4mA

3874 PGM T08

## POWER-UP TIMING

Symbol	Parameter	Max.	Units
t <sub>PUR</sub>	Power-Up (V <sub>CC</sub> Min.) to RAM Operation	500	μs
t <sub>PUST</sub>	Power-Up (V <sub>CC</sub> Min.) to Store Operation	5	ms

3874 PGM T09

## CAPACITANCE T<sub>A</sub> = 25°C, F = 1.0MHZ, V<sub>CC</sub> = 5V.

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (2)	Input/Output Capacitance	40	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (2)	Input Capacitance	24	pF	V <sub>IN</sub> = 0V

3874 PGM T10

Notes: (1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.

(2) This parameter is periodically sampled and not 100% tested.

XM20C64

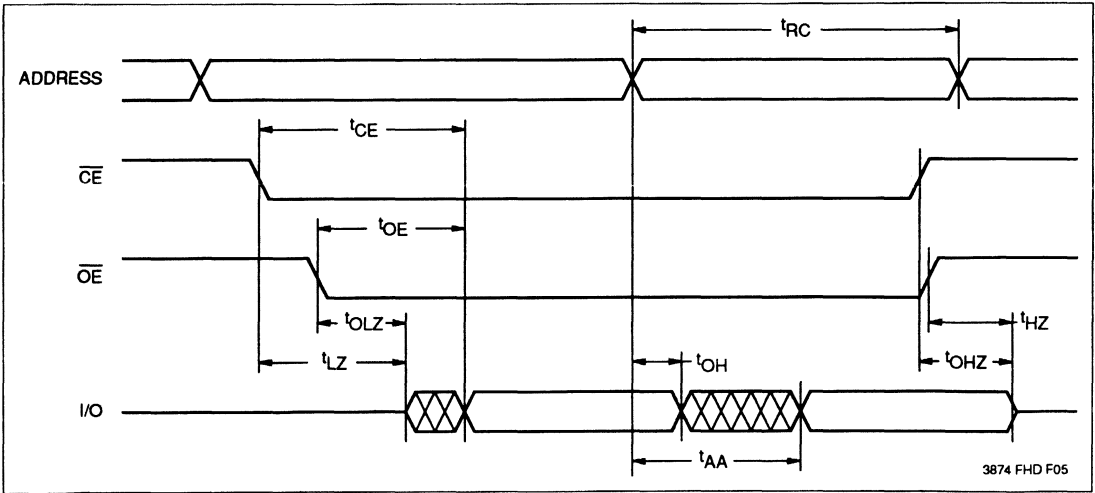
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	Limits		Units
		Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	55		ns
t <sub>CE</sub>	Chip Enable Access Time		55	ns
t <sub>AA</sub>	Address Access Time		55	ns
t <sub>OE</sub>	Output Enable Access Time		30	ns
t <sub>LZ</sub> <sup>(3)</sup>	CE Low to Output in Low Z	0		ns
t <sub>OLZ</sub> <sup>(3)</sup>	OE Low to Output in Low Z	0		ns
t <sub>HZ</sub> <sup>(3)</sup>	CE High to Output in Low Z	0	25	ns
t <sub>OHZ</sub> <sup>(3)</sup>	OE High to Output in Low Z	0	25	ns
t <sub>OH</sub>	Output Hold	0		ns

3874 PGM T03

Read Cycle Timing Diagram



3874 FHD F05

Note: (3) t<sub>LZ</sub> min., t<sub>HZ</sub> min., t<sub>OLZ</sub> min., and t<sub>OHZ</sub> min. are periodically sampled and not 100% tested. t<sub>HZ</sub> max. and t<sub>OHZ</sub> max. are measured from the point when CE or OE return high (whichever occurs first) to the time when the outputs are no longer driven.

MODE SELECTION

CE	WE	NE	OE	Mode	I/O State	Power
H	X	X	X	Module Not Selected	High Z	Standby
L	H	H	L	Read RAMActive	Data Output	Active
L	L	H	X	Write RAM	Data Input	Active
L	L	L	H	Issue Software Command	Data Input	Active
L	H	H	H	Output Disabled	High Z	Active
L	H	L	L	Hardware Array Recall	High Z	Active
L	H	L	H	No Op	High Z	Active
L	L	L	L	Not Allowed	High Z	Active

3874 PGM T04

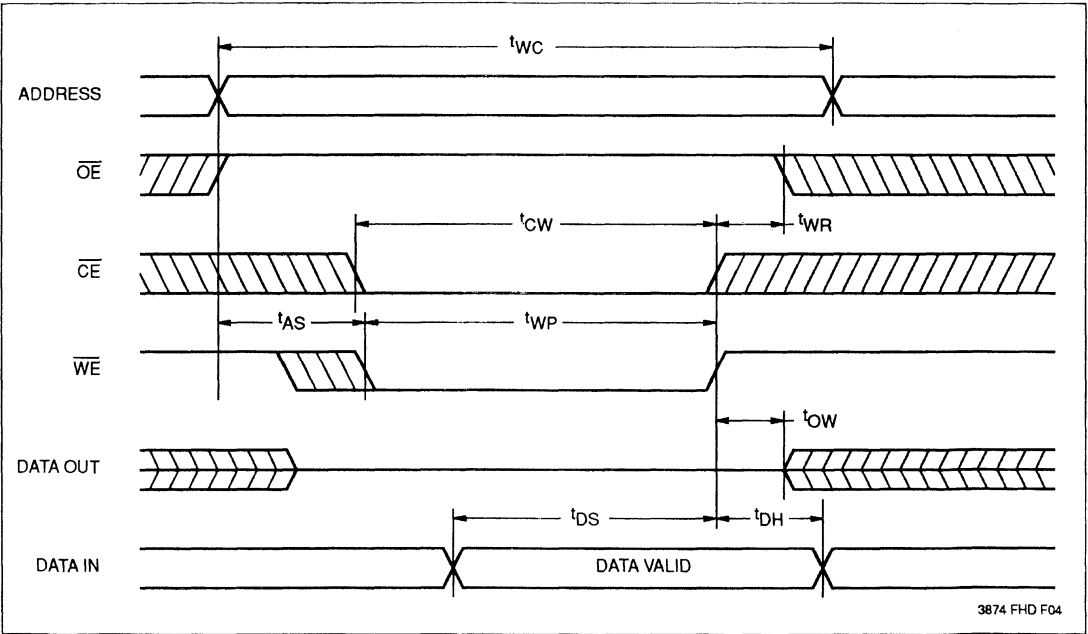
**XM20C64**

**Write Cycle Limits**

Symbol	Parameter	Limits		Units
		Min.	Max.	
$t_{WC}$	Write Cycle time	55		ns
$t_{WP}$	WE Pulse Width	40		ns
$t_{CW}$	$\overline{CE}$ Pulse Width	40		ns
$t_{AS}$	Address Setup	0		ns
$t_{DS}$	Data Setup	25		ns
$t_{DH}$	Data Hold	0		ns
$t_{OW}$	Output Active from End of Write		5	ns
$t_{WR}$	End of Write to Read	0		ns

3874 PGM T02

**Write Cycle Timing Diagram**



3874 FHD F04

**XM20C64**

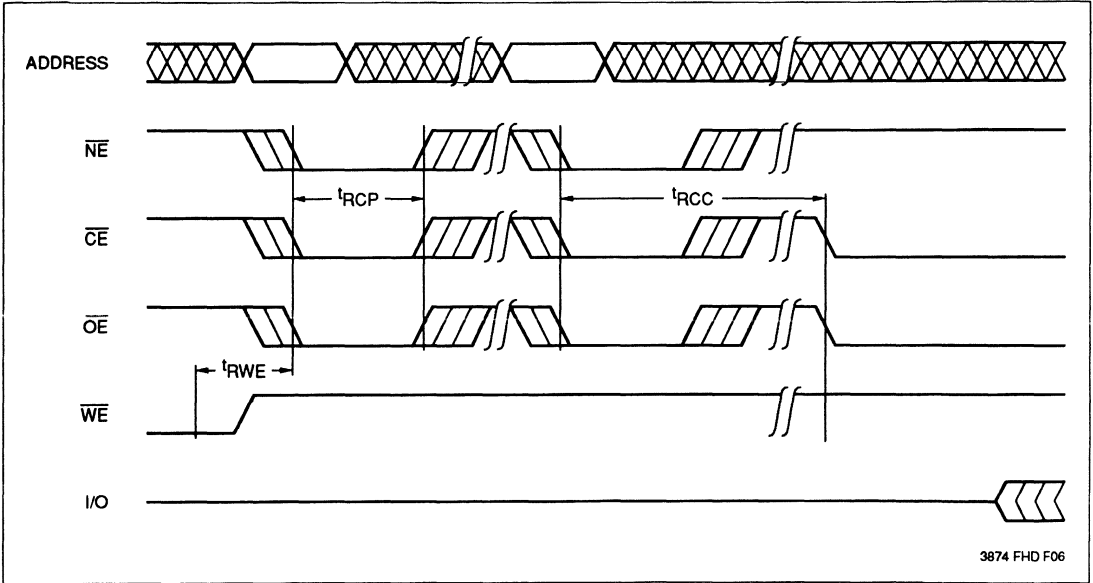
**Array Recall Timing**

Symbol	Parameter	Limits		Units
		Min.	Max.	
$t_{RCC}$	Array Recall Time		10	
$t_{RCP}$	Recall Strobe Pulse Width	50		
$t_{RWE}$	Delay From WE HIGH to Recall	0		

3874 PGM T05

**Note:** The recall sequence must be repeated for each memory component individually. This is accomplished by sequencing through the Array Recall Cycle with all four combinations of  $A_{11}$ , and  $A_{12}$ .

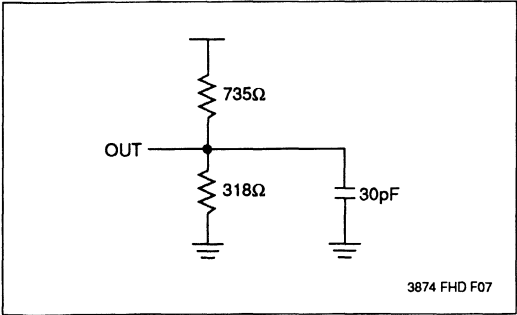
**Array Recall Cycle**



3874 FHD F06

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**EQUIVALENT TEST LOAD CIRCUIT**



3874 FHD F07

**XM20C64**

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**NOTES**

## 64K

## XM20C64FR

**8K x 8**

## High Speed AUTOSTORE™ NOVRAM

## FEATURES

- **High Speed:  $t_{AA} = 55ns$**
- **NO Batteries!!**
- **Low Power CMOS**
- **AUTOSTORE™ NOVDRAM**
  - Automatically Stores RAM data to E2PROM upon Power-fail Detection
- **Open Drain AUTOSTORE Output Pin**
  - Provides Interrupt or Status Information
  - Linkable to System Reset Circuitry
- **Auto Recall**
  - Automatically Recalls E2PROM Data During Power-on
- **Fully Decoded Module**
- **Two Temperature Ranges**
  - Commercial
  - Industrial
- **High Reliability**
  - Endurance: 1,000,000 Store Cycles
  - Data Retention: 100 Years
- **ESD Protection**
  - >2KV All Pins

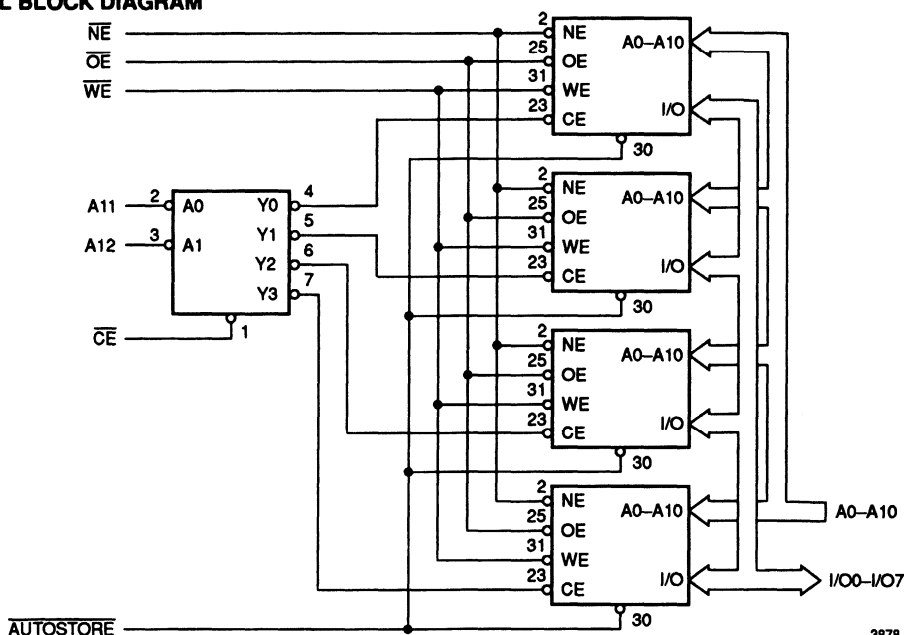
## DESCRIPTION

The XM20C64FR is a high speed nonvolatile RAM Module. It is comprised of four Xicor X20C16 high speed NOVRAMs, a high speed "ACT" decoder and decoupling capacitors mounted on a FR-4 substrate. The XM20C64FR is configured 8K x 8 and is fully decoded. The module is a 28-lead DIP conforming to the industry standard pinout for SRAMs.

The XM20C64FR fully supports the AUTOSTORE feature, providing hands-off automatic storing of RAM data into E2PROM when  $V_{CC}$  falls below the AUTOSTORE threshold.

The XM20C64FR is a highly reliable memory component, supporting unlimited writes to RAM, a minimum 1,000,000 store cycles and a minimum 100 year data retention.

### FUNCTIONAL BLOCK DIAGRAM



3878 FHD F01

**AUTOSTORE™ NOVRAM** is a trademark of Xicor, Inc.

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Characteristics subject to change without notice

# XM20C64FR

## PIN DESCRIPTIONS

### Addresses ( $A_0$ – $A_{12}$ )

The address inputs select an 8-bit memory location during read and write operations.

### Chip Enable ( $\overline{CE}$ )

The chip enable input must be LOW to enable all read, write and user requested nonvolatile operations.

### Output Enable ( $\overline{OE}$ )

During normal RAM operations  $\overline{OE}$  controls the data output buffers. If a hardware nonvolatile operation is selected ( $\overline{NE} = \overline{CE} = \text{LOW}$ ) and  $\overline{OE}$  strobes LOW a recall operation will be initiated.

$\overline{OE}$  LOW will always disable a STORE operation regardless of the state of  $\overline{NE}$ ,  $\overline{WE}$ , and  $\overline{CE}$  so long as the internal transfer has not commenced.

### Write Enable ( $\overline{WE}$ )

During normal RAM operations  $\overline{WE} = \overline{CE} = \text{LOW}$  will cause data to be written to the RAM address pointed to by the  $A_0$ – $A_{12}$  inputs.

### Nonvolatile Enable ( $\overline{NE}$ )

The nonvolatile input controls the transfer of data from the E<sup>2</sup>PROM array to the RAM array, when strobed LOW in conjunction with  $\overline{CE} = \overline{OE} = \text{LOW}$ .

### Data In/Data Out ( $I/O_0$ – $I/O_7$ )

Data is written to or read from the X20C64 through the I/O pins. The I/O pins are placed in the high impedance state when either  $\overline{CE}$  or  $\overline{OE}$  is HIGH or when  $\overline{NE}$  is LOW.

### AUTOSTORE OUTPUT ( $\overline{AS}$ )

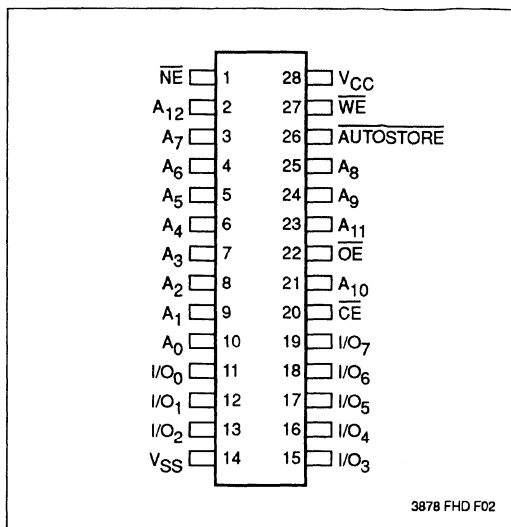
$\overline{AS}$  is an open drain output. When it is asserted (driving LOW) it indicates  $V_{CC}$  has fallen below the AUTOSTORE threshold and an internal store operation has been initiated. Because  $\overline{AS}$  is an open drain output it may be wire-ORed with multiple open drain outputs and used as an interrupt input or as an input to a power on reset circuit.

## DEVICE OPERATION

RAM operations are identical to those of a standard SRAM. When  $\overline{OE}$  and  $\overline{CE}$  are asserted data is presented at the I/Os from the address location pointed to by the  $A_0$ – $A_{12}$  inputs.

RAM write operations are initiated and the address input is latched by HIGH to LOW transition of  $\overline{CE}$  or  $\overline{WE}$ ,

## PIN CONFIGURATION



whichever occurs last. Data are latched on the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first.

An array recall, E<sup>2</sup>PROM data transferred to RAM, is initiated whenever  $\overline{OE} = \overline{CE} = \text{LOW}$ . A recall is also performed automatically upon power up.

## COMMAND SEQUENCE OPERATIONS

The X20C64 employs a version of the industry standard Software Data Protection (SPD). The end user can select various options for transferring data from RAM into the E<sup>2</sup>PROM array.

All command sequences are comprised of three specific data/address write operations performed with  $\overline{NE}$  LOW. A Store operation can be directly selected by issuing an immediate Store command. The user may also enable and disable the AUTOSTORE function through the software data protection sequence. Refer to Table 1 below for a complete description of the command sequence.

## OPERATIONAL NOTES

The X20C64 should be viewed as a subsystem when writing software for the various store operations. The module contains four discrete components each needing to be set to the required state individually. The two high order address bits ( $A_{11}$  and  $A_{12}$ ) select only one of the four components.

XM20C64FR

TABLE 1

Step	Operation	A <sub>0</sub> –A <sub>10</sub> *	Data Pattern
1	Write	555	AA
2	Write	2AA	55
3	Write	555	Command

3878 Pgm T11

\* It should be noted, the high order addresses should remain stable during the operations. It should also be noted that these commands are not global, that is only one device on the module will be affected by each command operation.

TABLE 2

Command [Hex]	Function
CC	Enable Autostore
CD	Disable Autostore
33	Perform Immediate Store

3878 Pgm T12

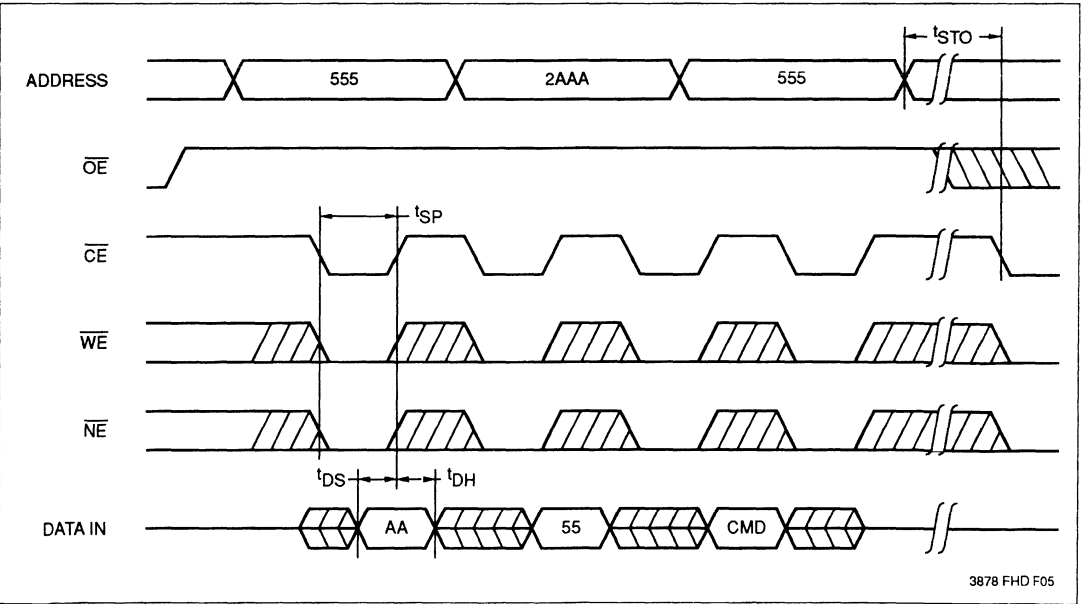
Command Sequence Timing Limits

Symbol	Parameter	Limits		Units
		Min.	Max.	
t <sub>STO</sub>	Store Time		5	ns
t <sub>SP</sub>	Command Write Pulse Width	50		ns
t <sub>SPH</sub>	Inter Command Delay	55		ns

3878 PGM T15

**Note:** All Write Command Sequence timings must conform to the standard write timing requirements.

Command Write Sequence





# XM20C64FR

### ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....	-65°C to +125°C
Storage Temperature .....	-65°C to +125°C
Voltage on any Pin with Respect to Ground .....	-1.0V to +7V

### RECOMMEND OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C

3826 PGM T02

### \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the module. This is a stress rating only and the functional operation of the module at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect module reliability.

Supply Voltage	Limits
XM20C64FR	5V $\pm$ 10%

3826 PGM T03

### D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I <sub>CC1</sub>	V <sub>CC</sub> Active Current		100	mA	$\overline{NE} = \overline{WE} = V_{IH}$ , $\overline{CE} = \overline{OE} = V_{IL}$ Address Inputs = TTL Inputs @ f = 20MHz All I/Os = Open
I <sub>CC2</sub>	V <sub>CC</sub> Active Current (AUTOSTORE)		10	mA	All Inputs = V <sub>IH</sub> , All I/Os - Open
I <sub>SB</sub>	V <sub>CC</sub> Standby Current		1.5	mA	All Inputs = V <sub>CC</sub> -0.3V All I/Os = Open
I <sub>LI</sub>	Input Leakage Current		10	$\mu$ A	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	$\mu$ A	V <sub>OUT</sub> = GND to V <sub>CC</sub> , $\overline{CE} = V_{IH}$
V <sub>IL</sub> (1)	Input Low Voltage	-0.5	0.8	V	
V <sub>IH</sub> (1)	Input High Voltage	2.0	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 5mA
V <sub>OLAS</sub>	AUTOSTORE Output		0.4	V	I <sub>OLAS</sub> = 1mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -4mA

3826 PGM T04

### POWER-UP TIMING

Symbol	Parameter	Max.	Units
t <sub>PUR</sub>	Power-Up (V <sub>CC</sub> Min.) to RAM Operation	500	$\mu$ s
t <sub>PUW</sub>	Power-Up (V <sub>CC</sub> Min.) to Store Operation	5	ms

3826 PGM T05

### CAPACITANCE T<sub>A</sub> = 25°C, F = 1.0MHZ, V<sub>CC</sub> = 5V.

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (2)	Input/Output Capacitance	40	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (2)	Input Capacitance	24	pF	V <sub>IN</sub> = 0V

3826 PGM T06

Notes: (1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.

XM20C64FR

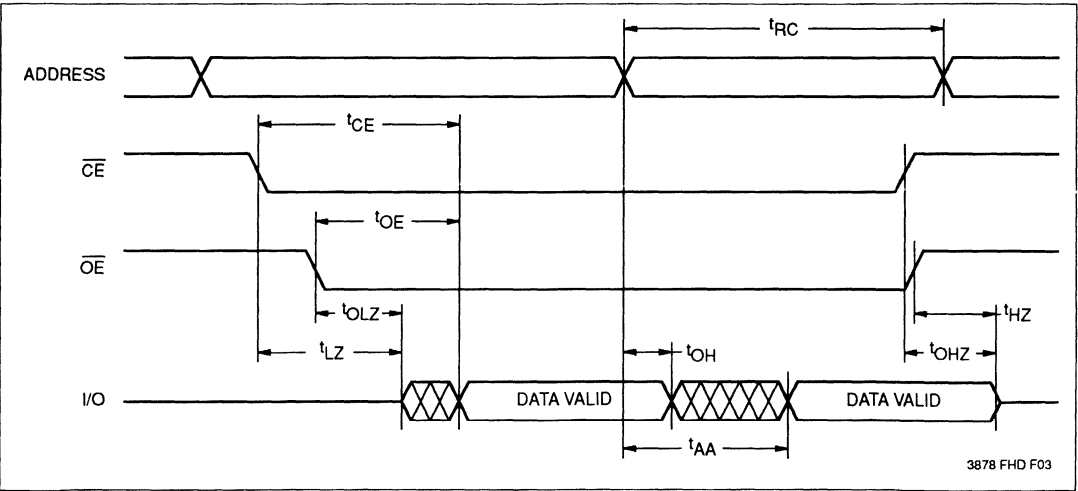
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	Limits		Units
		Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	55		ns
t <sub>CE</sub>	Chip Enable Access Time		55	ns
t <sub>AA</sub>	Address Access Time		55	ns
t <sub>OE</sub>	Output Enable Access Time		30	ns
t <sub>LZ</sub>	CE Low to Output in Low Z	0		ns
t <sub>OLZ</sub>	OE Low to Output in Low Z	0		ns
t <sub>HZ</sub>	CE High to Output in Low Z	0	25	ns
t <sub>OHZ</sub>	OE High to Output in Low Z	0	25	ns
t <sub>OH</sub>	Output Hold	0		ns

3826 PGM T10

Read Cycle Timing Diagram



3878 FHD F03

Mode Selection

Control Input States				Mode	I/O State	Power
CE	WE	NE	OE			
H	X	X	X	Module Not Selected	High Z	Standby
L	H	H	L	Read RAM	Data Output	Active
L	L	H	X	Write RAM	Data Input	Active
L	L	L	H	Issue Software Command	Data Input	Active
L	H	H	H	Output Disabled	High Z	Active
L	H	L	L	Hardware Array Recall	High Z	Active
L	H	L	H	No Op	High Z	Active
L	L	L	L	Not Allowed	High Z	Active

3878 PGM T15

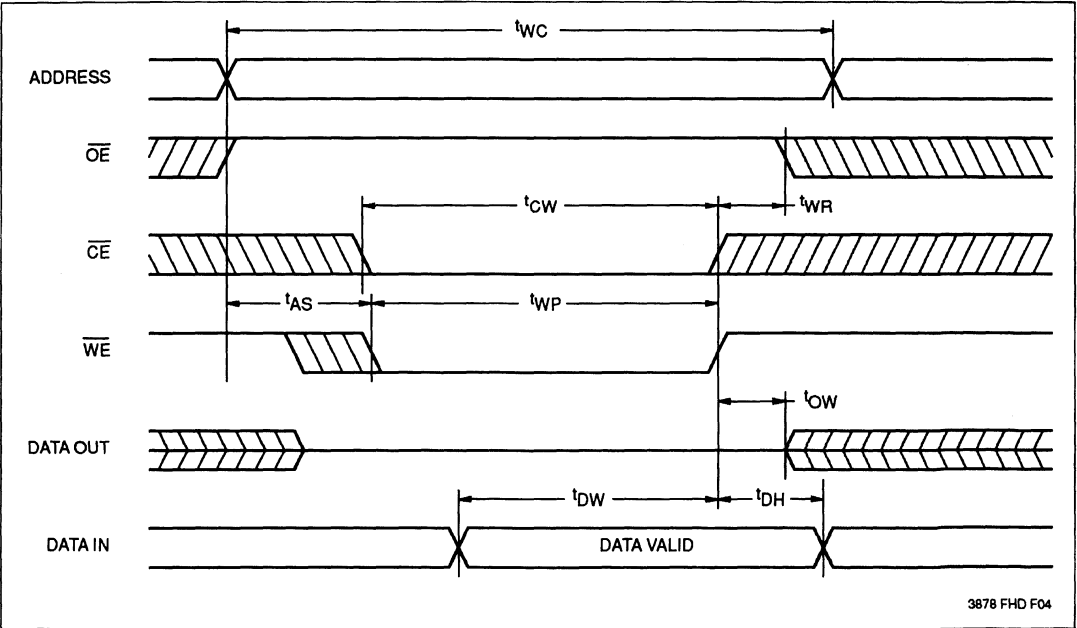
**XM20C64FR**

**Write Cycle Limits**

Symbol	Parameter	Limits		Units
		Min.	Max.	
t <sub>WC</sub>	Write CycleTime	55		ns
t <sub>WP</sub>	WE Pulse Width	40		ns
t <sub>CW</sub>	CE Pulse Width	40		ns
t <sub>AS</sub>	Address Setup	0		ns
t <sub>DS</sub>	Data Setup	25		ns
t <sub>DH</sub>	Data Hold	0		ns
t <sub>OW</sub>	Output Active from End of Write		5	ns
t <sub>WR</sub>	End of Write to Read	0		ns

3826 PGM T10

**Write Cycle Timing Diagram**



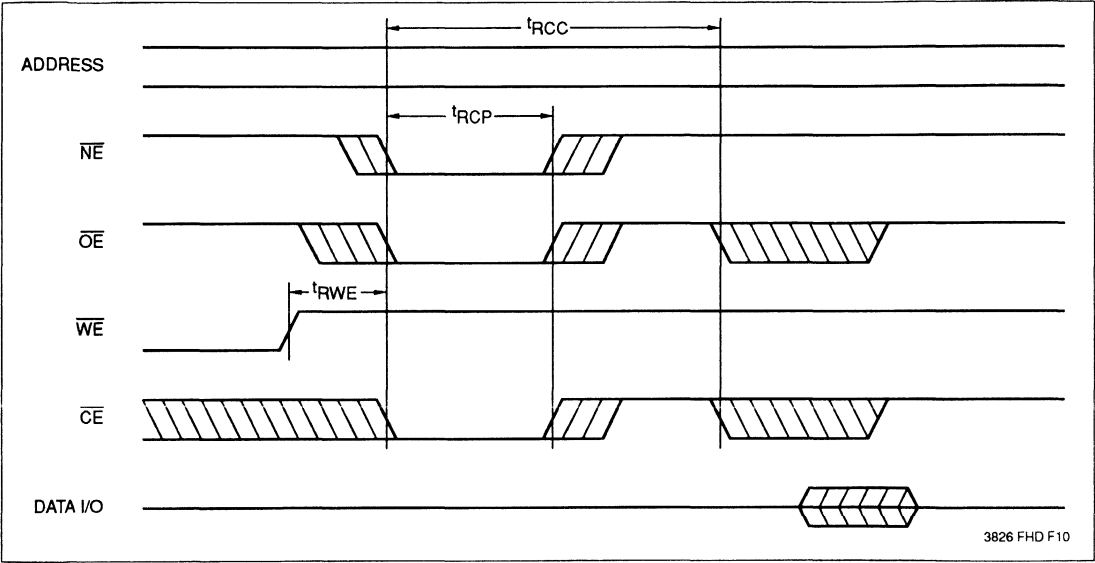
XM20C64FR

ARRAY RECALL CYCLE LIMITS

Symbol	Parameter	Limits		Units
		Min.	Max.	
$t_{RCC}$	Array Recall Cycle Time		10	$\mu$ s
$t_{RCP}^{(5)}$	Recall Pulse Width to Initiate Recall	50		ns
$t_{RWE}$	WE Setup Time to NE	0		ns

3878 PGM T13

Array Recall Cycle

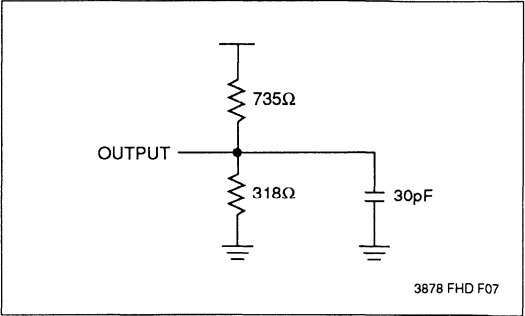


**Note:** (5) The Recall Pulse Width ( $t_{RCP}$ ) is a minimum time that  $\overline{NE}$ ,  $\overline{OE}$  and  $\overline{CE}$  must be LOW simultaneously. To insure data integrity,  $\overline{NE}$  and  $\overline{CE}$  must return HIGH after initiation of and through the duration ( $t_{RCC}$ , 10  $\mu$ s) of the Recall operation. During  $t_{RCC}$ ,  $\overline{OE}$  and  $\overline{WE}$  may go LOW providing the host access to other devices in the system.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

EQUIVALENT A.C. LOAD CIRCUIT



**XM20C64FR**

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**NOTES**



## Advance Information

64K

XM20C64S

8K x 8

## High Speed AUTOSTORE™ NOVRAM

### FEATURES

- High Speed:  $t_{AA} = 55 \text{ ns}$
- NO! Batteries!!
- AUTOSTORE™ NOVRAM
  - Automatically Stores RAM data to E<sup>2</sup>PROM upon Power-fall Detection
- Open Drain AUTOSTORE Output Pin
  - Provides Interrupt or Status Information
  - Linkable to System Reset Circuitry
- Low Power CMOS
- Auto Recall
  - Automatically Recalls E<sup>2</sup>PROM Data During Power-on
- Fully Decoded Module
- Two Temperature Ranges
  - Commercial
  - Industrial
- High Reliability
  - Endurance: 1,00,000 Store Cycles
  - Data Retention: 100 Years
- ESD Protection
  - $\geq 2\text{KV}$  All Pins

### DESCRIPTION

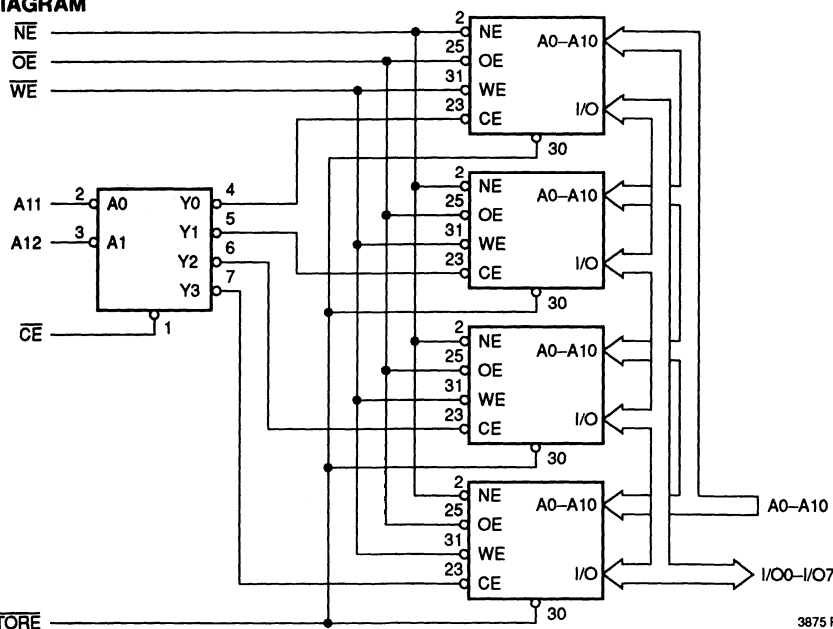
The XM20C64S is a high speed nonvolatile RAM Module. It is comprised of four Xicor X20C16 high speed NOVRAMs, a high speed "ACT" decoder and decoupling capacitors mounted on a FR-4 substrate. The XM20C64S is configured 8K x 8 and is fully decoded. The module is a 36-pin SIP conforming to the industry standard pinout for SRAMs.

The XM20C64S fully supports the AUTOSTORE feature, providing hands-off automatic storing of RAM data into E<sup>2</sup>PROM when  $V_{CC}$  falls below the AUTOSTORE threshold.

The XM20C64S is a highly reliable memory component, supporting unlimited writes to RAM, a minimum 1,000,000 store cycles and a minimum 100 year data retention.

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### FUNCTIONAL DIAGRAM



AUTOSTORE™ NOVRAM is a trademark of Xicor, Inc.

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# XM20C64S

## PIN DESCRIPTIONS

### Addresses ( $A_0$ - $A_{12}$ )

The address inputs select an 8-bit memory location during read and write operations.

### Chip Enable ( $\overline{CE}$ )

The chip enable input must be LOW to enable all read, write and user requested nonvolatile operations.

### Output Enable ( $\overline{OE}$ )

During normal RAM operations  $\overline{OE}$  controls the data output buffers. If a hardware nonvolatile operation is selected ( $\overline{NE} = \overline{CE} = \text{LOW}$ ) and  $\overline{OE}$  strobes LOW a recall operation will be initiated.

$\overline{OE}$  LOW will always disable a STORE operation regardless of the state of  $\overline{NE}$ ,  $\overline{WE}$ , and  $\overline{CE}$  so long as the internal transfer has not commenced.

### Write Enable ( $\overline{WE}$ )

During normal RAM operations  $\overline{WE} = \overline{CE} = \text{LOW}$  will cause data to be written to the RAM address pointed to by the  $A_0$ - $A_{12}$  inputs.

### Nonvolatile Enable ( $\overline{NE}$ )

The nonvolatile input controls the transfer of data from the E<sup>2</sup>PROM array to the RAM array, when strobed LOW in conjunction with  $\overline{CE} = \overline{OE} = \text{LOW}$ .

### Data In/Data Out ( $I/O_0$ - $I/O_7$ )

Data is written to or read from the X20C64 through the I/O pins. The I/O pins are placed in the high impedance state when either  $\overline{CE}$  or  $\overline{OE}$  is HIGH or when  $\overline{NE}$  is LOW.

### AUTOSTORE Output ( $\overline{AS}$ )

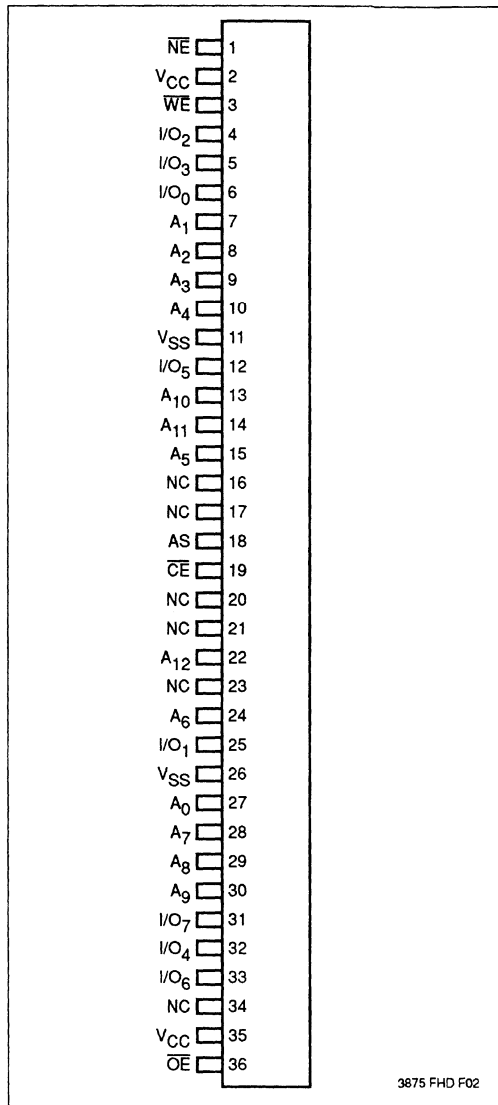
$\overline{AS}$  is an open drain output. When it is asserted (driving LOW) it indicates  $V_{CC}$  has fallen below the AUTOSTORE threshold and an internal store operation has been initiated. Because  $\overline{AS}$  is an open drain output it may be wire-ORed with multiple open drain outputs and used as an interrupt input or as an input to a power on reset circuit.

## DEVICE OPERATION

RAM operations are identical to those of a standard SRAM. When  $\overline{OE}$  and  $\overline{CE}$  are asserted data is presented at the I/Os from the address location pointed to by the  $A_0$ - $A_{12}$  inputs.

RAM write operations are initiated and the address input is latched by the HIGH to LOW transition of  $\overline{CE}$  or  $\overline{WE}$ ,

## PIN CONFIGURATION



whichever occurs last. Data are latched on the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first.

An array recall, E<sup>2</sup>PROM data transferred to RAM, is initiated whenever  $\overline{OE} = \overline{NE} = \overline{CE} = \text{LOW}$ . A recall is also performed automatically upon power up.

# XM20C64S

TABLE 1

Step	Operation	A <sub>0</sub> –A <sub>10</sub> *	Data Pattern
1	Write	555	AA
2	Write	2AA	55
3	Write	555	Command

3875 Pgm T11

\* It should be noted, the high order addresses should remain stable during the operations. It should also be noted that these commands are not global, that is only one device on the module will be affected by each command operation.

## Command Sequence Operations

The X20C64 employs a version of the industry standard Software Data Protection (SDP). The end user can select various options for transferring data from RAM into the E<sup>2</sup>PROM array.

All command sequences are comprised of three specific data/address write operations performed with  $\overline{NE}$ LOW. A Store operation can be directly selected by issuing an Immediate Store command. The user may also enable

TABLE 2

Command [Hex]	Function
CC	Enable Autostore
CD	Disable Autostore
33	Perform Immediate Store

3875 Pgm T12

and disable the AUTOSTORE function through the software data protection sequence. Refer to Table 1 below for a complete description of the command sequence.

## Operational Notes

The X20C64 should be viewed as a subsystem when writing software for the various store operations. The module contains four discrete components each needing to be set to the required state individually. The two high order address bits (A<sub>11</sub>, and A<sub>12</sub>) select only one of the four components.

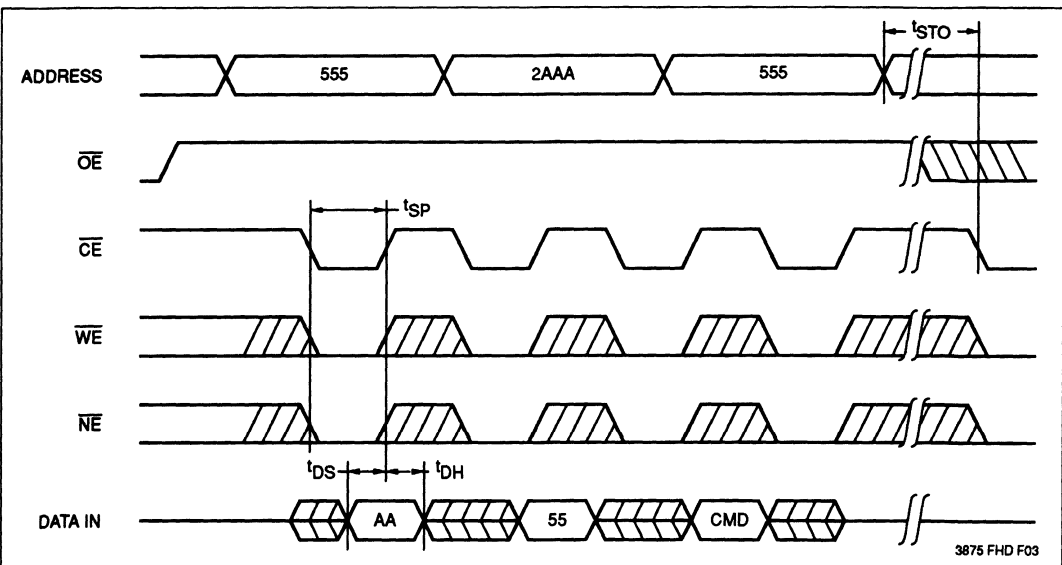
## Command Sequence Timing Limits

Symbol	Parameter	Limits		Units
		Min.	Max.	
t <sub>STO</sub>	Store Time		5	ns
t <sub>SP</sub>	Command Write Pulse Width	50		ns
t <sub>SPH</sub>	Inter Command Delay	55		ns

**Note:** All Write Command Sequence timings must conform to the standard write timing requirements.

3875 PGM T01

## Command Write Sequence



3875 FHD F03



**XM20C64S**

**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias .....	−65°C to +125°C
Storage Temperature .....	−65°C to +125°C
Voltage on any Pin with Respect to Ground .....	−1.0V to +7V

**\*COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the module. This is a stress rating only and the functional operation of the module at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect module reliability.

**RECOMMENDED OPERATING CONDITIONS**

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	−40°C	+85°C

3875 PGM T06

Supply Voltage	Limits
XM20C64S	5V ±10%

3875 PGM T07

**D.C. OPERATING CHARACTERISTICS** (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I <sub>CC1</sub>	V <sub>CC</sub> Active Current		100	mA	$\overline{NE} = \overline{WE} + V_{IH}$ , $\overline{CE} = \overline{OE} = V_{IL}$ , Address Inputs = TTL Inputs @ f = 20MHz All I/Os = Open
I <sub>CC2</sub>	V <sub>CC</sub> Active Current (AUTOSTORE)		10	mA	All Inputs = V <sub>IH</sub> , All I/Os = Open
I <sub>SB</sub>	V <sub>CC</sub> Standby Current		1.5	mA	All Inputs = V <sub>CC</sub> −0.3V All I/Os = Open
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>IN</sub> = GND to V <sub>CC</sub> , $\overline{CE} = V_{IH}$
V <sub>IL</sub> (1)	Input Low Voltage	−0.5	0.8	V	
V <sub>IH</sub> (1)	Input High Voltage	2.0	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 5mA
V <sub>OLAS</sub>	AUTOSTORE Output Voltage		0.4	V	I <sub>OLAS</sub> = 1mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = −4mA

3875 PGM T08

**POWER-UP TIMING**

Symbol	Parameter	Max.	Units
t <sub>PUR</sub>	Power-Up (V <sub>CC</sub> Min.) to RAM Operation	500	μs
t <sub>PUST</sub>	Power-Up (V <sub>CC</sub> Min.) to Store Operation	5	ms

3875 PGM T09

**CAPACITANCE** T<sub>A</sub> = 25°C, F = 1.0MHZ, V<sub>CC</sub> = 5V.

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (2)	Input/Output Capacitance	40	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (2)	Input Capacitance	24	pF	V <sub>IN</sub> = 0V

3875 PGM T10

Notes: (1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
 (2) This parameter is periodically sampled and not 100% tested.

XM20C64S

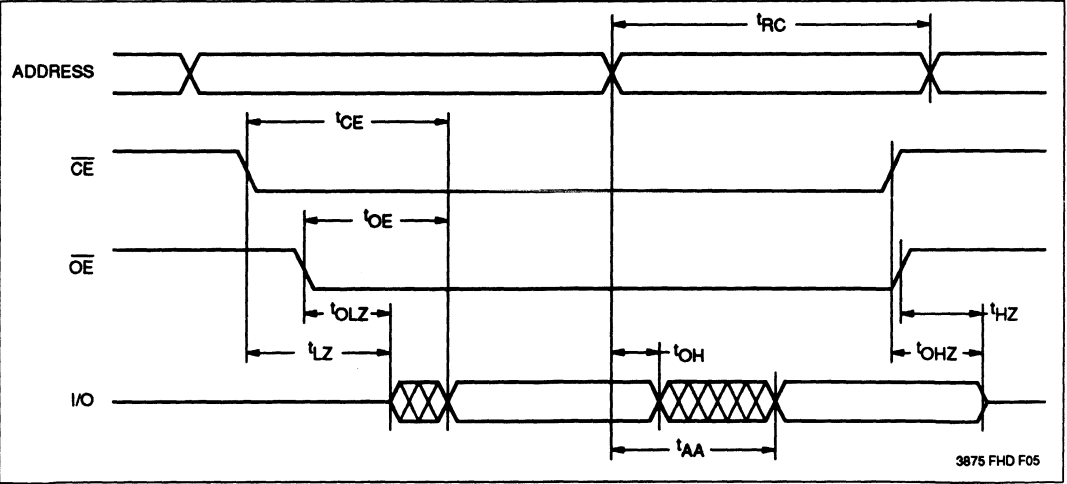
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	Limits		Units
		Min.	Max.	
$t_{RC}$	Read Cycle Time	55		ns
$t_{CE}$	Chip Enable Access Time		55	ns
$t_{AA}$	Address Access Time		55	ns
$t_{OE}$	Output Enable Access Time		30	ns
$t_{LZ}^{(3)}$	CE Low to Output in Low Z	0		ns
$t_{OLZ}^{(3)}$	OE Low to Output in Low Z	0		ns
$t_{HZ}^{(3)}$	CE High to Output in Low Z	0	25	ns
$t_{OHZ}^{(3)}$	OE High to Output in Low Z	0	25	ns
$t_{OH}$	Output Hold	0		ns

3875 PGM T03

Read Cycle Timing Diagram



3875 FHD F05

Note: (3)  $t_{LZ}$  min.,  $t_{HZ}$  min.,  $t_{OLZ}$  min., and  $t_{OHZ}$  min. are periodically sampled and not 100% tested.  $t_{HZ}$  max. and  $t_{OHZ}$  max. are measured from the point when CE or OE return high (whichever occurs first) to the time when the outputs are no longer driven.

MODE SELECTION

CE	WE	NE	OE	Mode	I/O State	Power
H	X	X	X	Module Not Selected	High Z	Standby
L	H	H	L	Read RAM	Data Output	Active
L	L	H	X	Write RAM	Data Input	Active
L	L	L	H	Issue Software Command	Data Input	Active
L	H	H	H	Output Disabled	High Z	Active
L	H	L	L	Hardware Array Recall	High Z	Active
L	H	L	H	No Op	High Z	Active
L	L	L	L	Not Allowed	High Z	Active

3875 PGM T04

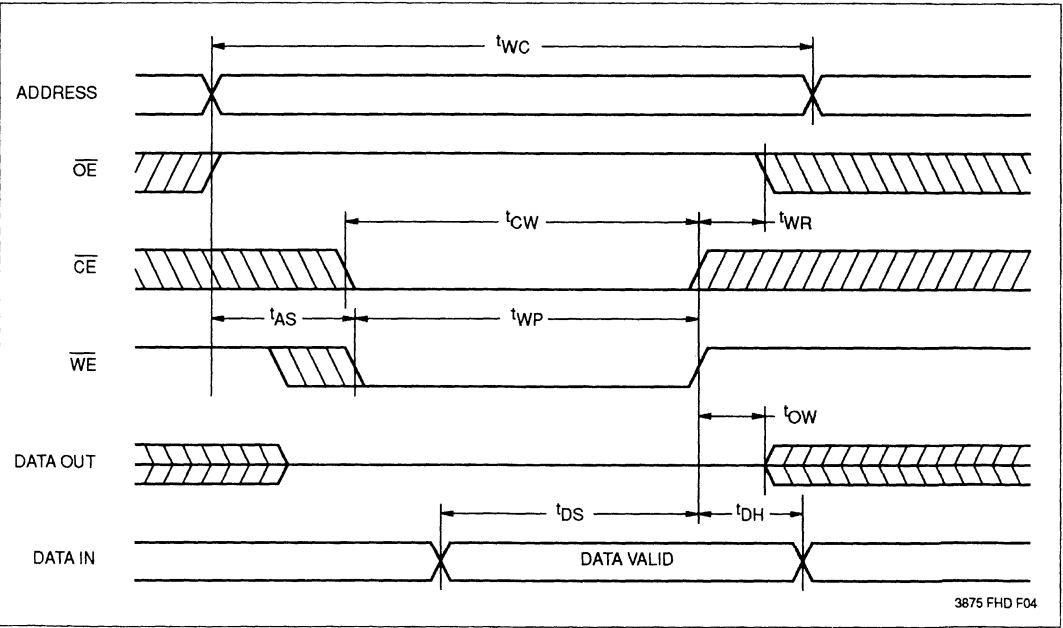
**XM20C64S**

**Write Cycle Limits**

Symbol	Parameter	Limits		Units
		Min.	Max.	
t <sub>WC</sub>	Write Cycle time	55		ns
t <sub>WP</sub>	WE Pulse Width	40		ns
t <sub>CW</sub>	CE Pulse Width	40		ns
t <sub>AS</sub>	Address Setup	0		ns
t <sub>DS</sub>	Data Setup	25		ns
t <sub>DH</sub>	Data Hold	0		ns
t <sub>OW</sub>	Output Active from End of Write		5	ns
t <sub>WR</sub>	End of Write to Read	0		ns

3875 PGM T02

**Write Cycle Timing Diagram**



3875 FHD F04

# **XM20C64S**

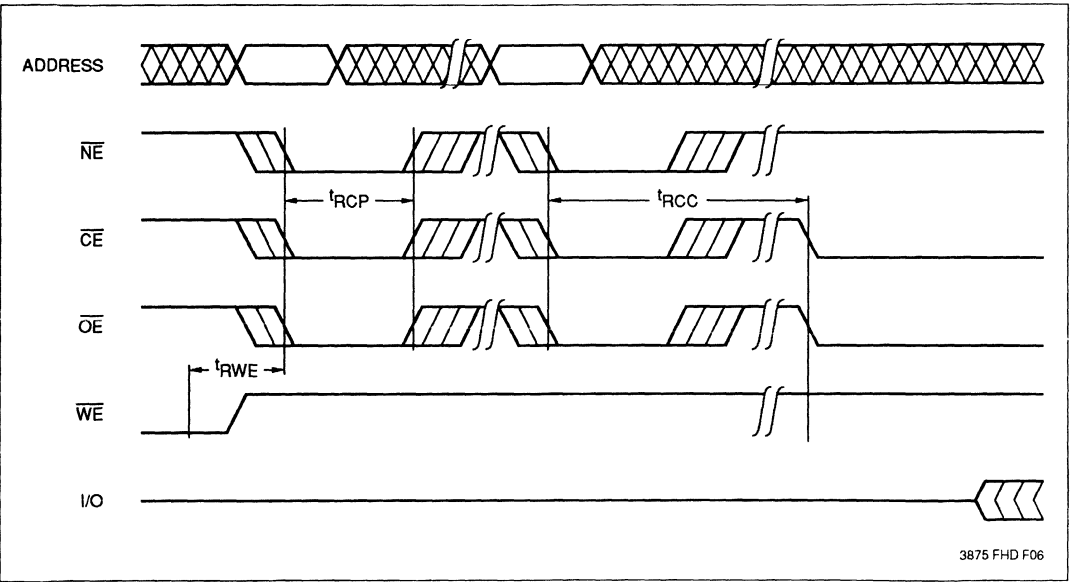
## **Array Recall Timing**

Symbol	Parameter	Limits		Units
		Min.	Max.	
$t_{RCC}$	Array Recall Time		10	
$t_{RCP}$	Recall Strobe Pulse Width	50		
$t_{RWE}$	Delay From WE HIGH to Recall	0		

3875 PGM T05

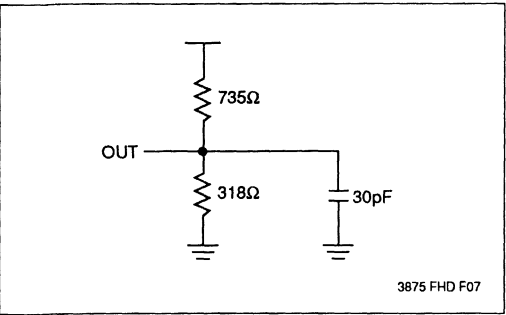
**Note:** The recall sequence must be repeated for each memory component individually. This is accomplished by sequencing through the Array Recall Cycle with all four combinations of  $A_{11}$ , and  $A_{12}$ .

## **Array Recall Cycle**



**6**

## **EQUIVALENT TEST LOAD CIRCUIT**



**XM20C64S**

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**NOTES**



## Advance Information

128K

**XM20C128S**

16K x 8

### High Speed AUTOSTORE™ NOVRAM

#### FEATURES

- **High Speed:**  $T_{AA} = 55ns$
- **NO! Batteries!!**
- **Low Power CMOS**
- **AUTOSTORE™ NOVRAM**
  - Automatically Stores RAM Data to E<sup>2</sup>PROM upon Power-fall Detection
- **Open Drain AUTOSTORE Output Pin**
  - Interrupt or Status Information
  - Linkable to System Reset Circuitry
- **Auto Recall**
  - Automatically Recalls E<sup>2</sup>PROM Data During Power-on
- **Fully Decoded Module**
- **Three Temperature Ranges**
  - Commercial
  - Industrial
- **High Reliability**
  - Endurance: 1,000,000 Store Cycles
  - Data Retention: 100 Years
- **ESD Protection**
  - $\geq 2KV$  All Pins

#### DESCRIPTION

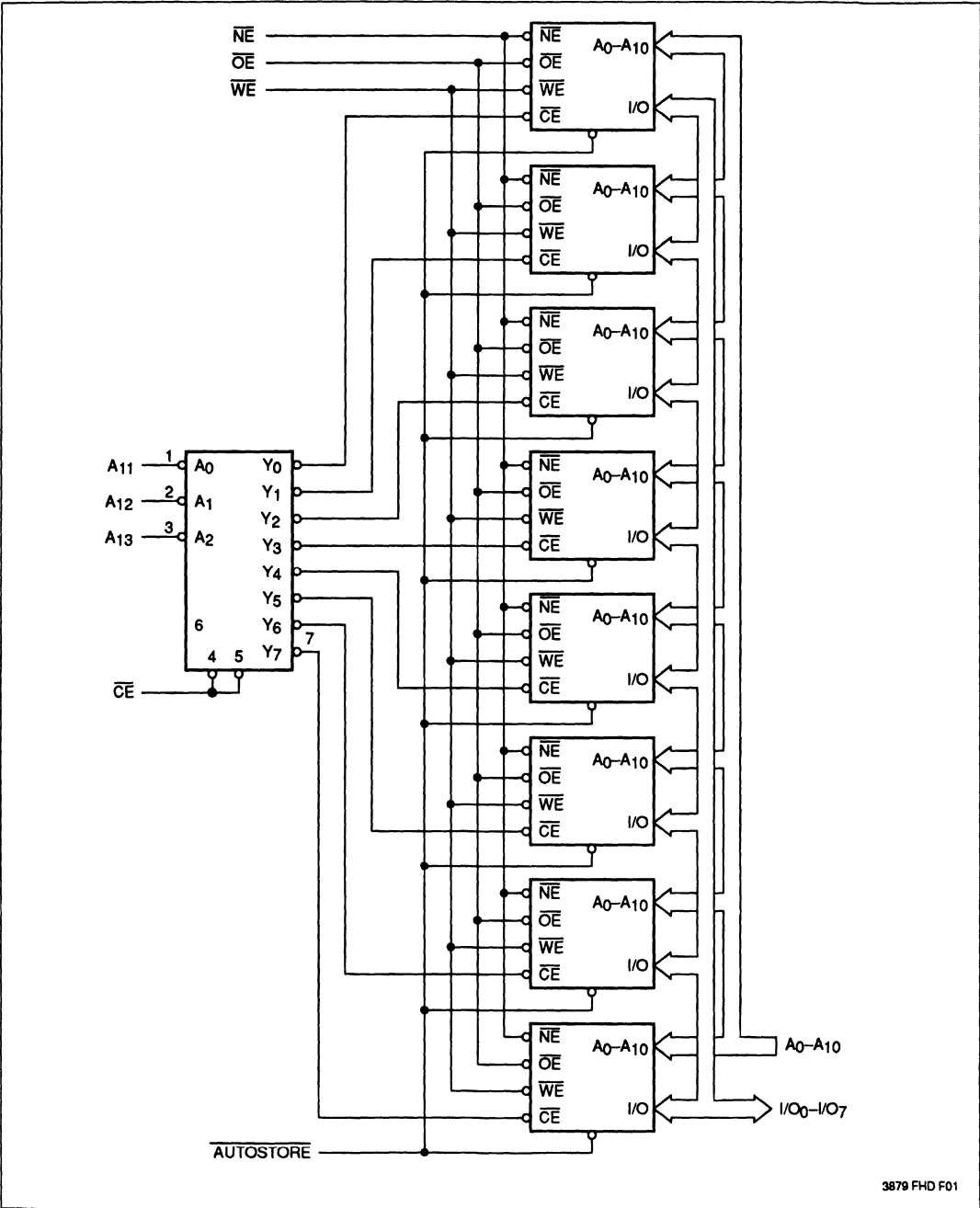
The XM20C128S is a high speed nonvolatile RAM Module. It is comprised of eight Xicor X20C16 high speed NOVRAMs, a high speed "ACT" decoder and decoupling capacitors mounted on a FR-4 substrate. The XM20C128S is configured 16K x 8 and is fully decoded. The module is a 36-pin SIP conforming to the industry standard pinout for SRAMS.

The XM20C128S fully supports the AUTOSTORE feature, providing hands-off automatic storing of RAM data into E<sup>2</sup>PROM when VCC falls below the AUTOSTORE threshold.

The XM20C128S is a highly reliable memory component, supporting unlimited writes to RAM, a minimum 1,000,000 store cycles and a minimum 100 year data retention.

**XM20C128S**

**FUNCTIONAL BLOCK DIAGRAM**



3879 FHD F01

# XM20C128S

## PIN DESCRIPTIONS

### Addresses (A<sub>0</sub>–A<sub>13</sub>)

The address inputs select an 8-bit memory location during read and write operations.

### Chip Enable ( $\overline{\text{CE}}$ )

The chip enable input must be LOW to enable all read, write and user requested nonvolatile operations.

### Output Enable ( $\overline{\text{OE}}$ )

During normal RAM operations  $\overline{\text{OE}}$  controls the data output buffers. If a hardware nonvolatile operation is selected ( $\overline{\text{NE}} = \overline{\text{CE}} = \text{LOW}$ ) and  $\overline{\text{WE}}$  strobes LOW a recall operation will be initiated.

$\overline{\text{OE}}$  LOW will always disable a STORE operation regardless of the state of  $\overline{\text{NE}}$ ,  $\overline{\text{WE}}$ , and  $\overline{\text{CE}}$  so long as the internal transfer has not commenced.

### Write Enable ( $\overline{\text{WE}}$ )

During normal RAM operations  $\overline{\text{WE}} = \overline{\text{CE}} = \text{LOW}$  will cause data to be written to the RAM address pointed to by the A<sub>0</sub>–A<sub>12</sub> inputs.

### Nonvolatile Enable ( $\overline{\text{NE}}$ )

The nonvolatile input controls the transfer of data from the E<sup>2</sup>PROM array to the RAM array, when strobed LOW in conjunction with  $\overline{\text{CE}} = \overline{\text{OE}} = \text{LOW}$ .

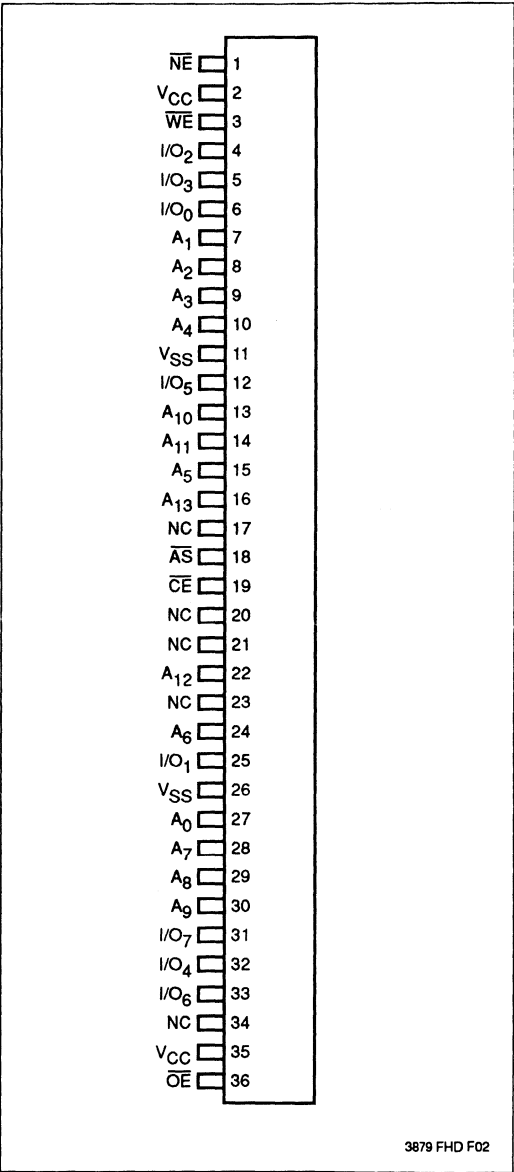
### Data In/Data Out (I/O<sub>0</sub>–I/O<sub>7</sub>)

Data is written to or read from the XM20C128S through the I/O pins. The I/O pins are placed in the high impedance state when either  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  is HIGH or when  $\overline{\text{NE}}$  is LOW.

### AUTOSTORE Output ( $\overline{\text{AS}}$ )

$\overline{\text{AS}}$  is an open drain output. When it is asserted (driving LOW) it indicates  $V_{\text{CC}}$  has fallen below the AUTOSTORE threshold and an internal store operation has been initiated. Because  $\overline{\text{AS}}$  is an open drain output it may be wire-ORed with multiple open drain outputs and used as an interrupt input or as an input to a power on reset circuit.

## PIN CONFIGURATION



3879 FHD F02



## XM20C128S

### DEVICE OPERATION

RAM operations are identical to those of a standard SRAM. When  $\overline{OE}$  and  $\overline{CE}$  are asserted data is presented at the I/Os from the address location pointed to by the  $A_0$ – $A_{13}$  inputs.

RAM write operations are initiated and the address input is latched by the HIGH to LOW transition of  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Data are latched on the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first.

An array recall, E<sup>2</sup>PROM data transferred to RAM, is initiated whenever  $\overline{OE} = \overline{NE} = \overline{CE} = \text{LOW}$ . A recall is also performed automatically upon power up.

#### Command Sequence Operations

The X20C128S employs a version of the industry standard Software Data Protection (SDP). The end user can

select various options for transferring data from RAM into the E<sup>2</sup>PROM array.

All command sequences are comprised of three specific data/address write operations performed with  $\overline{NE}$  LOW. A Store operation can be directly selected by issuing an Immediate Store command. The user may also enable and disable the AUTOSTORE function through the software data protection sequence.

#### Operational Notes

The X20C128S should be viewed as a subsystem when writing software for the various store operations. The module contains eight discrete components each needing to be set to the required state individually. The three high order address bits ( $A_{11}$ ,  $A_{12}$  and  $A_{13}$ ) select only one of the eight components.

TABLE 1. COMMAND SEQUENCE

Step	Operation	$A_0$ – $A_{10}$ *	Data Pattern	Command [Hex]	Function
1	Write	555	AA	CC	Enable AUTOSTORE
2	Write	2AA	55	CD	Disable AUTOSTORE
3	Write	555	Command	33	Perform Immediate Store

*\*It should be noted, the high order addresses should remain stable during the operations. It should also be noted that these commands are not global, that is only one device on the module will be affected by each command operation.*

### MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{NE}$	$\overline{OE}$	Mode	I/O State	Power
H	X	X	X	Module Not Selected	High Z	Standby
L	H	H	L	Read RAM	Data Output	Active
L	L	H	X	Write RAM	Data Input	Active
L	L	L	H	Issue Software Command	Data Input	Active
L	H	H	H	Output Disabled	High Z	Active
L	H	L	L	Hardware Array Recall	High Z	Active
L	H	L	H	No Op	High Z	Active
L	L	L	L	Not Allowed	High Z	Active

3879 PGM T04

XM20C128S

ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias .....-65°C to +125°C  
Storage Temperature .....-65°C to +125°C  
Voltage on any Pin with  
    Respect to Ground .....-1.0V to +7V

\*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the module. This is a stress rating only and the functional operation of the module at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect module reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C

3879 PGM T06

Supply Voltage	Limits
XM20C128S	5V ±10%

3879 PGM T07

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I <sub>CC1</sub>	V <sub>CC</sub> Active Current		200	mA	$\overline{NE} = \overline{WE} = V_{IH}$ , $\overline{CE} = \overline{OE} = V_{IL}$ Address Inputs = TTL Inputs @ f = 20MHz All I/Os = Open
I <sub>CC2</sub>	V <sub>CC</sub> Active Current (AUTOSTORE)		20	mA	All Inputs = V <sub>IH</sub> , All I/Os - Open
I <sub>SB</sub>	V <sub>CC</sub> Standby Current		3.0	mA	All Inputs = V <sub>CC</sub> -0.3V All I/Os = Open
I <sub>LI</sub>	Input Leakage Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>IN</sub> = GND to V <sub>CC</sub> , $\overline{CE} = V_{IH}$
V <sub>IL</sub> (1)	Input Low Voltage	-0.5	0.8	V	
V <sub>IH</sub> (1)	Input High Voltage	2.0	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 5mA
V <sub>OLAS</sub>	AUTOSTORE Output Voltage		0.4	V	I <sub>OLAS</sub> = 1mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -4mA

3879 PGM T08

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t <sub>PUR</sub>	Power-Up (V <sub>CC</sub> Min.) to RAM Operation	500	µs
t <sub>PUST</sub>	Power-Up (V <sub>CC</sub> Min.) to Store Operation	5	ms

3879 PGM T09

CAPACITANCE T<sub>A</sub> = 25°C, F = 1.0MHZ, V<sub>CC</sub> = 5V.

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (2)	Input/Output Capacitance	80	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (2)	Input Capacitance	48	pF	V <sub>IN</sub> = 0V

3879 PGM T10

Notes: (1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
(2) This parameter is periodically sampled and not 100% tested.

# XM20C128S

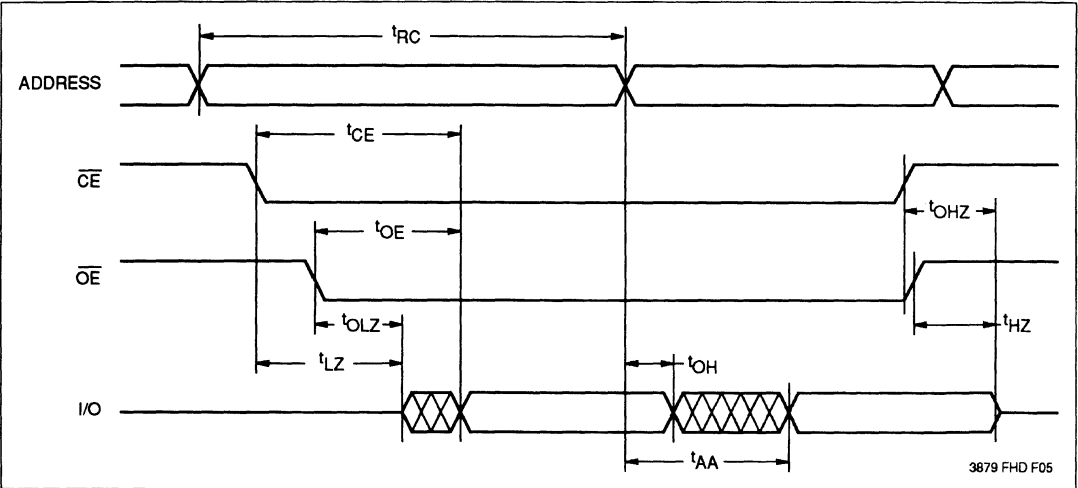
## A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

### Read Cycle Limits

Symbol	Parameter	Limits		Units
		Min.	Max.	
$t_{RC}$	Read Cycle Time	55		ns
$t_{CE}$	Chip Enable Access Time		55	ns
$t_{AA}$	Address Access Time		55	ns
$t_{OE}$	Output Enable Access Time		30	ns
$t_{LZ}^{(3)}$	$\overline{CE}$ Low to Output in Low Z	0		ns
$t_{OLZ}^{(3)}$	$\overline{OE}$ Low to Output in Low Z	0		ns
$t_{HZ}^{(3)}$	$\overline{CE}$ High to Output in Low Z	0	25	ns
$t_{OHZ}^{(3)}$	$\overline{OE}$ High to Output in Low Z	0	25	ns
$t_{OH}$	Output Hold	0		ns

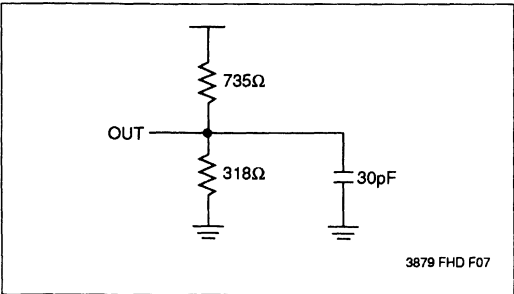
3879 PGM T03

### Read Cycle Timing Diagram



**Note:** (3)  $t_{LZ}$  min.,  $t_{HZ}$  min.,  $t_{OLZ}$  min., and  $t_{OHZ}$  min. are periodically sampled and not 100% tested.  $t_{HZ}$  max. and  $t_{OHZ}$  max. are measured from the point when  $\overline{CE}$  or  $\overline{OE}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

### EQUIVALENT TEST LOAD CIRCUIT



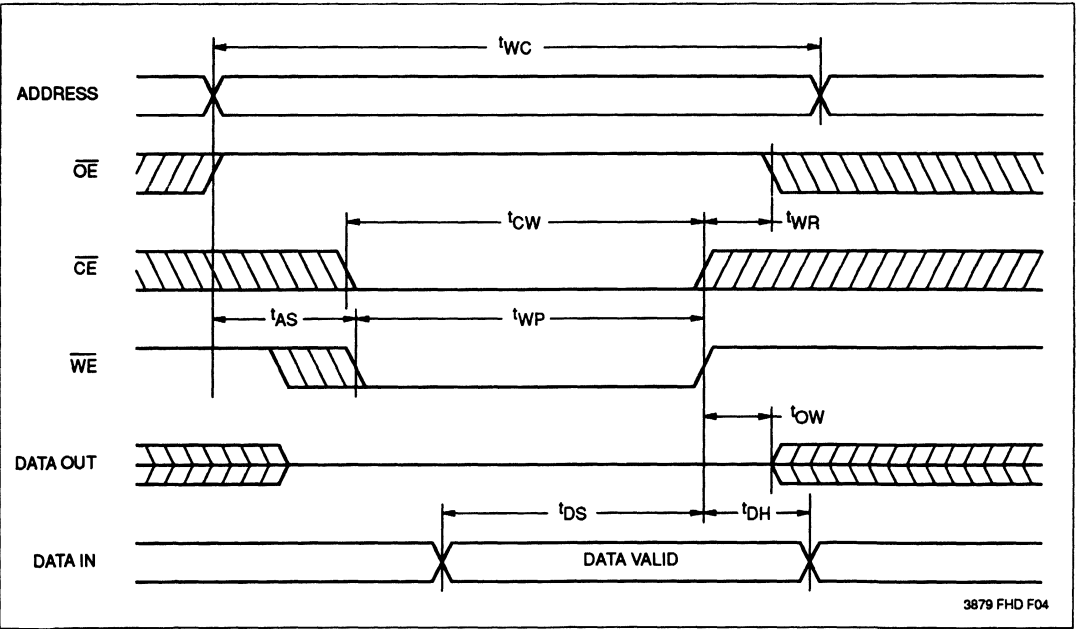
**XM20C128S**

**Write Cycle Limits**

Symbol	Parameter	Limits		Units
		Min.	Max.	
$t_{WC}$	Write Cycle Time	55		ns
$t_{WP}$	$\overline{WE}$ Pulse Width	40		ns
$t_{CW}$	$\overline{CE}$ Pulse Width	40		ns
$t_{AS}$	Address Setup	0		ns
$t_{DS}$	Data Setup	25		ns
$t_{DH}$	Data Hold	0		ns
$t_{OW}$	Output Active from End of Write		5	ns
$t_{WR}$	End of Write to Read	0		ns

3879 PGM T02

**Write Cycle Timing Diagram**



3879 FHD F04

# XM20C128S

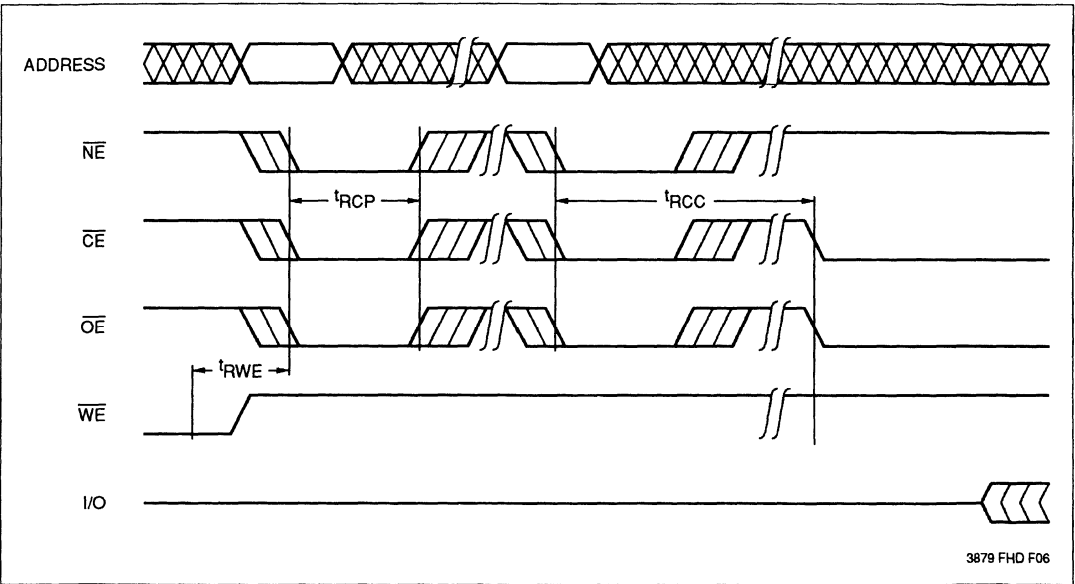
## Array Recall Timing

Symbol	Parameter	Limits		Units
		Min.	Max.	
$t_{RCC}$	Array Recall Time		10	
$t_{RCP}$	Recall Strobe Pulse Width	50		
$t_{RWE}$	Delay From $\overline{WE}$ HIGH to Recall	0		

3879 PGM T05

**Note:** The recall sequence must be repeated for each memory component individually. This is accomplished by sequencing through the Array Recall Cycle with all eight combinations of  $A_{11}$ ,  $A_{12}$  and  $A_{13}$ .

## Array Recall Cycle



# XM20C128S

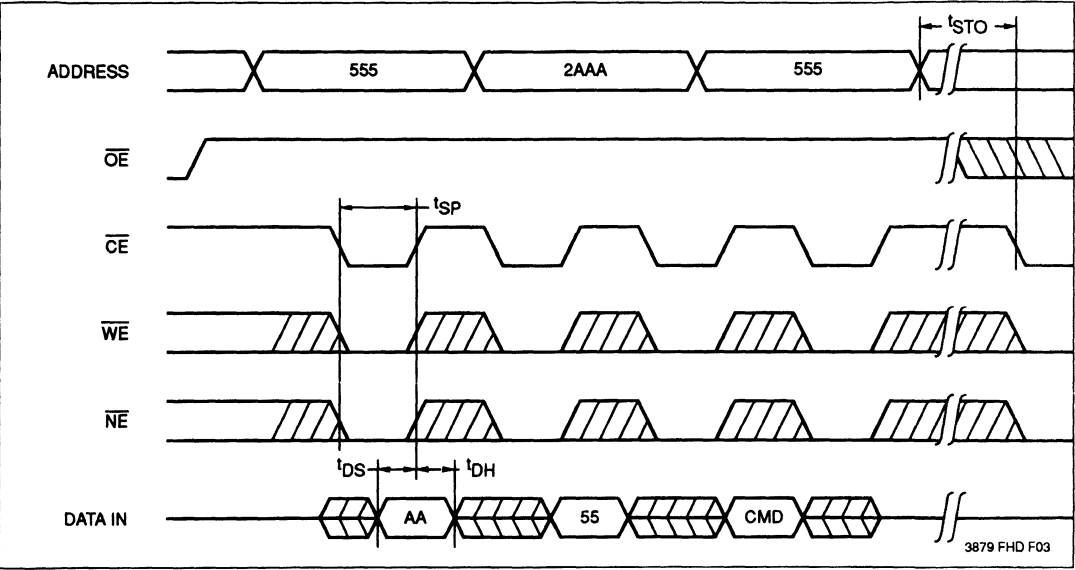
## Command Sequence Timing Limits

Symbol	Parameter	Limits		Units
		Min.	Max.	
$t_{STO}$	Store Time		5	ns
$t_{SP}$	Command Write Pulse Width	50		ns
$t_{SPH}$	Inter Command Delay	55		ns

**Note:** All write command sequence timings must conform to the standard write timing requirements.

3879 PGM T01

## Command Write Sequence



**XM20C128S**

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**NOTES**



<b>NOVRAM* Data Sheets</b>	<b>1</b>
<b>Serial Products Data Sheets</b>	<b>2</b>
<b>E<sup>2</sup>PROM Data Sheets</b>	<b>3</b>
<b>E<sup>2</sup>POT™ Data Sheets</b>	<b>4</b>
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# Xicor Military Program Overview

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## INTRODUCTION

Xicor, Inc. is committed to supplying products that meet the demands of the Military and High Reliability marketplace. Xicor's high performance Textured Poly Floating Gate (TPFG) and Direct Write cell offer an intrinsic reliability, when combined with the screening requirements of MIL-STD-883 produces an extremely enhanced product.

The Xicor Quality Assurance Program has been designed to be carried out by all employees in order to maintain the highest standards in producing these products. The backbone of the system is a self-auditing SPC program that has been implemented throughout the company. This program influences product definition, product design, testability criteria, fabrication process and final test philosophies.

Every Xicor product is designed to meet or exceed 100% functionality over the full military temperature range. This attention to detail in design has lead to the manufacture of the only floating gate 5 Volt, byte alterable memories qualified for use by the oil industry in down hole drilling operations at 170°C for both read and write operations. In addition, Xicor's continued exploitation of its proprietary TPFG technology has allowed it to maintain a generation lead in die size for all product densities.

## MIL-STD-883 and SMD Products

Xicor offers two different military category products. Most Xicor products are available with processing 100% compliant to paragraph 1.2.1 of MIL-STD-883. Secondly, a large number of products are available to the SMD (Standardized Military Drawing) program administered by DESC. These products are not only fully compliant with MIL-STD-883 but they are also screened to the electrical requirements set forth in the individual SMDs.

## ADDITIONAL DATA AND SERVICES

### Source Control Drawings

Customers may provide source control drawings for Xicor review and quotation. To reduce overall product

cost to the customer and to assure full compliance with the requirements of MIL-STD-883, Xicor will, on occasion, respond with waiver requests. Xicor must review and accept a customer source control drawing prior to acceptance of an order. Orders to SCDs must be placed directly with the factory to assure compliance. A customer may, however, purchase standard Xicor product with REFERENCE ONLY to the SCD either directly from the factory or through one of Xicor's franchised distributor locations.

### Quality Conformance Inspection Data

QCI Groups A and B are performed on each lot of devices as standard procedure for all MIL-STD-883 products. This data is available to the customer and should be requested at the time of quotation to insure its shipment with the product.

Generic QCI data for Groups C and D which qualify the product being shipped is also available.

Attributes data (copies of the the lot travelers) are also available for customer purchase. This requirement should be so noted prior order placement.

### Customer Source Inspection

Customer Source inspection may be performed at final ship point at Xicor. This requirement must be specified and quoted prior to or placement. The standard source inspection is comprised of the following:

- Group A testing: Sample size based on Table I Method 5005 MIL-STD-883, LTPD values and Table B-1 Appendix B of MIL-M-38510.
- Documentation review of all travelers, drawings and purchase orders.

The following sections contain: detailed screening and test methods performed for all MIL-STD-883 compliant products; reference tables listing compliant Xicor products, a SMD to Xicor part number cross reference table, a description of Xicor's Military Die Program and a white paper discussing the declassification procedures for Xicor's E<sup>2</sup>PROMs.

## Military Program Overview

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### MIL-STD-883 FLOWS

#### ASSEMBLY, ENVIRONMENTAL AND FINAL TEST SCREENING METHODS

Screen		Test Method	Application
Internal Visual		2010, Condition B	100%
Temperature Cycling		1010, Condition C	100%
Constant Acceleration (Centrifuge)		2001, Condition E, Y-Axis	100%
Seal:	Fine	1014, Condition A or B	100%
	Gross	1014, Condition C	100%
External Visual		2009	100%
Pre Burn-In Electricals		As Applicable	100%
Burn-In		1015, Condition D, Class B	100%
Post Burn-In and Final Electricals <sup>(1)</sup>		Per Device Data Sheet	
Static Tests		Subgroups 1, 2, 3	100%
Functional Tests		Subgroups 7, 8A, 8B	100%
Switching Tests		Subgroups 9, 10, 11	100%
Dynamic Tests		Subgroup 4 (Method 3012)	Periodically Tested
Solder Dip Lead Finish (As Applicable)		MIL-M-38510, Paragraph 3.5.6.2.1a.	100%
Seal: <sup>(2)</sup>	Fine	1014, Condition A or B	Sample
	Gross	1014, Condition C	Sample
External Visual		2009	100%
Quality Conformance Inspection <sup>(3)</sup>		5005, Class B	Sample

**Notes:** (1) Percent defective allowable (PDA) is 5% (Subgroups 1 and 7) for each lot.

(2) Sample tested in accordance with Method 5004.

(3) Sample tested in accordance with Class B requirements for Groups A, B, C and D.

# Military Program Overview

## QUALITY CONFORMANCE INSPECTIONS, METHOD 5005

The following Tables illustrate the Groups A, B, C and D Tests, Test Methods, Conditions and frequency of testing for all qualified products.

**TABLE 1. GROUP A ELECTRICAL TESTS** (Performed on each lot or subplot)

Test	Subgroup	LTPD*
Static Tests at +25°	1	116/0
Static Tests at +125°C	2	116/0
Static Tests at -55°C	3	116/0
Functional Tests at +25°C	7	116/0
Functional Tests at +125°C	8A	116/0
Functional Tests at -55°C	8B	116/0
Switching Tests at +25°C	9	116/0
Switching Tests at +125°C	10	116/0
Switching Tests at -55°C	11	116/0

**TABLE 2. GROUP B ASSEMBLY INTEGRITY TESTS** (Performed on each lot)

Test	Test Method	Conditions	LTPD
Subgroup 2 Resistance to Solvents	2015	Top and Bottom Mark	4/0*
Subgroup 3 Solderability	2003	Solder Temperature: +245°C ±5°C	10
Subgroup 5 Bond Strength	2011	Condition D	15

**TABLE 3. GROUP C DIE RELATED TESTS** (Performed periodically per MIL-STD-883, paragraph 1.2.1)

Test	Test Method	Conditions	LTPD
Subgroup 1 Steady State Lifetest Endpoint Electricals	1005	Condition D Subgroups 1, 2, 3, 7, 8, 9, 10, 11 Per Applicable Device Specification	5

\*LTPD=Quantity/Accept Number

## Military Program Overview

**TABLE 4. GROUP D PACKAGE RELATED TESTS** (Performed periodically per MIL-STD-883, paragraph 1.2.1)

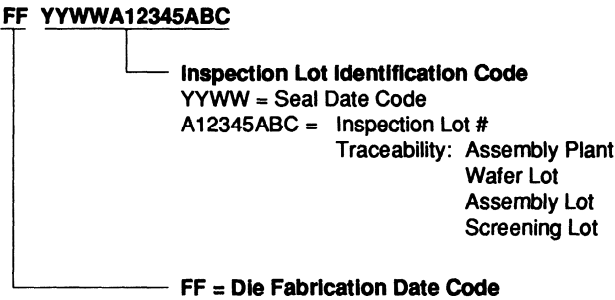
Test	Test Method	Conditions	LTPD
Subgroup 1 Physical Dimensions	2016	Per MIL-M-38510, Appendix C	15
Subgroup 2 Lead Integrity Seal: Fine Gross	2004 1014 1014	Condition B2, Lead Fatigue Condition A or B Condition C	5
Subgroup 3 Thermal Shock Temperature Cycling Moisture Resistance Endpoint Electricals Seal: Fine Gross Visual Examination	1011 1010 1004 5005 1014 1014 1010 and 1004	Condition B, 15 Cycles Condition C, 100 Cycles 10 Cycles Subgroups 1, 2, 3, 7, 8, 9, 10, 11 Condition A or B Condition C	15
Subgroup 4 Mechanical Shock Variable Frequency Vibration Constant Acceleration Seal: Fine Gross Visual Examination Endpoint Electricals	2002 2007 2001 1014 1014 1010	Condition B, 1.5 kg at 0.5 ms Condition A, 4 Cycles X, Y, & Z Condition E, 30 kg, Y1 Condition A or B Condition C  Subgroups 1, 2, 3, 7, 8, 9, 10, 11 Per Applicable Device Specification	15
Subgroup 5 Salt Atmosphere Seal: Fine Gross Visual Examination	1009 1014 1014 1009	Condition A, 24 Hours Condition A or B Condition C	15
Subgroup 6 Internal Water Vapor Content	1018	5000 ppm at 100°C	5/1*
Subgroup 7 Adhesion of Lead Finish	2025	(LTPD Applies to Leads)	15
Subgroup 8 Lid Torque	2024	Glass Frit Seal Packages Only	5/0*

\*LTPD = Quantity/Accept Number

# Military Program Overview

## TOPSIDE MARK

The topside mark of each MIL-STD-883 compliant device provides complete wafer lot, assembly and screening lot traceability. This marking appears as an alphanumeric code as shown below:



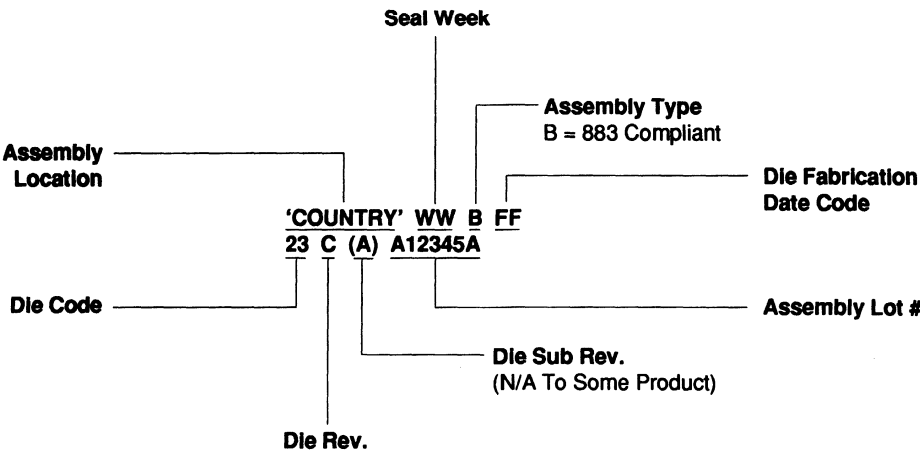
In addition, the following items will appear as part of the topside marking:

- Xicor Logo
- Xicor CAGE Code Number: 60395
- MIL-STD-883 Compliance Indicator: C
- ESD Identifier: ▽

**Notes:** On some packages, either the Xicor Logo or the CAGE Code number will appear, but not both.

## BACKSIDE MARK

The backside mark provides wafer lot and assembly lot traceability. This appears in an alphanumeric code as follows:



## Military Program Overview

### MIL-STD-883 PRODUCT LISTING

Xicor Part Number	Organization	Speeds*	Package Style and Lead/Pin/PAD Count				SMD Number	Page Number
			CERDIP	LCC	FLATPACK	PGA		
NOVRAMs								
X22C10	64 x 4	120ns	18				TBD	1-1
X22C12	256 x 4	120ns	18				TBD	1-9
X20C04	512 x 8	200ns	28	32			TBD	1-17
X20C05	512 x 8	35ns	28	32			TBD	1-27
X20C16	2K x 8	35ns	28	32			TBD	1-41
Serial NOVRAMs								
X24C44	16 x 16	0-1MHz	8				TBD	2-1
X24C45	16 x 16	0-1MHz	8				TBD	2-13
Serial E <sup>2</sup> PROMs								
X24C02	256 x 8	0-100KHz	8				TBD	2-71
X24C04	512 x 8	0-100KHz	8				5962-89590	2-95
X24C16	2K x 8	0-100KHz	8				5962-89667	2-131
E <sup>2</sup> POT Digitally Controlled Potentiometer								
X9CMME			8				TBD	4-1
5 Volt, Byte Alterable E <sup>2</sup> PROMs								
X2816C	2K x 8	90-200ms	24	32			TBD	3-1
X28C64	8K x 8	150-250ns	28	32	28	28	5962-87514	3-45
X28HC64	8K x 8	55-120ns	28	32	28	28	TBD	3-61
X28C256	32K x 8	150-300ns	28	32	28	28	5962-88525	3-77
X28HC256	32K x 8	70-120ns	28	32	28	28	5962-88634	3-93
X28TC256	32K x 8	35-55ns	28	32			TBD	3-125
X28C512	64K x 8	120-250ns	32	32	32	36	5962-90869	3-127
X28C513	64K x 8	120-250ns		32			5962-90869	3-127
X28C010	128K x 8	120-250ns	32	32	32	36	5962-38267	3-143
Microcontroller Peripheral Memory								
X88C64	8K x 8	120ns					TBD	5-1

\* Speeds for parallel access devices is tAA in ns; for serial devices speed is min. to max. clock rate in Hz.

**Military Program Overview**

**Standardized Military Drawing (SMD)  
Numeric Cross Reference Guide**

SMD Number	MIL-STD-883 Part Number	Package Style	Page Number	Product Description
5962-3826701 MUX <sup>1</sup>	X28C010EMB-25	32 LCC	3-143	128K x 8 5 Volt Byte Alterable E <sup>2</sup> PROM
5962-3826701 MXX	X28C010DMB-25	32 CERDIP	3-143	
5962-3826701 MZX	X28C010FMB-25	32 FLATPACK	3-143	
5962-3826703 MUX	X28C010EMB-20	32 LCC	3-143	
5962-3826703 MXX	X28C010DMB-20	32 CERDIP	3-143	
5962-3826703 MZX	X28C010FMB-20	32 FLATPACK	3-143	
5962-3826705 MUX	X28C010EMB-15	32 LCC	3-143	
5962-3826705 MXX	X28C010DMB-15	32 CERDIP	3-143	
5962-3826705 MZX	X28C010FMB-15	32 FLATPACK	3-143	
5962-3826707 MUX	X28C010EMB-12	32 LCC	3-143	
5962-3826707 MXX	X28C010DMB-12	32 CERDIP	3-143	
5962-3826707 MZX	X28C010FMB-12	32 FLATPACK	3-143	
5962-8751403 XX	X28C64DMB-25	28 CERDIP	3-45	8K x 8 5 Volt Byte Alterable E <sup>2</sup> PROM
5962-8751403 YX	X28C64EMB-25	32 LCC	3-45	
5962-8751403 ZX	X28C64FMB-25	28 FLATPACK	3-45	
5962-8751404 XX	X28C64DMB-20	28 CERDIP	3-45	
5962-8751404 YX	X28C64EMB-20	32 LCC	3-45	
5962-8751404 ZX	X28C64FMB-20	28 FLATPACK	3-45	
5962-8751405 XX <sup>2</sup>	X28C64DMB-25	28 CERDIP	3-45	
5962-8751405 YX <sup>2</sup>	X28C64EMB-25	32 LCC	3-45	
5962-8751405 ZX <sup>2</sup>	X28C64FMB-25	28 FLATPACK	3-45	

1. UX = 32 PAD LCC for the 1Mbit Device  
2. These devices are screened for 100,000 write cycle endurance

LEGEND - SMD SUFFIX	
M = MIL-STD-883	XX = CERDIP
PX = CERDIP (8 Lead)	YX = LCC
UX = PGA	ZX = FLATPACK
VX = CERDIP (18 Lead)	



## Military Program Overview

### STANDARDIZED MILITARY DRAWING (SMD) NUMERIC CROSS REFERENCE GUIDE (Continued)

SMD Number	MIL-STD-883 Part Number	Package Style	Page Number	Product Description
5962-8852502 UX	X28C256KMB	28 PGA	3-77	<b>32K x 8 5 Volt Byte Alterable E<sup>2</sup>PROM</b>
5962-8852502 XX	X28C256DMB	28 CERDIP	3-77	
5962-8852502 YX	X28C256EMB	32 LCC	3-77	
5962-8852502 ZX	X28C256FMB	28 FLATPACK	3-77	
5962-8852503 UX	X28C256KMB-25	28 PGA	3-77	
5962-8852503 XX	X28C256DMB-25	28 CERDIP	3-77	
5962-8852503 YX	X28C256EMB-25	32 LCC	3-77	
5962-8852503 ZX	X28C256FMB-25	28 FLATPACK	3-77	
5962-8852504 UX	X28C256KMB-20	28 PGA	3-77	
5962-8852504 XX	X28C256DMB-20	28 CERDIP	3-77	
5962-8852504 YX	X28C256EMB-20	32 LCC	3-77	
5962-8852504 ZX	X28C256FMB-20	28 FLATPACK	3-77	
5962-8852505 UX <sup>3</sup>	X28C256KMB-25	28 PGA	3-77	
5962-8852505 XX <sup>3</sup>	X28C256DMB-25	28 CERDIP	3-77	
5962-8852505 YX <sup>3</sup>	X28C256EMB-25	32 LCC	3-77	
5962-8852505 ZX <sup>3</sup>	X28C256FMB-25	28 FLATPACK	3-77	
5962-8852506 UX	X28C256KMB-15	28 PGA	3-77	<b>32K x 8 5 Volt Byte Alterable E<sup>2</sup>PROM</b>
5962-8852506 XX	X28C256DMB-15	28 CERDIP	3-77	
5962-8852506 YX	X28C256EMB-15	32 LCC	3-77	
5962-8852506 ZX	X28C256FMB-15	28 FLATPACK	3-77	
5962-8863401 UX	X28HC256KMB-12	28 PGA	3-93	
5962-8863401 XX	X28HC256DMB-12	28 CERDIP	3-93	
5962-8863401 YX	X28HC256EMB-12	32 LCC	3-93	
5962-8863401 ZX	X28HC256FMB-12	28 FLATPACK	3-93	
5962-8863403 UX	X28HC256KMB-90	28 PGA	3-93	
5962-8863403 XX	X28HC256DMB-90	28 CERDIP	3-93	
5962-8863403 YX	X28HC256EMB-90	32 LCC	3-93	
5962-8863403 ZX	X28HC256FMB-90	28 FLATPACK	3-93	
5962-8959001 PX	X24C04DMB	8 CERDIP	2-95	<b>512 x 8 Serial E<sup>2</sup>PROM</b>
5962-8966701 PX	X24C16DMB	8 CERDIP	2-131	<b>2K x 8 Serial E<sup>2</sup>PROM</b>

3. These devices are screened for 100,000 write cycle endurance

#### LEGEND - SMD SUFFIX

M = MIL-STD-883	XX = CERDIP
PX = CERDIP (8 Lead)	YX = LCC
UX = PGA	ZX = FLATPACK
VX = CERDIP (18 Lead)	

# Military Program Overview

STANDARDIZED MILITARY DRAWING (SMD) NUMERIC CROSS REFERENCE GUIDE (Continued)

SMD Number	MIL-STD-883 Part Number	Package Style	Page Number	Product Description
5962-9086901 MUX	X28C512KMB-25	36 PGA	3-127	64K x 8 5 Volt Byte Alterable E <sup>2</sup> PROM
5962-9086901 MXX	X28C512DMB-25	32 CERDIP	3-127	
5962-9086901 MYX	X28C512EMB-25	32 LCC	3-127	
5962-9086901 MZX	X28C512FMB-25	32 FLATPACK	3-127	
5962-9086902 MUX <sup>4</sup>	X28C512KMB-25	36 PGA	3-127	
5962-9086902 MXX <sup>4</sup>	X28C512DMB-25	32 CERDIP	3-127	
5962-9086902 MYX <sup>4</sup>	X28C512EMB-25	32 LCC	3-127	
5962-9086902 MZX <sup>4</sup>	X28C512FMB-25	32 FLATPACK	3-127	
5962-9086903 MUX	X28C512KMB-20	36 PGA	3-127	
5962-9086903 MXX	X28C512DMB-20	32 CERDIP	3-127	
5962-9086903 MYX	X28C512EMB-20	32 LCC	3-127	
5962-9086903 MZX	X28C512FMB-20	32 FLATPACK	3-127	
5962-9086904 MUX <sup>4</sup>	X28C512KMB-20	36 PGA	3-127	
5962-9086904 MXX <sup>4</sup>	X28C512DMB-20	32 CERDIP	3-127	
5962-9086904 MYX <sup>4</sup>	X28C512EMB-20	32 LCC	3-127	
5962-9086904 MZX <sup>4</sup>	X28C512FMB-20	32 FLATPACK	3-127	
5962-9086905 MUX	X28C512KMB-15	36 PGA	3-127	
5962-9086905 MXX	X28C512DMB-15	32 CERDIP	3-127	
5962-9086905 MYX	X28C512EMB-15	32 LCC	3-127	
5962-9086905 MZX	X28C512FMB-15	32 FLATPACK	3-127	
5962-9086906 MUX <sup>4</sup>	X28C512KMB-15	36 PGA	3-127	
5962-9086906 MXX <sup>4</sup>	X28C512DMB-15	32 CERDIP	3-127	
5962-9086906 MYX <sup>4</sup>	X28C512EMB-15	32 LCC	3-127	
5962-9086906 MZX <sup>4</sup>	X28C512FMB-15	32 FLATPACK	3-127	
5962-9086907 MUX	X28C512KMB-12	36 PGA	3-127	
5962-9086907 MXX	X28C512DMB-12	32 CERDIP	3-127	
5962-9086907 MYX	X28C512EMB-12	32 LCC	3-127	
5962-9086907 MZX	X28C512FMB-12	32 FLATPACK	3-127	
5962-9086908 MUX <sup>4</sup>	X28C512KMB-12	36 PGA	3-127	
5962-9086908 MXX <sup>4</sup>	X28C512DMB-12	32 CERDIP	3-127	
5962-9086908 MYX <sup>4</sup>	X28C512EMB-12	32 LCC	3-127	
5962-9086908 MZX <sup>4</sup>	X28C512FMB-12	32 FLATPACK	3-127	
5962-9086909 MYX	X28C513EMB-25	32 LCC	3-127	
5962-9086910 MYX <sup>4</sup>	X28C513EMB-25	32 LCC	3-127	
5962-9086911 MYX	X28C513EMB-20	32 LCC	3-127	
5962-9086912 MYX <sup>4</sup>	X28C513EMB-20	32 LCC	3-127	
5962-9086913 MYX	X28C513EMB-15	32 LCC	3-127	
5962-9086914 MYX <sup>4</sup>	X28C513EMB-15	32 LCC	3-127	
5962-9086915 MYX	X28C513EMB-12	32 LCC	3-127	
5962-9086916 MYX <sup>4</sup>	X28C513EMB-12	32 LCC	3-127	

4. Write Cycle Time = 5ms

## **Military Program Overview**

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NOTES



## Military Die Products Program

### FEATURES

- High Performance Advanced CMOS Technology
- 0°C to 70°C Operating Temperature
- 100 Year Data Retention
- 95% Yield Excluding Assembly Related Losses
- Commercial Data Sheet Parameters (except input levels)
- Die Visually Inspected to MIL-STD-883, T/M 2010 Condition B
- Optional Die Element Evaluation per MIL-STD-883, T/M 5008

### DESCRIPTION

Xicor die products are fabricated with Xicor's Advanced CMOS Floating Gate technology. Like all Xicor programmable nonvolatile memories, they are 5V only devices.

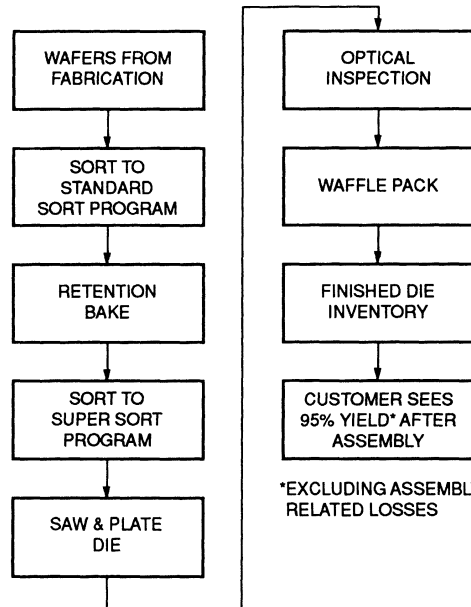
Xicor die products are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

Products to be shipped in die form follow the flow shown below. This insures a 95% yield (excluding assembly related losses) to the commercial data sheet. The slowest datasheet access time is guaranteed. All A.C. parameters and D.C. parameters except input and output voltages are guaranteed.

For military applications, Xicor now offers die with element evaluation testing per MIL-STD-883. A description of the element evaluation testing can be found on the following page.

Bonding diagrams, die size/thickness and other information required for use of die can be obtained from your local Xicor sales representative.

### TEST FLOW



\*EXCLUDING ASSEMBLY RELATED LOSSES

## Military Die Products Program

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### DIE ELEMENT EVALUATION

Test samples shall be taken from the same wafer lot as the production die, assembled and tested to the die element evaluation as specified in paragraph 3.2 of Test Method 5008, MIL-STD-883, Class B.

Subgroup	Test	Test Method	Quantity (Accept No.)
1	Internal Visual	2010, Condition B	10 (0)
2	Final Electricals <sup>(1)</sup>	Per Applicable Device Specification	10 (1)
3	Wire Bond Evaluation	2011, Condition C or D	10 (0) wires or 20 (1) wires

**Notes:** (1) Final Electricals to be performed at customer's specified temperature range.

### DIE ORDERING INFORMATION

When ordering, please specify die in waffle pack or die in wafer form.

Part number suffix:     H = Die in waffle pack  
                                  W = Die in wafer form

## Declassification Procedures For Xicor 5 Volt Only E<sup>2</sup>PROMs

Richard Palm and Cliff Zittlaw

### INTRODUCTION

With their introduction into the market place, 5 volt only E<sup>2</sup>PROMs were quickly designed into many military electronics systems. They provided a mechanism for easily updating data bases and software programs without the requisite board removal and component changes associated with other nonvolatile semiconductor memories. Because the E<sup>2</sup>PROMs might contain classified data, many OEMs were required to provide a means of erasure.

This paper will review the basics of the technology, two techniques employed for chip declassification and a complete description of Xicor's declassification experiments and results will be reviewed.

### DEVICE OPERATION

Xicor E<sup>2</sup>PROMs employ Fowler-Nordheim tunneling to transfer charge onto or off of a floating gate. The voltages required to transfer charge are generated on-board the device.

Figure 1 is a cut away view of the cell structure. Poly 1 acts as both the cell ground isolation transistor and programming cathode; Poly 2 is the floating gate; and Poly 3 acts as both the select word line transistor and

erase tunnel anode. Poly 2 is totally surrounded by an oxide electrically isolating it from all other device structures. Its channel region acts as both the floating gate charge-conditional current path for reading and the data conditional current path for writing.

A schematic representation is illustrated in Figure 2. Because the construction of the cell incorporates the poly 1 to 2 programming and poly 2 to 3 erase tunneling elements in a single structure, data storage is a direct, single pass operation, involving the following sequence. First the poly 1 line, common to the entire array, is brought low, cutting off the conduction path from bit line through the cell to array ground. Next, the bit lines are set up to either 0V for an erase operation or about 16V for a program operation. The poly 3 word line is ramped up to about 22V in 1ms to drive the nonvolatile charge transport. To erase, the bit line is grounded, whereupon the channel voltage under poly 2 capacitively steers the floating gate towards ground. This induces sufficient voltage across the poly 3/2 tunneling element to remove electrons from the floating gate. When the bit line is high for programming, the channel potential steers the floating gate positively. This induces sufficient voltage across the poly 2/1 tunneling element to inject electrons onto the floating gate.

7

Figure 1. Cell Cross Section

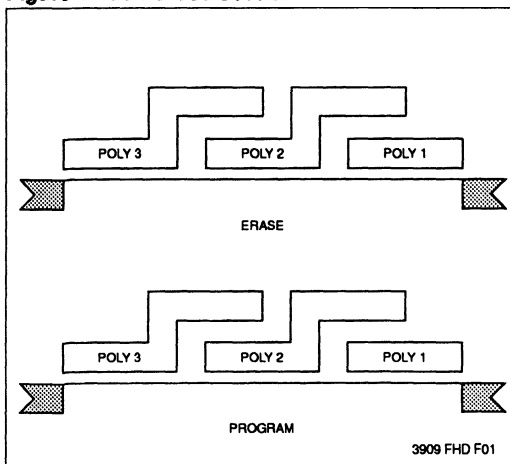
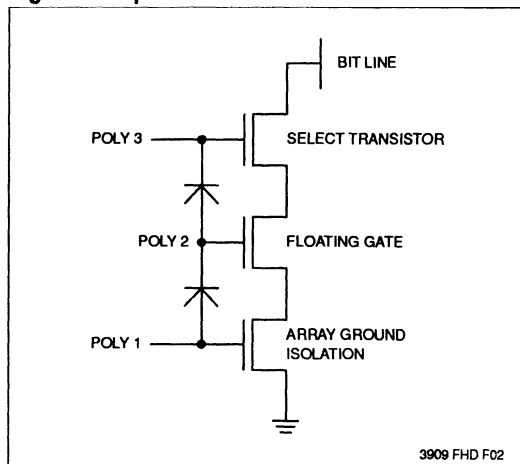


Figure 2. Equivalent Cell Circuit



## Declassification Procedures for Xicor 5 Volt Only E<sup>2</sup>PROMs

During tunneling, charge will be trapped in the interpoly oxides. This trap-up is caused by the accumulation of trapped negative charge in the dielectric due to the repeated passage of current. These charges create a potential which is additive and opposite to that of the floating gate.

The basic cell operation and description of charge trap in the dielectric is fundamental background for understanding the experiments described in later sections. For detailed descriptions of device operation and endurance in floating gate memories refer to Xicors 1988 Data Book.

### First Generation Chip Clear Techniques

E<sup>2</sup>PROMs require a relatively long period of time to program/erase data on the floating gate. The maximum time generally specified for the first generation devices (X2816A) was 10ms per byte. In a manufacturing/test environment each byte must be programmed and verified with multiple patterns at all  $V_{CC}$  limits and temperature limits. With the X2816A, a 2K x 8 device, one rewrite of the entire array would take approximately 20 seconds. When multiplied times all the test variables, the test time would begin to take minutes per device.

In order to reduce test times most manufacturers incorporated test modes whereby the entire array could be erased (changed to all 1s) or programmed (changed to all 0s) in a single 10ms cycle.

This operation for Xicor devices is performed by raising the  $\overline{OE}$  input to  $V_{OE}$  (a voltage higher than  $V_{CC}$ ), setting the I/Os to a specified TTL level and strobing the  $\overline{WE}$  and  $\overline{CE}$  inputs LOW. This whole operation is similar to a standard write operation with the exception of  $V_{OE}$ .

It should be noted that  $V_{OE}$  is not coupled into the device. The high voltage on  $\overline{OE}$  is detected by the input circuitry and conditions the internal logic for a chip mode operation (sometimes referred to as block mode or mass mode). The high voltage required for tunneling is generated by the device's on-board charge pumps.

The timing diagrams and input level requirements were shared with the OEMs requiring these functions. The chip erase (not chip program) function was subsequently specified on various Standardized Military Drawings and slash sheets; thereby, becoming de facto standard features.

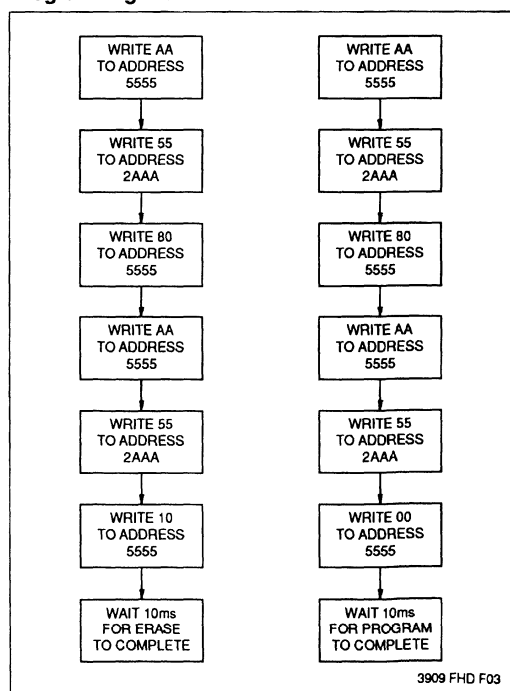
### Second Generation Chip Clear Techniques

The X28256 was the first device to employ software data protection. This feature was developed to eliminate the most common design problem encountered with 5 volt only nonvolatile memories, inadvertent writes during power-up/-down cycling. During power transitions, positive control of E<sup>2</sup>PROM inputs cannot always be guaranteed before system stabilization. This can lead to inadvertently generating write conditions to the E<sup>2</sup>PROMs, resulting in corrupted data.

Based on Xicor's experience in resolving these system design issues, the company implemented software data protection. When employed by the end user, the device will ignore all attempts to write unless a specific three byte command sequence is issued (refer to Xicor Data Book).

Expanding on the three byte command sequence, Xicor implemented 5 volt only chip erase and chip program algorithms that may be employed to completely erase or program the device in a single 10ms operation. This is illustrated in Figure 3.

**Figure 3. 5 Volt Only Chip Erase and Chip Program Algorithm**



## Declassification Procedures for Xicor 5 Volt Only E<sup>2</sup>PROMs

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### Classified Erase Experiment

Recently a number of our customers have requested data regarding the effectiveness of the chip erase modes. Their contractual requirements have specified declassification procedures that do not specifically encompass E<sup>2</sup>PROMs. The declassification procedures default to those reserved for ferrite core memories. This requires a minimum 100 erase/program cycles for secret and below data and a minimum 1000 erase/program cycles for top secret data.

In certain applications where data has to be declassified on a daily basis or end of work shift basis, the specified procedures would predominate over actual useful data writes as the end of life endurance mechanism.

Intuitively we understood the requirements to be far in excess of actual need. From daily test operation it was evident that after a chip erase or program operation the contents would be read back as all 1s or all 0s under normal operating conditions.

In order to prove no "residual" data could be read out under any conditions, Xicor proceeded with a study: first, to determine if there was a method of data recovery; secondly, if there was recoverable data, what was the optimum method of declassification.

### Background

The tests performed for this report were done with the full knowledge of the device's internal and external operating characteristics, including all the device's proprietary test modes. Once the device is fully erased or programmed in a single pass there is no known method of scanning the die in a non-intrusive manner to detect latent or residual data patterns. Therefore a method had to be found which would make a read operation most sensitive to floating gate charge or other residual charge which might be a result of previously stored data.

### Reading Data

A highly sensitive method of reading needed to be found to insure the results of the experiment were valid. The X28C256 has a proprietary test mode which allows measurement of individual cell currents. During the experiments, cell currents were recorded after declassification and downloaded to a computer. The data were passed through a software filter that emulated a self centering sense amplifier, approximately three times more sensitive than the on-chip sense amplifier.

### Figure of Merit

A figure of merit rating was employed to determine the effectiveness of declassification tests. The figure of merit was derived by exclusive or'ing the erased pattern with the original pattern and summing the result over the array. This number is then divided by the total number of bits to give a figure of merit. A figure of 0.5 would mean the data has been totally scrambled, while less than 0.5 would mean the complement data is appearing, and for more than 0.5 would mean the original data is appearing. For example 0.8 means that 20% of the bits are randomly different from the original pattern. Therefore, a figure of merit of 0.5 would be the ideal result.

### Moving Address Pattern

A moving address pattern was employed to eliminate any potential misinterpretation of data due to the physical proximity of cells to ground planes or voltage lines.

### The Experiments

It was well known that under normal device operation, randomly changing the data pattern on a regular basis or infrequently performing software updates, a single chip erase operation would be sufficient to insure no data could be recovered. Therefore, based on knowledge of the device a worst case experiment was developed. Worst case would be iteratively writing the same data pattern to the device, maximizing traps in the interpoly oxides. It was known that latent charge (or lack of charge) on the floating gate after erasure would not be detectable, but the traps might modify the local electric fields enough to be detectable under laboratory conditions.

### Experiment #1. Gathering A Baseline

The tests were originally performed on units provided from production after basic go/no-go tests without full screening. The test consisted of writing the moving address pattern to the device 4,000 times without any intervening pattern being written. After a single pass chip erase (all 1's) and chip program (all 0's) in the 5 volt only mode, the pattern was not detectable when reading under normal operating conditions. However, by employing the proprietary test mode under an extreme voltage condition on V<sub>CC</sub> and using the computer analysis tool a latent pattern could be detected with a figure of merit of 0.79. This was not a read of the floating gate charge, but a detection of the traps caused by the iterative writing of the same pattern.



## Declassification Procedures for Xicor 5 Volt Only E<sup>2</sup>PROMs

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### Experiment #2. Impact Of Standard Screening

The experiment was then continued to determine the effect of standard production precycling. This precycling is normally performed to screen infant mortality failures prior to shipment. The screen is repetitive erase/program cycles which would cause trap-up. Trapping is logarithmic; therefore, after precycling any additional writing would not add many traps, reducing the likelihood of data recovery.

After precycling, the devices were cycled 4,000 times with the moving address pattern. This was followed by five 5 volt only erase/program cycles, yielding a read back figure of merit of 0.53 under the special test conditions.

### Experiment #3. Impact Of High Temperature During Declassification

In this experiment, devices were subjected to 2000 cycles of the same moving address pattern. 5 volt only erase and program was performed at + 125C with the following results:

	Figure of Merit
Erase 1	.57
Program1	.55
Erase 2	.52
Program2	.52

### Experiment #4. Chip Erase Only As A Means Of Declassification

Additional units were cycle 100,000 times with the moving address pattern. These units were then subjected to 5 volt only chip erasure. The results are as follows:

	Figure of Merit
Erase 1	.59
Erase 2	.55
Erase 3	.53

**Recommendations**—In most applications a single erase operation is sufficient, in worst case applications three to five erase/program cycles will render the data totally unrecoverable. Below are application examples and recommended methods of declassification.

**Data logging**—where monitored data are stored in sequential fashion as the data are generated. This is generally done by simply incrementing the address for each new data to be stored; when reaching the end of the allocated memory space recording begins at address zero. Single chip erase cycle (10ms) or single chip erase/program cycle (20ms).

**Program storage**—where the program is updated infrequently with data changing in a random manner. Single chip erase cycle (10ms) or a single chip erase/program cycle (20ms).

**Program storage**—where the data are frequently updated but only the data actually changed is being rewritten. Single chip erase cycle (10ms) or a single chip erase/program cycle (20ms).

**Program storage**—where the data are frequently updated, most of the data is unchanged and all addresses are rewritten for each update.

- Perform a single erase/program cycle prior to each update. Then for declassification a single chip erase/program cycle (20ms) would be required.
- If data are loaded at beginning of each work shift and data then declassified at end of each work shift; perform end of shift declassification utilizing a single chip erase/program cycle (20ms).
- If data are frequently updated with no intervening erase/program cycles then declassify with three chip erase/program cycles (100ms).

Any inquiries regarding this paper should be made to:

**Xicor Military Marketing Department**  
**851 Buckeye Court**  
**Milpitas, CA 95035**  
Phone: (408) 432-8888

# Declassification Procedures for Xicor 5 Volt Only E<sup>2</sup>PROMs

**Footnote:**

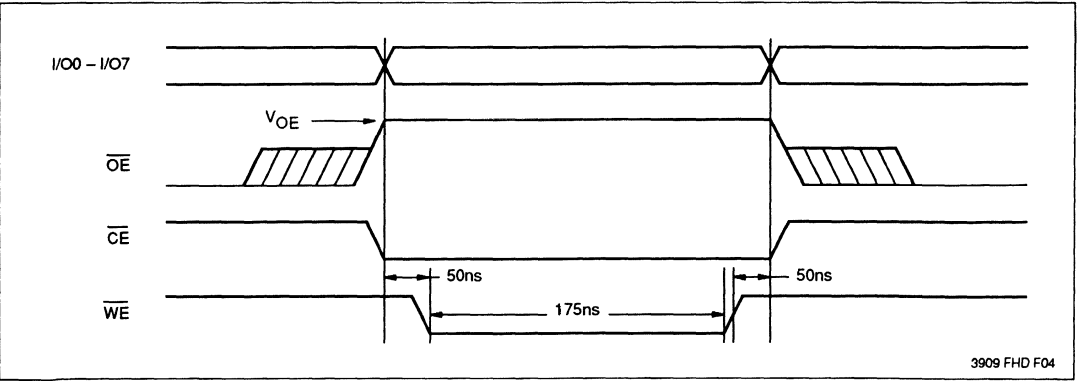
This report has shown the effectiveness of the 5 volt only Classified Erase Algorithm under various applications conditions. Because the internal mechanism is identical for the V<sub>OE</sub> operating mode, the conclusions are valid for its use also.

It should be noted for applications where neither 5 volt only erase/program nor the V<sub>OE</sub> method of erase/program are suitable; writing all 1's in either byte or pag emode is equivalent to a chip erase operation and writing all 0's is equivalent to a chip program operation.

Below is a cross matrix table indicating by product the method of chip erase/program employed. Where V<sub>OE</sub> mode is defined the V<sub>OE</sub> voltage and I/O conditions required are also defined.

Xicor Device	V <sub>OE</sub> Chip Mode			5Volt Only Mode Available
	V <sub>OE</sub>	I/O State for Program	I/O State for Erase	
X2816B	20V	00	FF	NO
X28C64	14V	00	FF	Yes
X28HC64	14V	00	FF	Yes
X28C256	14V	00	FF	Yes
X28HC256	14V	00	FF	Yes
X28VC256	14V	00	FF	Yes
X28C512	14V	00	FF	Yes
X28C010	14V	00	FF	Yes

**Figure 4. Universal V<sub>OE</sub> Chip Mode Waveforms**



Individual device timing requirements are available from Xicor. Address states are "don't care" for this operation. Once initiated, the operation (either chip erase or chip program) is self-timed and will complete within 10ms.

**Ordering Information**

The required mode of declassification must be stated prior to ordering the applicable Xicor MIL-STD-883 device. Xicor does not guarantee declassification on "off-the-shelf" MIL-STD-883 product.

Please contact your local Xicor Sales Office for availability and ordering information.

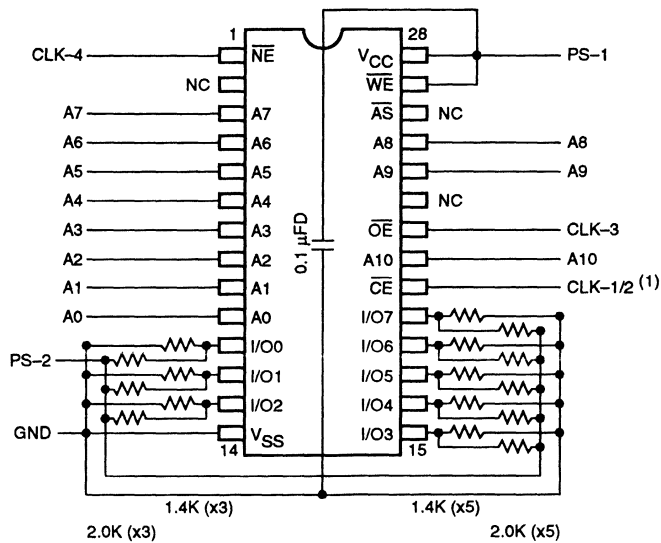
## **Declassification Procedures for Xicor 5 Volt Only E<sup>2</sup>PROMs**

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NOTES

# Military Product Burn-in Circuits and Timing

**Figure 1. X20C04, X20C05, X20C16 Burn-In Circuit**



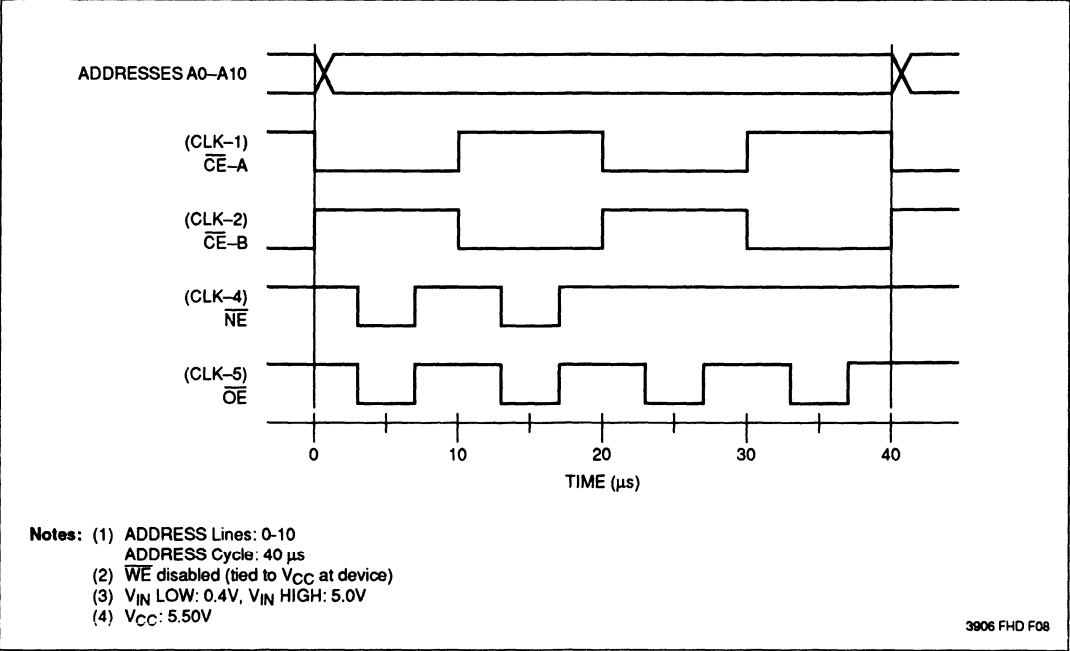
- Notes:** (1) CLK-1: Rows 1, 3, 5... (odd rows  $\overline{CE}$ -A)  
 CLK-2: Rows 2, 4, 6... (even rows  $\overline{CE}$ -B)  
 CLK-2 =  $\overline{CLK}$ -1  
 (2)  $\overline{WE}$  (Pin 27) must be hardwired to  $V_{CC}$  (Pin 28) at device as shown.  
 (3) I/O Pull Up: 2.0 K ohms, I/O Pull Down: 1.4 K ohms  
 (4) All Resistors: 1% Metal Film, 1/4 Watt  
 (5) Pin 24 (A9) and Pin 25 (A10) are no connects on the X20C04 and X20C05.  
 (6) Pin 26 ( $\overline{AS}$ ) is a no connect on the X20C04.

3906 FHD F01



# Military Product Burn-In Circuits and Timing

Figure 3. X20C04, X20C05, X20C16 Burn-In Timing



# Military Product Burn-in Circuits and Timing

Figure 4. X22C10, X22C12 Burn-In Circuit

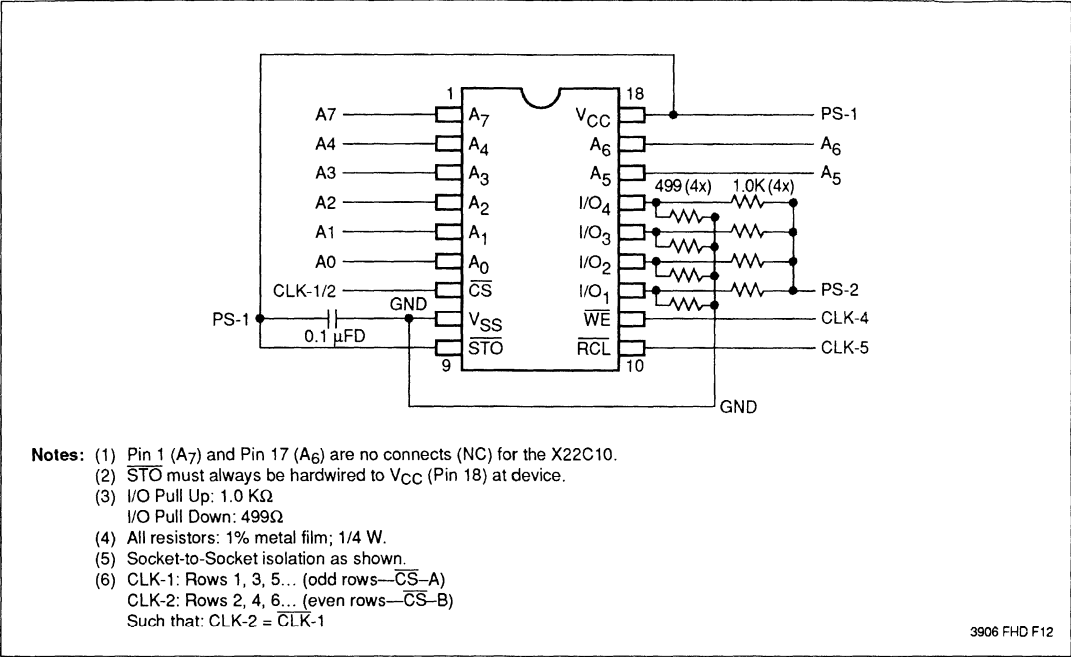
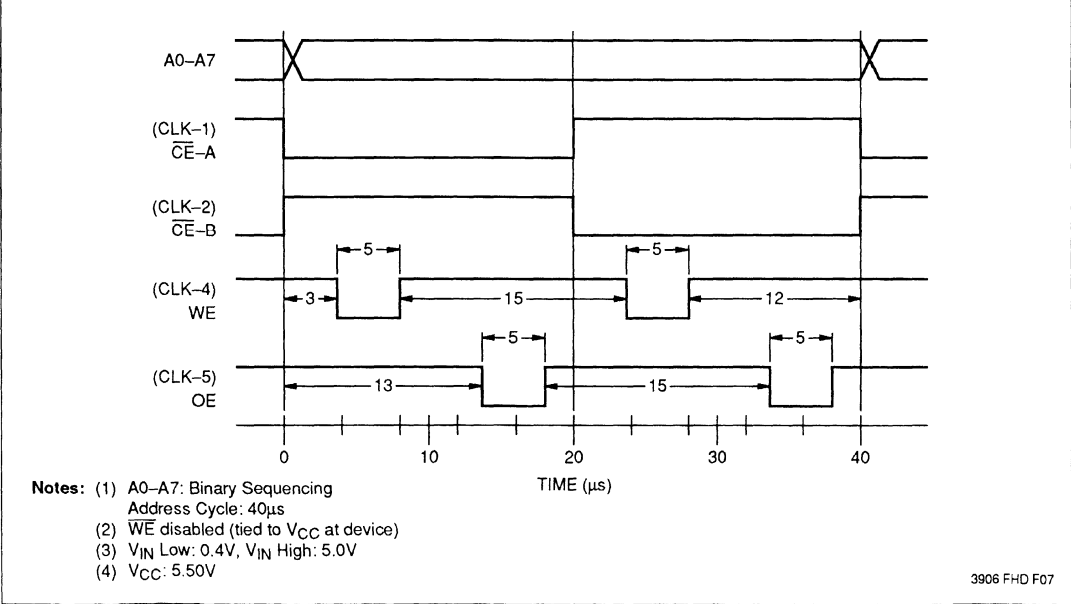


Figure 5. X22C10, X22C12 Burn-In Timing



# Military Product Burn-in Circuits and Timing

Figure 6. X24C02, X24C04, X24C16 Burn-In Circuit

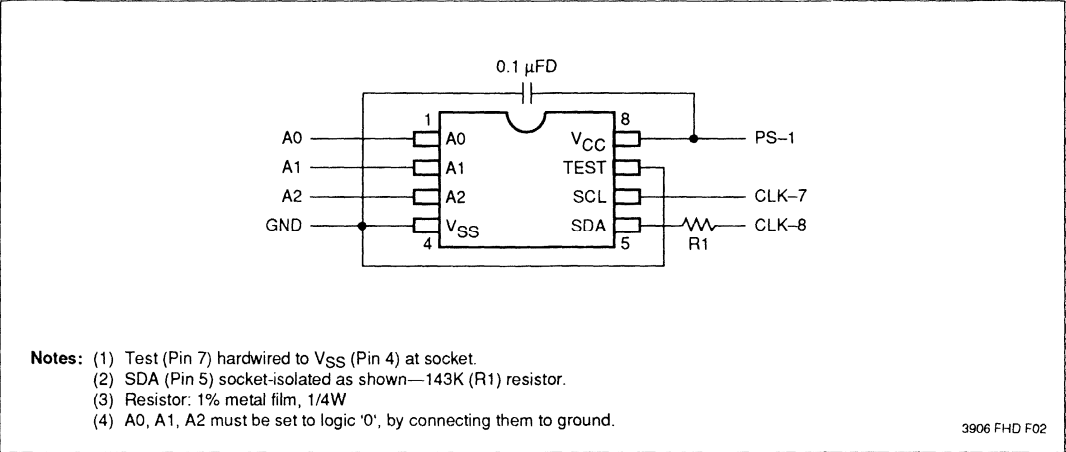
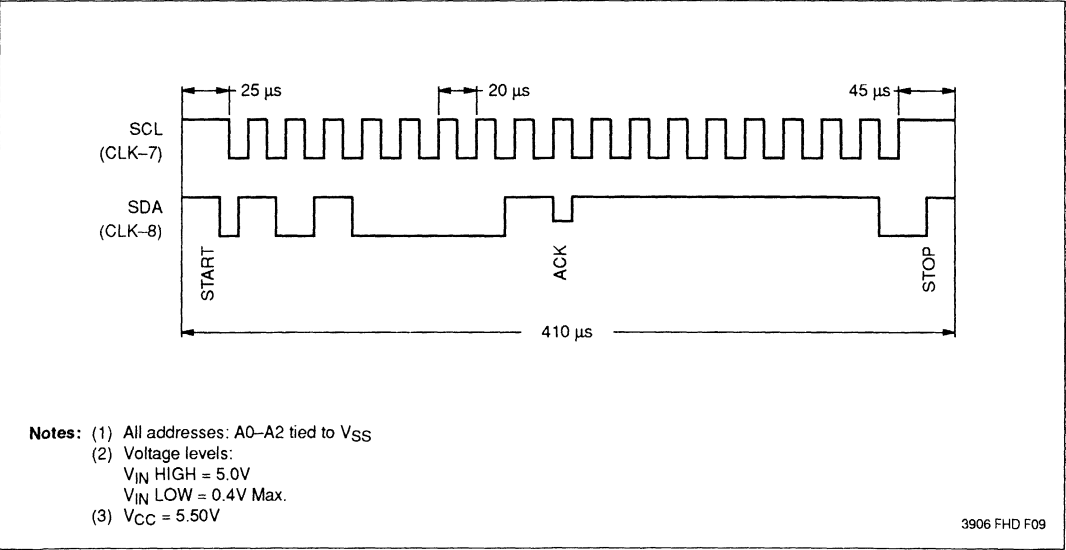


Figure 7. X24C02, X24C04, X24C16 Burn-In Timing





## Military Product Burn-in Circuits and Timing

Figure 8. X24C44 and X24C45 Burn-In Circuit

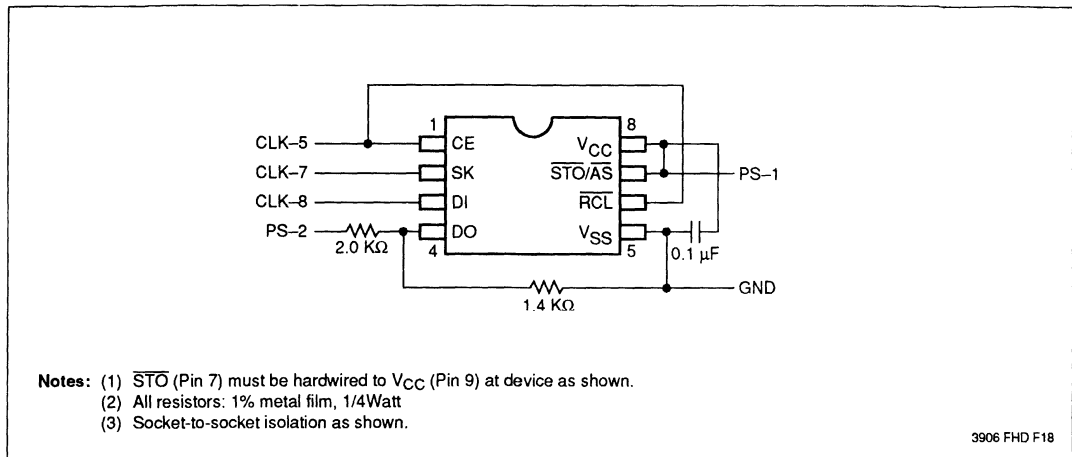
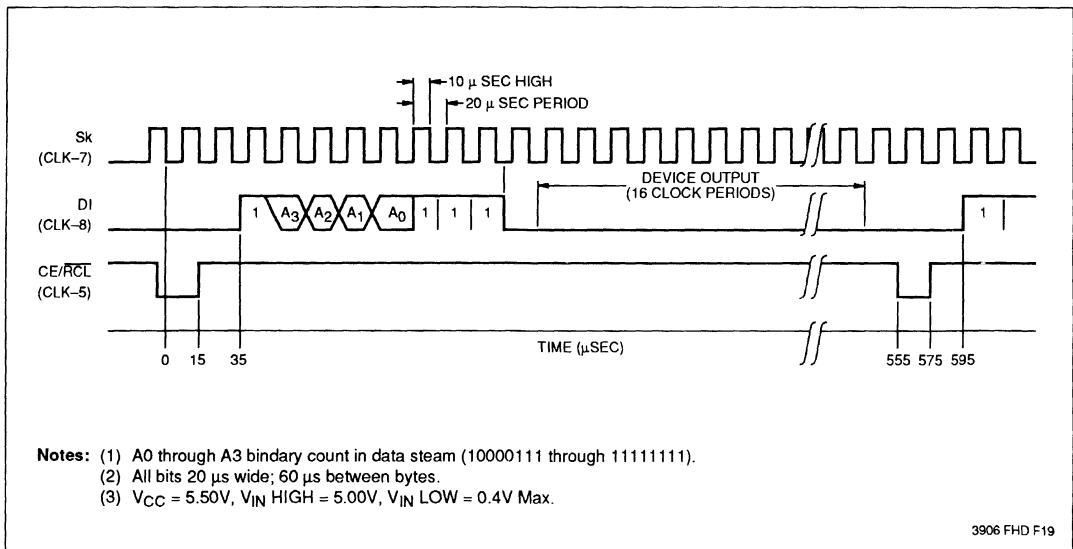
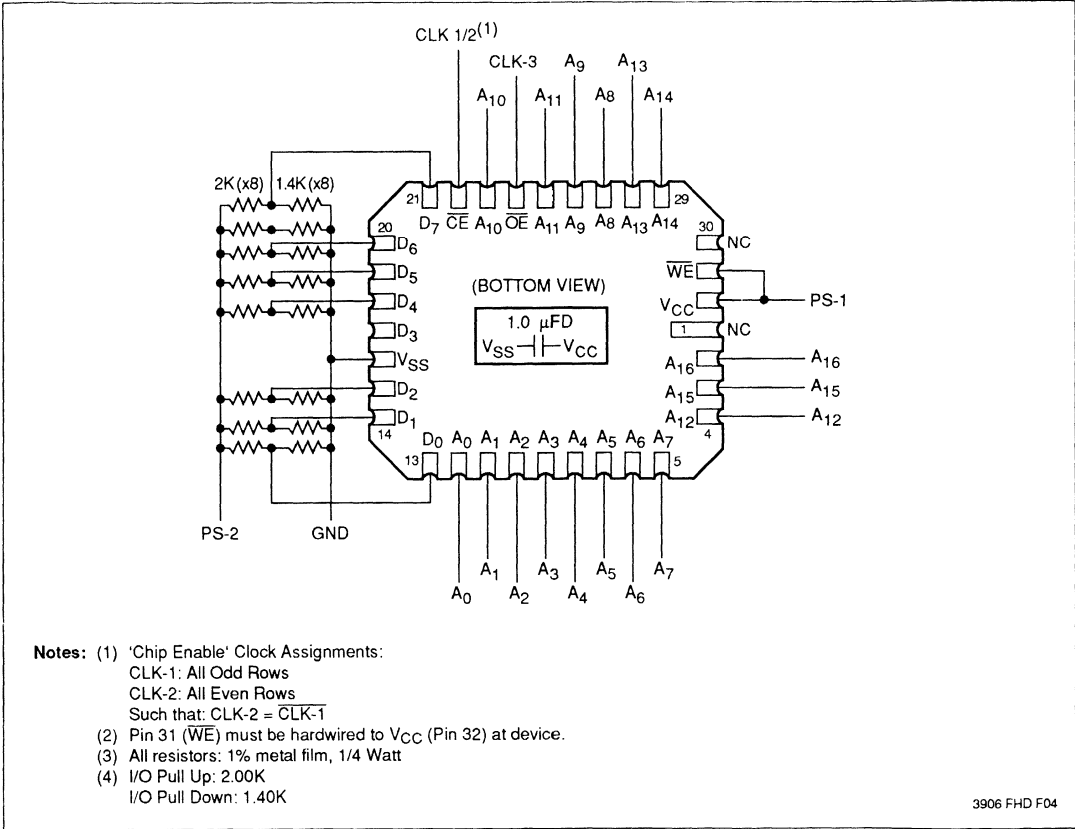


Figure 9. X24C44 and X24C45 Burn-In Timing



# Military Product Burn-in Circuits and Timing

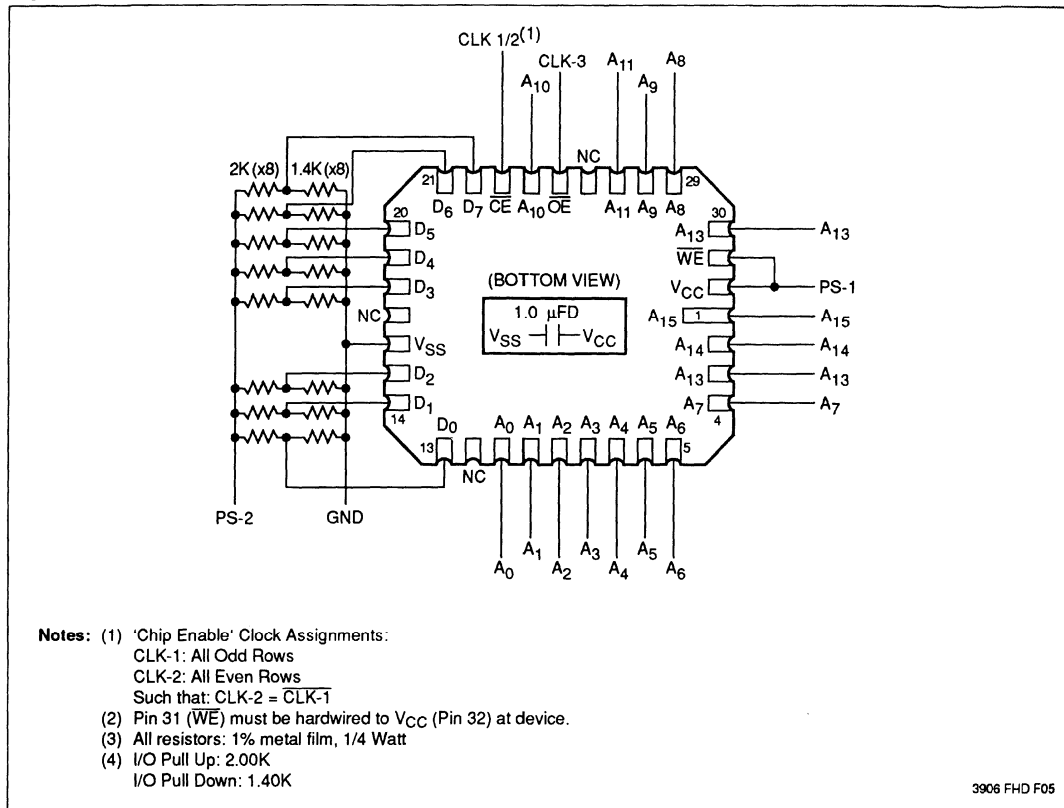
Figure 10. X28C512, X28C010 (LCC) Burn-In Circuit



3906 FHD F04

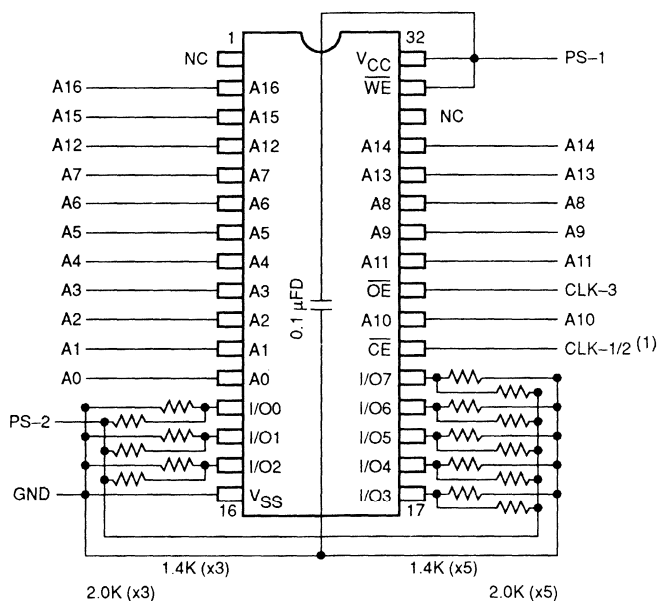
## Military Product Burn-in Circuits and Timing

Figure 11. X2816C, X28C64, X28HC64, X28C256, X28HC256, X28C513 (LCC) Burn-In Circuit



## Military Product Burn-in Circuits and Timing

**Figure 12. X28C512, X28C010 Burn-In Circuit**

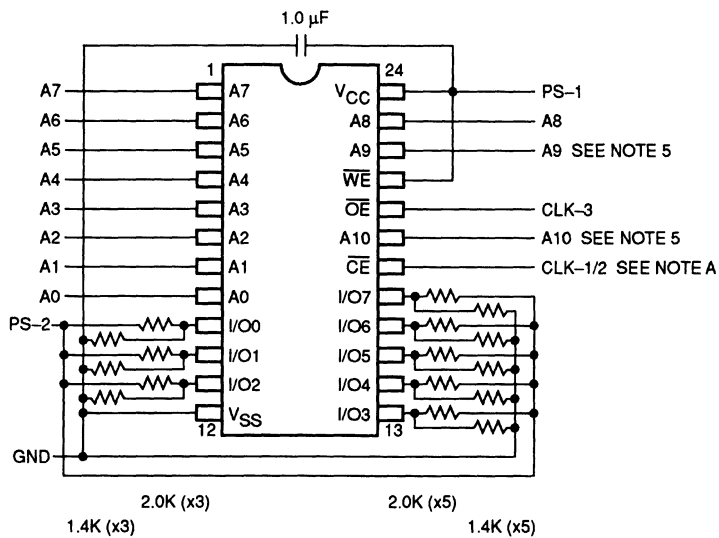


- Notes:** (1) 'Chip Enable' Clock Assignments:  
CLK-1: All Odd Rows  
CLK-2: All Even Rows  
Such that:  $\text{CLK-2} = \overline{\text{CLK-1}}$
- (2) Pin 31 (WE) must be hardwired to  $V_{CC}$  (Pin 32) at device.
- (3) All resistors: 1% metal film, 1/4 Watt
- (4) I/O Pull Up: 2.00K  
I/O Pull Down: 1.40K
- (5) Pin 2 (A16) is a no connect on the X28C512.

3906 FHD F03

## Military Product Burn-in Circuits and Timing

Figure 13. X2816C (DIP) Burn-In Circuit



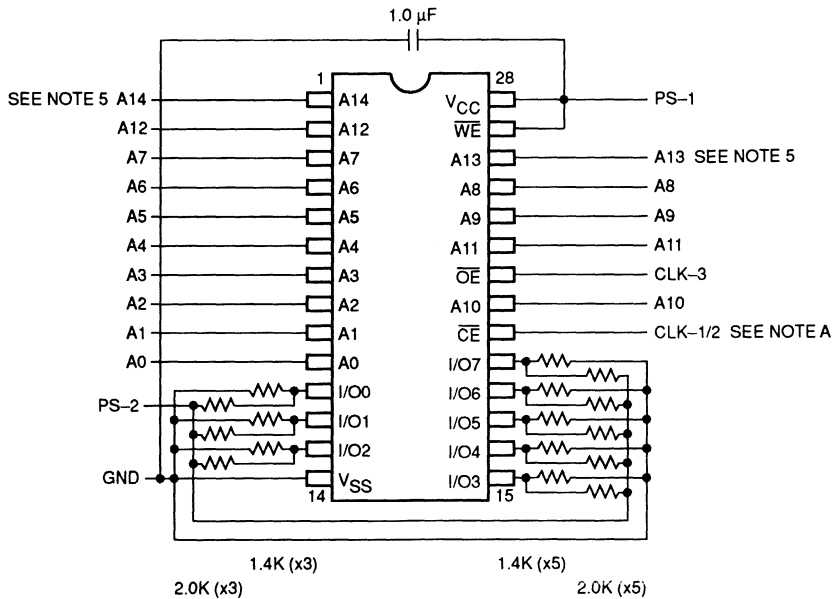
**Note A:** CLK-1: Rows 1, 3, 5 ... (odd rows— $\overline{CE_A}$ )  
 CLK-2: Rows 2, 4, 6 ... (even rows— $\overline{CE_B}$ )  
 Such that: CLK-2 = CLK-1

**Note B:** (1)  $\overline{WE}$  must always be hardwired to  $V_{CC}$  (Pin 24) at device as shown.  
 (2) All resistors: 1% metal film, 1/4 Watt  
 (3) I/O Pull Up: 2.0K $\Omega$   
 I/O Pull Down: 1.4K $\Omega$   
 (4) Socket-to-socket isolation as shown.

3906 FHD F20

# Military Product Burn-in Circuits and Timing

Figure 14. X28C64, X28HC64, X28C256, X28HC256 (DIP) Burn-In Circuit



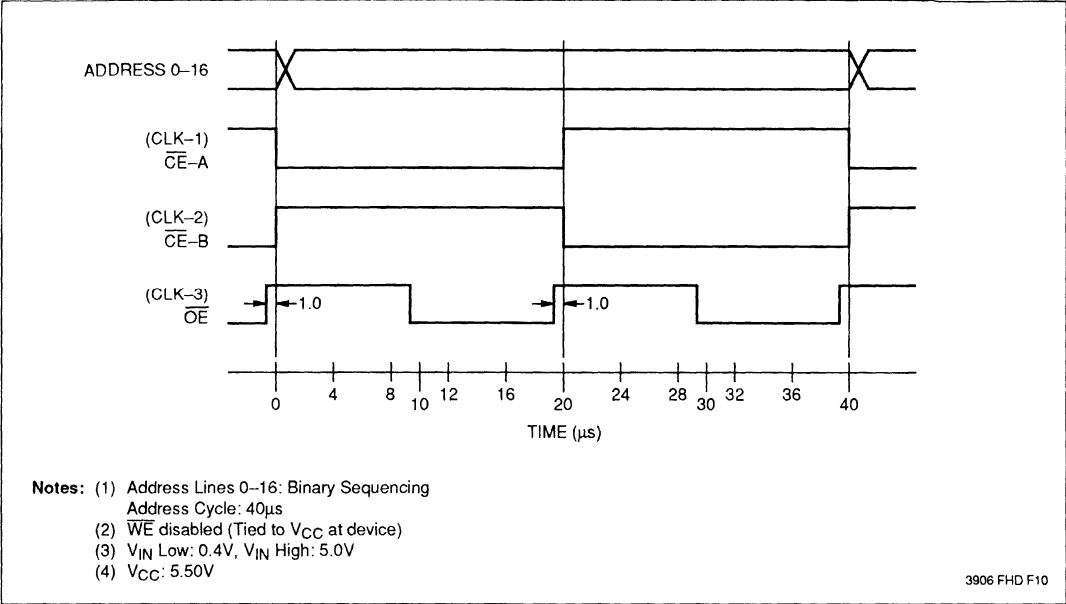
**Note A:** CLK-1: Rows 1, 3, 5 ... (odd rows— $\overline{CE}_A$ )  
 CLK-2: Rows 2, 4, 6 ... (even rows— $\overline{CE}_B$ )  
 Such that: CLK-2 = CLK-1

**Note B:** (1)  $\overline{WE}$  must always be hardwired to  $V_{CC}$  (Pin 28) at device as shown.  
 (2) All resistors: 1% metal film, 1/4 Watt  
 (3) I/O Pull Up: 2.0K $\Omega$   
 I/O Pull Down: 1.4K $\Omega$   
 (4) Socket-to-socket isolation as shown.  
 (5) Pin 1 (A14) and Pin 26 (A13) are no connects (NC) for the X28C64, X28HC64.

3906 FHD F21

# Military Product Burn-in Circuits and Timing

Figure 15. X2816C, X28C64, X28HC64, X28C256, X28HC256, X28C512, X28C513, X28C010 (LCC) Burn-In Timing



# Military Product Burn-in Circuits and Timing

Figure 16. X9CMME Burn-In Circuit

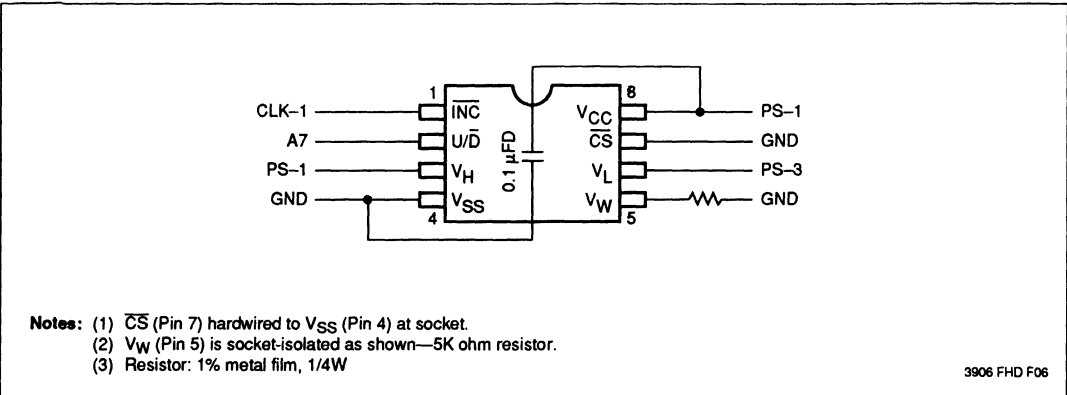
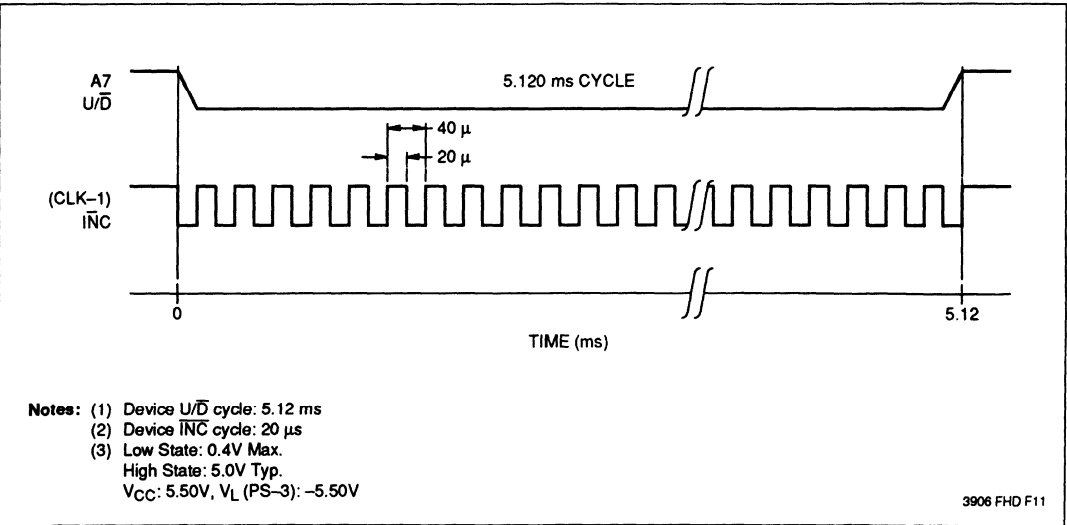


Figure 17. X9CMME Burn-In Timing





# Military Product Burn-in Circuits and Timing

Figure 18. X88C64, X68C64 Burn-In Circuit

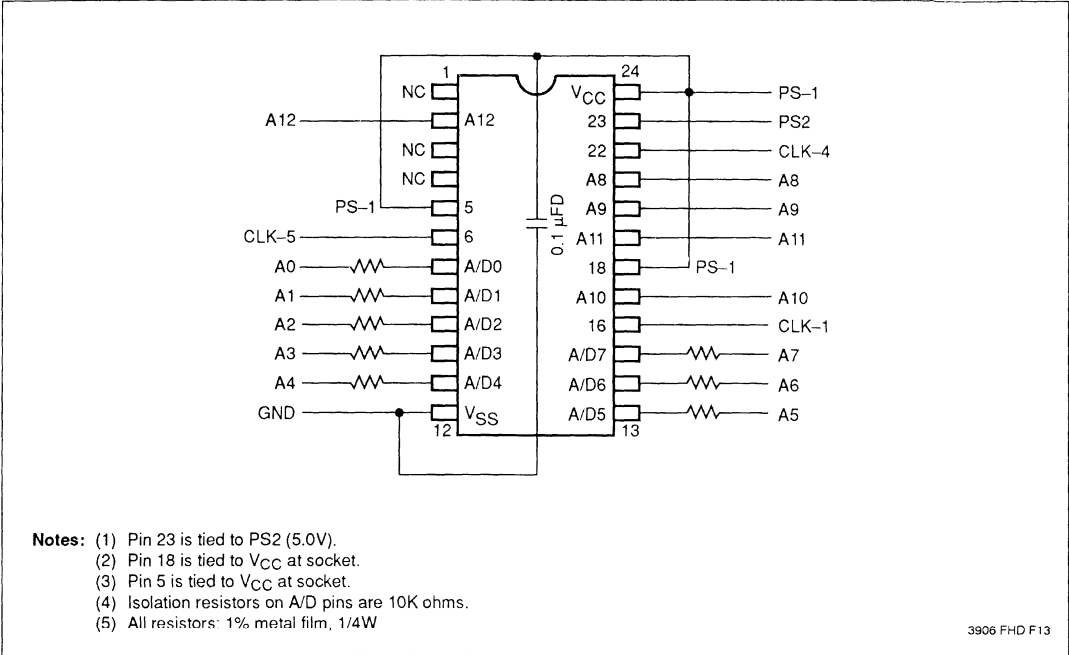
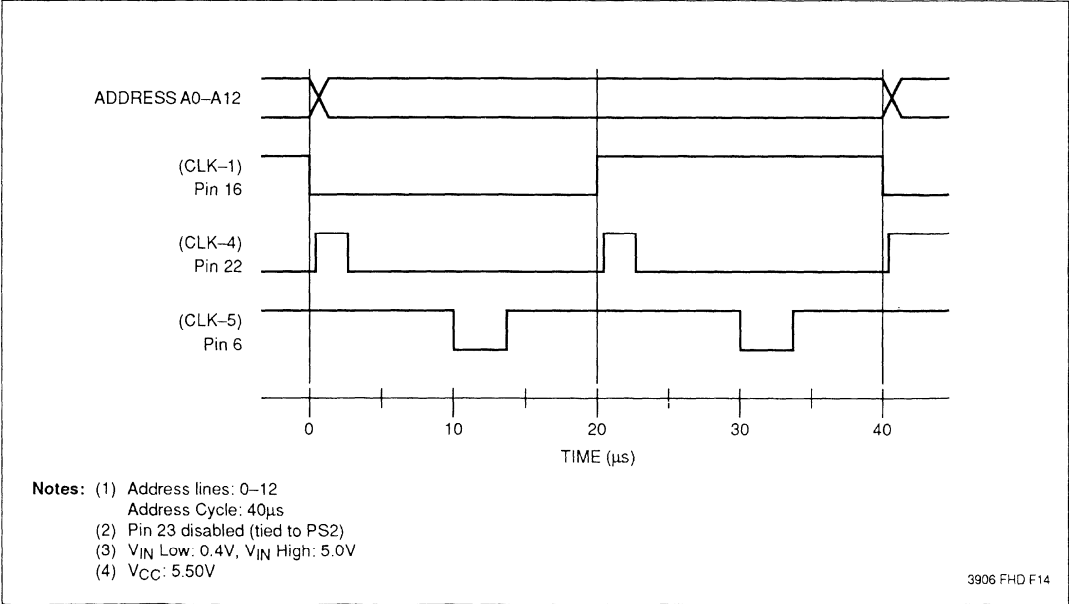


Figure 19. X88C64, X68C64 Burn-In Timing

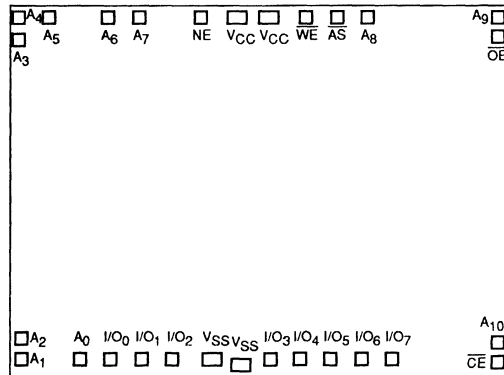




<b>NOVRAM* Data Sheets</b>	<b>1</b>
<b>Serial Products Data Sheets</b>	<b>2</b>
<b>E<sup>2</sup>PROM Data Sheets</b>	<b>3</b>
<b>E<sup>2</sup>POT™ Data Sheets</b>	<b>4</b>
<b>Microcontroller Peripheral Products</b>	<b>5</b>
<b>Memory Subsystems</b>	<b>6</b>
<b>Military Products</b>	<b>7</b>
<b>Die Products</b>	<b>8</b>
<b>Application Notes and Briefs</b>	<b>9</b>
<b>Reliability</b>	<b>10</b>
<b>General Information</b>	<b>11</b>

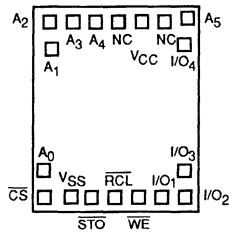


## Die Size and Pad Location



X20C16 Die Revision A  
.203 x .151

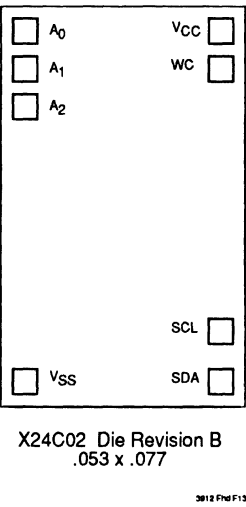
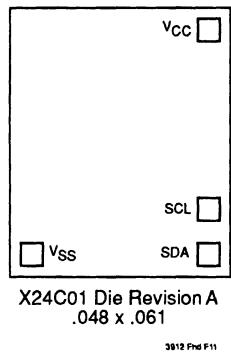
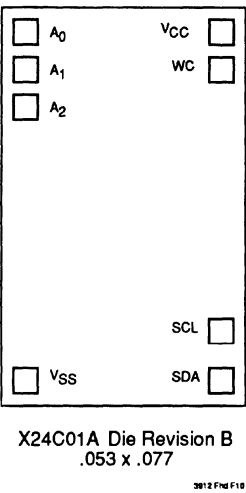
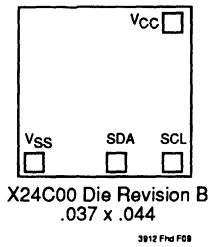
3912 Fnd F07



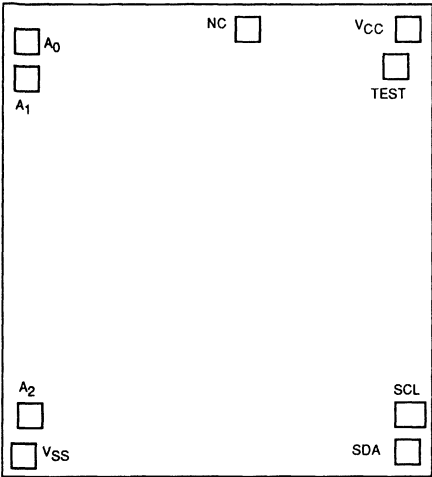
X22C10 Die Revision B  
.067 x .081

3912 Fnd F08

Die Size and Pad Location

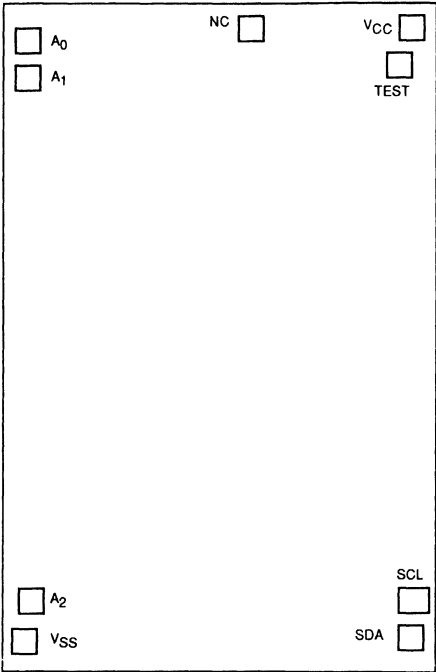


# Die Size and Pad Location



X24C04 Die Revision B  
.088 x .097

2012 Fnd F14

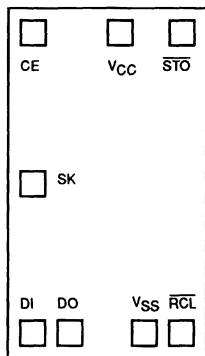


X24C16 Die Revision D  
.088 x .134

2012 Fnd F18

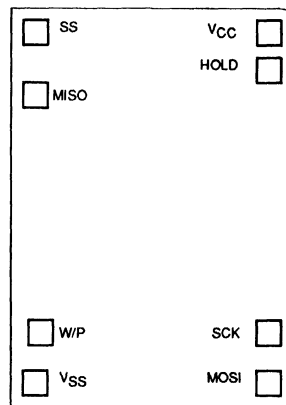
## Die Size and Pad Location

---



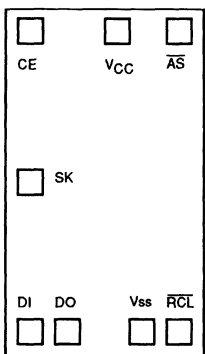
X24C44 Die Revision A  
.041 x .071

2012 Fnd F17



X25C02 Die Revision A  
.059 x .072

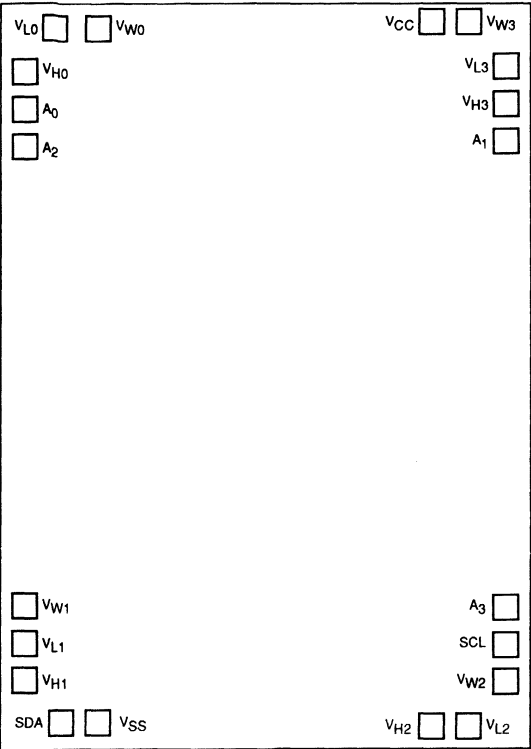
2012 Fnd F18



X24C45 Die Revision A  
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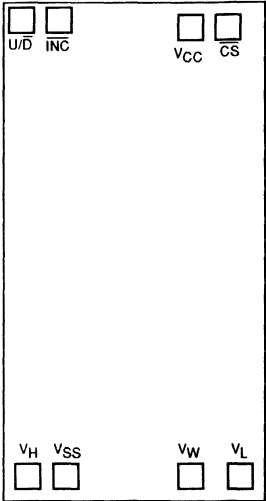
2012 Fnd F19

Die Size and Pad Location



X9241 Die Revision A  
.109 x .148

3812 Fnd F31

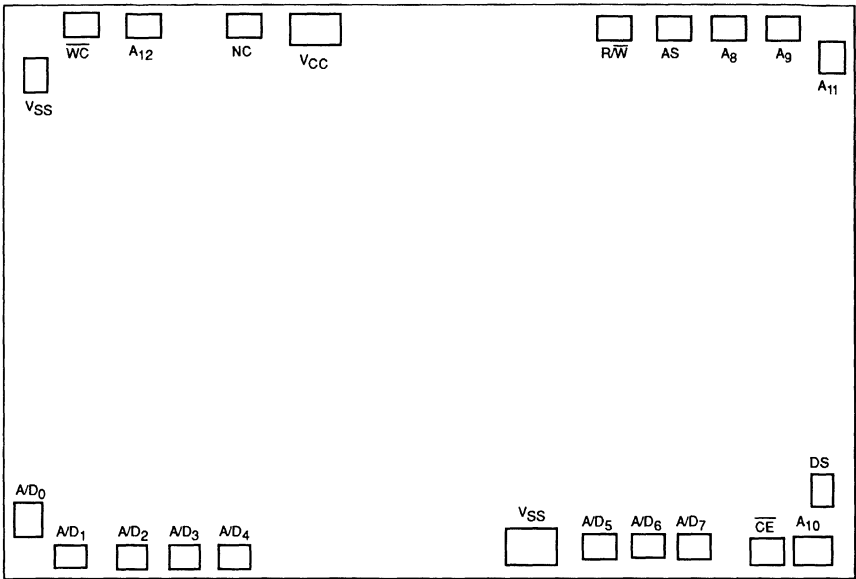


X9CMME Die Revision A  
.054 x .100

3812 Fnd F32

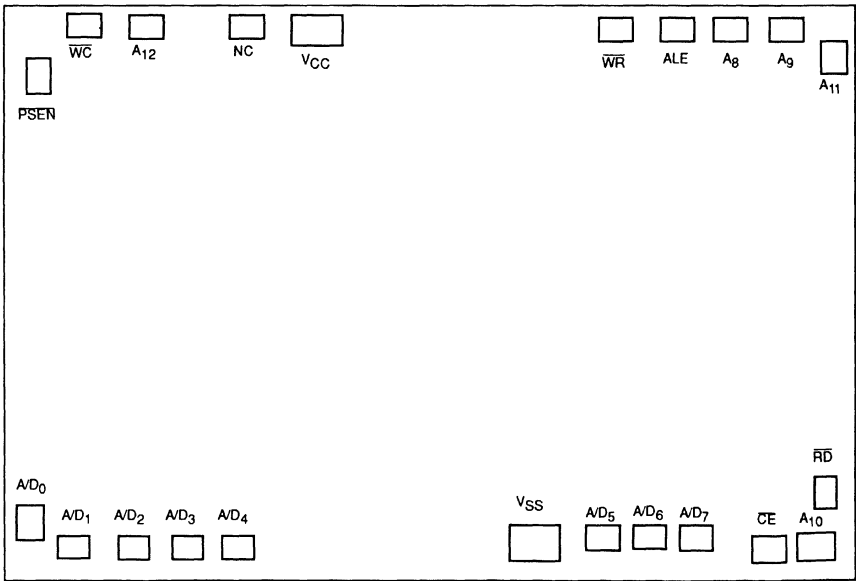


# Die Size and Pad Location



X86C64 Die Revision A  
.170 x .115

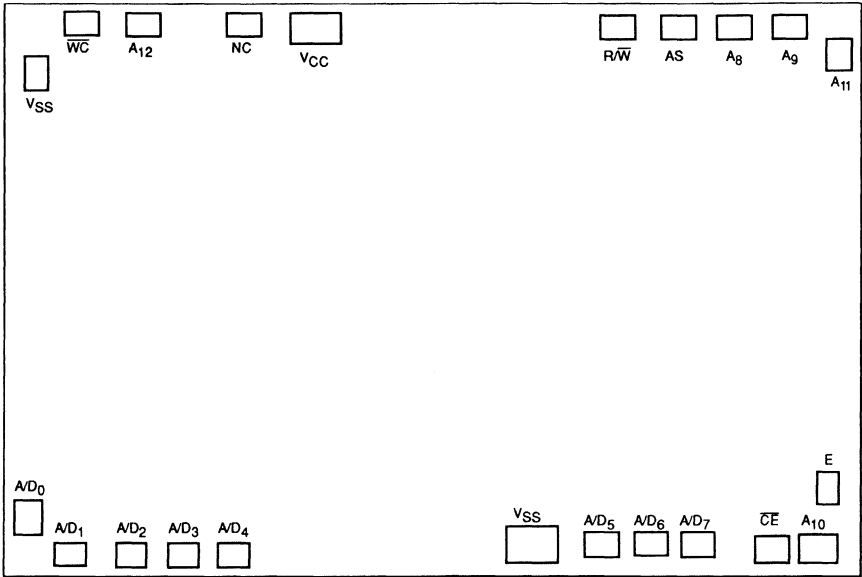
3812 Fnd F28



X88C64 Die Revision A  
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3812 Fnd F30

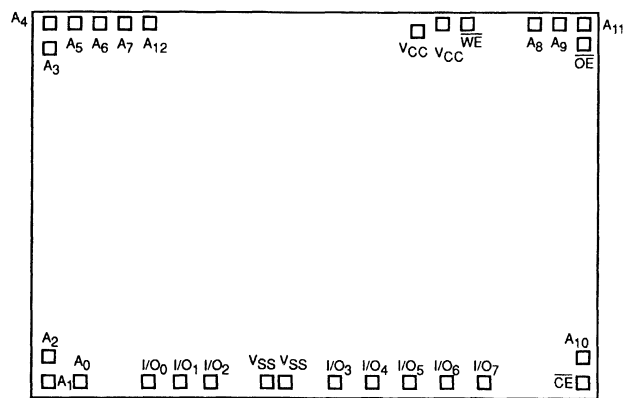
Die Size and Pad Location



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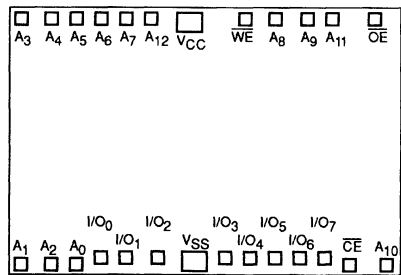
9812 F001 F 58

# Die Size and Pad Location



X28C64 Die Revision D  
.227 x .157

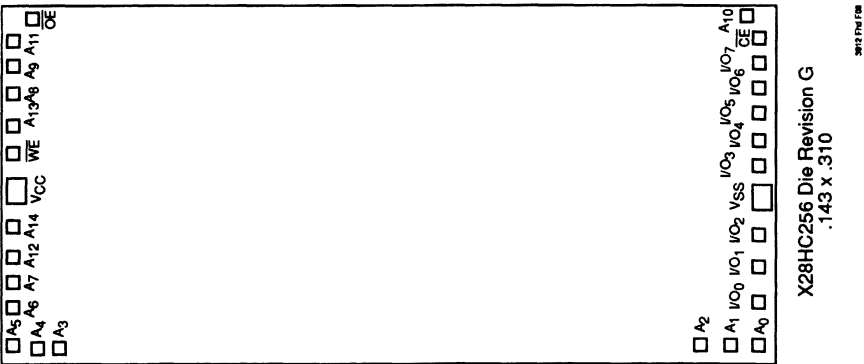
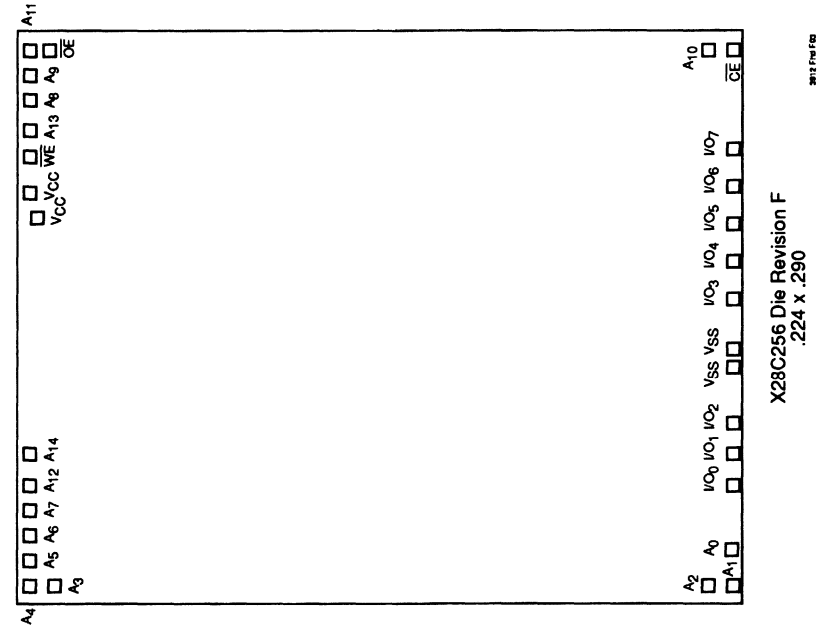
3912 Fnd F25



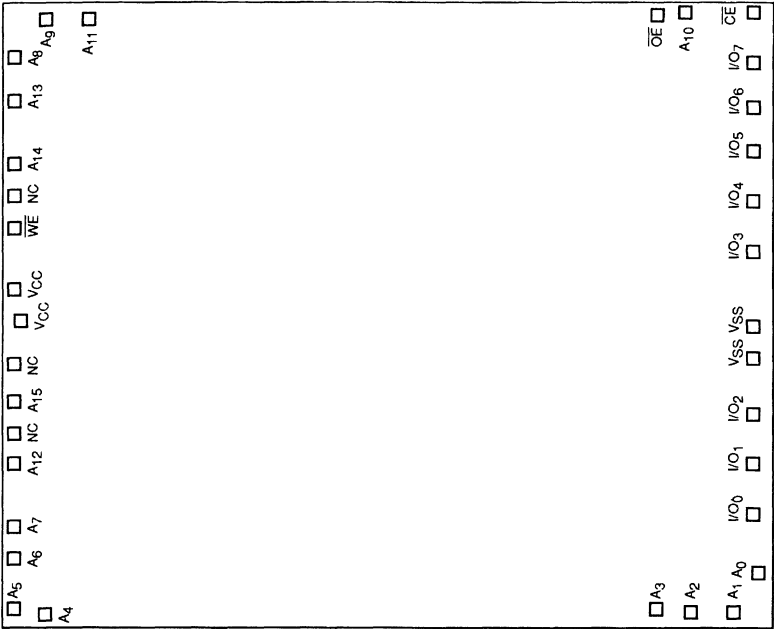
X28HC64 Die Revision C  
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3912 Fnd F27

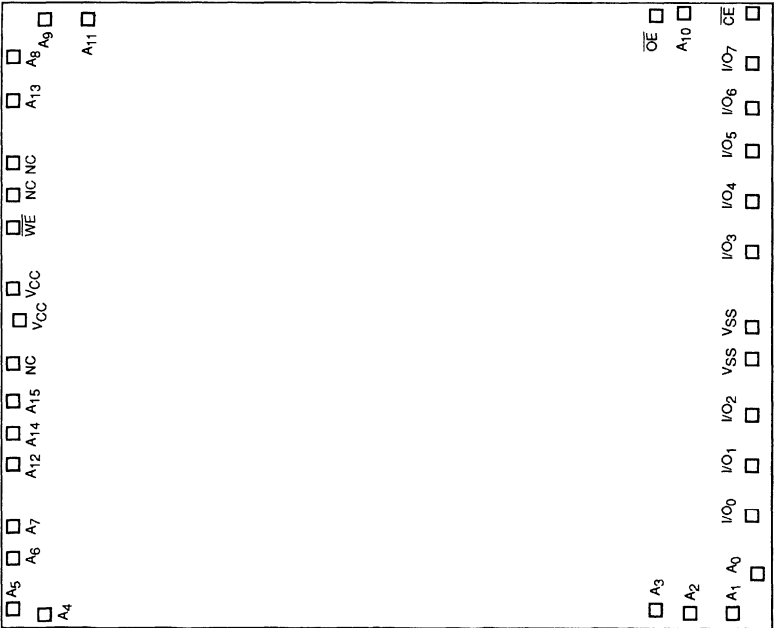
Die Size and Pad Location



Die Size and Pad Location

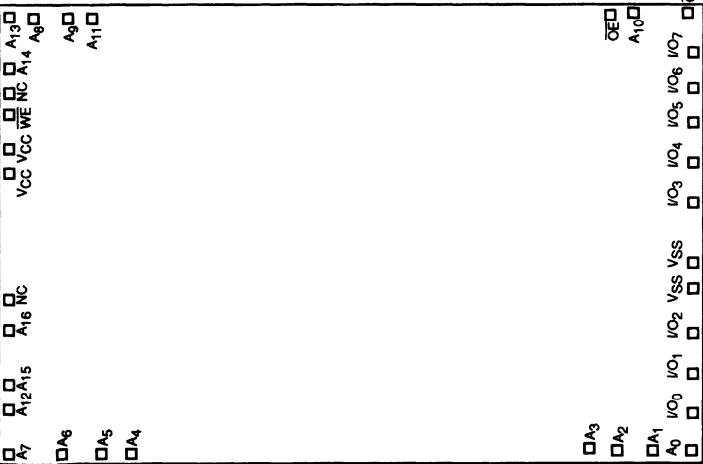
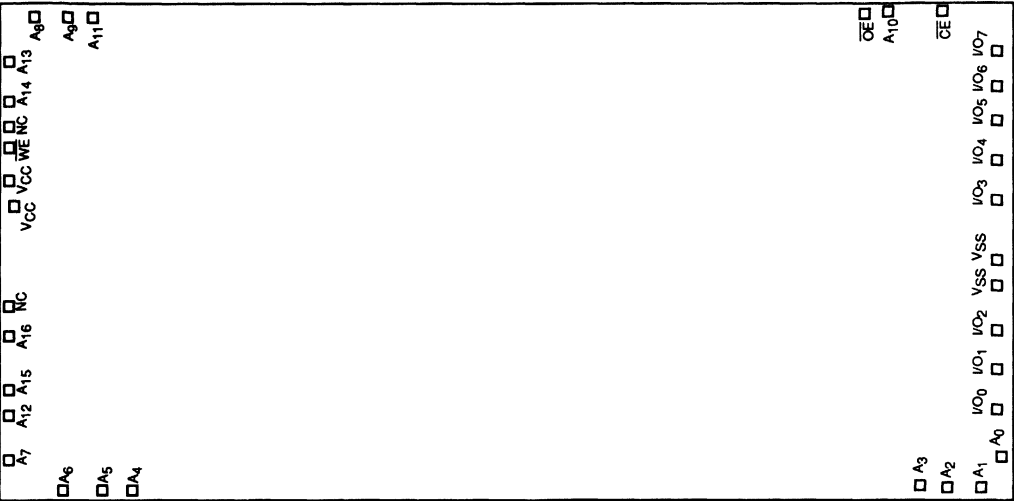


2012 FWD 004



2012 FWD 005

Die Size and Pad Location



X28C010 Die Revision B  
.232 x .358

X28C010 Die Revision A  
.253 x .510

## Die Size and Pad Location

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NOTES



<b>NOVRAM* Data Sheets</b>	<b>1</b>
<b>Serial Products Data Sheets</b>	<b>2</b>
<b>E<sup>2</sup>PROM Data Sheets</b>	<b>3</b>
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**NOTES**



## INTRODUCTION

The X2444 is a 256 bit serial NOVRAM internally configured as sixteen 16-bit words of RAM overlaid bit for bit with a nonvolatile E<sup>2</sup>PROM. The X2444 has the standard hardware RECALL and STORE inputs plus the ability to perform these same operations under software control, thereby freeing two microcontroller port pins for other tasks. The serial interface allows the X2444 to be packaged in a low cost space saving 8-pin mini DIP.

When teamed with the 8051 family of microcontrollers, the X2444's small physical size, software instruction set and serial interface make it an ideal parameter store and scratch pad memory while maintaining full use of the 8051 serial port as a UART.

## SCOPE

This application note describes interfacing the X2444 with the 8051 family of microcontrollers. Emphasis will be placed on the timing considerations of the interface, and explaining the modifications to the instruction words for normal device operation. This note assumes the reader has access to a Xicor Data Book and Intel *Microcontroller Handbook*.

## SERIAL PORT OPERATION

Port 3 on the 8051 provides a serial port that can be used in two basic configurations, full duplex and half duplex. This note examines the half duplex (mode 0) operation in interfacing to the X2444. Port 3 pin 1 (P3.1) is the clock output for both transmit and receive modes and Port 3 pin 0 (P3.0) is used for bidirectional data transfers.

The clock output frequency is  $\frac{1}{12}$  of the XTAL oscillator input frequency. To simplify timing calculations this note will assume an input frequency of 12 MHz resulting in a symmetrical 1 MHz output on P3.1.

The P3.1 and P3.0 pins when inactive (neither transmitting nor receiving) are always a logic 1 (HIGH). When a data transfer commences P3.1 will be LOW during machine cycle states S3, S4 and S5 and will be HIGH during states S6, S1 and S2. When transmitting, data is shifted out on P3.0 during S6P2 (state 6 phase 2) LSB first. When receiving, data is sampled during S5P2. Refer to Figure 1 for the basic 8051 serial port timing.

8051 / 2444  
PIN / PIN

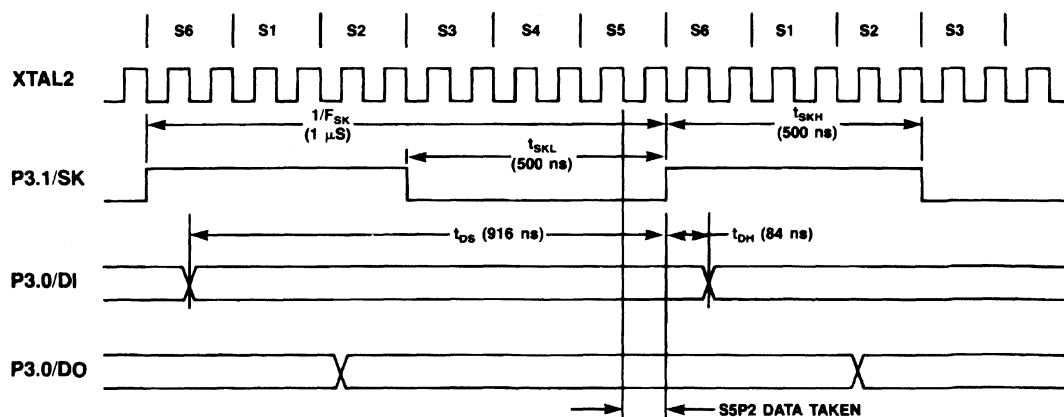


Figure 1. 12 MHz 8051 Serial Port Mode 0 and X2444 Timing

0003-2

# HARDWARE CONNECTIONS

The X2444 directly interfaces with the 8051 with no external circuitry required. DI and DO of the X2444 are both tied to P3.0, SK is tied to P3.1, CE is tied to any free port pin configured as an output and STORE and RECALL are tied to V<sub>CC</sub> (see Figure 2).

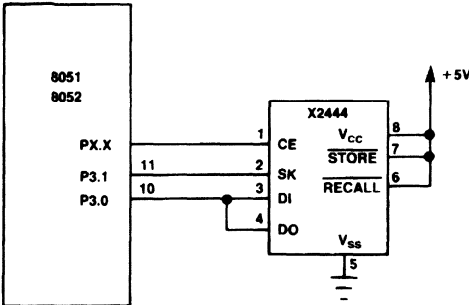


Figure 2. Basic Configuration

# X2444 OPERATIONS REVIEW

The X2444 is a serial device and in this application all chip functions are handled via the software instructions. The 8051 transmits data LSB first but the instruction format for the X2444 shows the instruction to be transmitted MSB first. This requires a simple transposition of the instruction, MSB for LSB. The memory is effectively a FIFO, so the data to be stored need not be transposed.

Internally the X2444 increments a bit (clock) counter. This is used to indicate the end of an instruction and if a read or write instruction is received, to increment a bit position pointer. This pointer enables individual RAM cells for writing and reading. The counter for the pointer increments from zero to fifteen. If CE remains HIGH and SK continues to clock, the counter will rollover from fifteen to zero. The word address does not increment; therefore, during a write operation if SK continues to clock and CE is HIGH, a 25<sup>th</sup> rising clock edge (8 edges for instruction + 16 edges for the data word + 1) would cause bit position zero to be overwritten.

# SYSTEM CHARACTERISTICS

Under normal operating conditions the X2444 expects CE to transition LOW to HIGH when SK is LOW in order that the first bit of data can be clocked into the X2444 on the first rising edge of SK. The data is sampled to see if it is "0" (a don't care state) or a "1" which is recognized as an instruction start. The 8051, however, places both P3.1 and P3.0 in the HIGH state when not actively transmitting. **THIS IS OK.** The X2444 internally gates CE and SK; therefore, toggling the port pin controlling CE to a HIGH effectively generates the first rising edge of SK, and also clocks in the HIGH present at P3.0 (DI).

What this does is clock a "1" into the X2444 indicating the start of an instruction prior to any shifting operation by the 8051 serial port. This will require dropping the leading "1" from the instruction. See Table 1 for the WAS/IS conditions for the equivalent instructions to be used by the 8051.

INSTRUCTION	WAS								IS							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
WRDS	1	X	X	X	X	0	0	0	X	0	0	0	X	X	X	X
STO	1	X	X	X	X	0	0	1	X	1	0	0	X	X	X	X
SLEEP	1	X	X	X	X	0	1	0	X	0	1	0	X	X	X	X
WRITE	1	A	A	A	A	0	1	1	X	1	1	0	A	A	A	A
WREN	1	X	X	X	X	1	0	0	X	0	0	1	X	X	X	X
RCL	1	X	X	X	X	1	0	1	X	1	0	1	X	X	X	X
READ*	1	A	A	A	A	1	1	X	1	X	1	1	A	A	A	A

\*Note: bit 7 of the READ command should be a "1" to avoid bus contention.

Table 1. Reconfigured Instruction Format

The 8051 will still generate eight rising clock edges on P3.1 for each byte loaded into the shift register (SBUF), effectively providing the X2444 with nine clocks for the first byte. For the single byte instructions the ninth clock and data are ignored by the X2444. Refer to Figure 3 for the single byte instruction timing.

8051/52 / 2444  
PIN / PIN

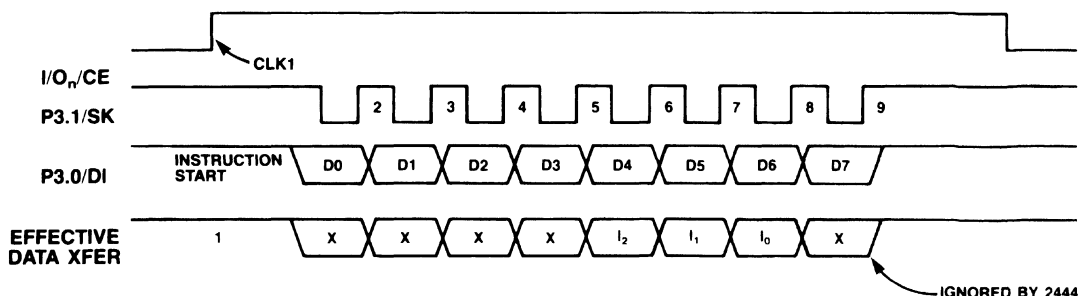


Figure 3. Single Byte Instructions

## WRITING

Writing to the RAM array is straightforward. The write instruction is issued by the 8051 in the same manner as the single byte instructions. The MSB (eighth bit) of the instruction byte is clocked in on the equivalent ninth clock rising edge. This bit is recognized as the first data bit transfer and is initially written into the addressed word's bit position zero. The 8051 will continue to transmit two more bytes of actual data. The LSB (bit "0") of the first byte will be physically located in bit position "1" and all subsequent bits will also be offset by one. The MSB (sixteenth data bit) of the word will be written into bit position zero, overwriting the last bit of the instruction byte. Refer to Figure 4 for the sequence of operations.

## READING

Reading data back from the RAM array is quite similar. The X2444 begins to shift data out during the instruction cycle (more on this later). After the instruction is shifted out, the 8051 must turn around P3.0 and configure it as an input. CE and SK are static during this period and the DO output will remain unchanged until after the rising edge of the first 8051 receive data clock. Therefore, the first data shifted into the 8051 will be from bit position "1", equivalent to the LSB originally written. Refer to Figure 5 for the sequence of operations.

8051 / 2444  
PIN / PIN

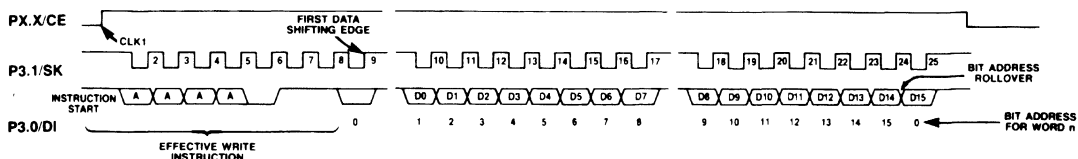


Figure 4. Write Cycle Sequence

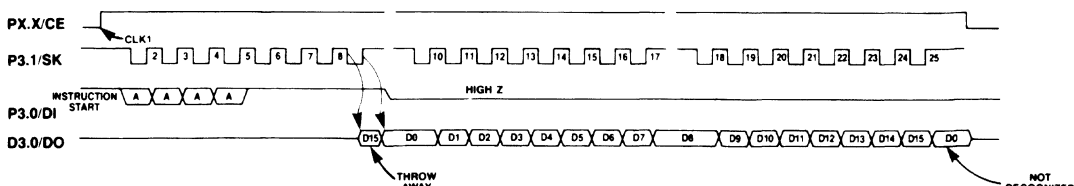


Figure 5. Read Cycle Sequence

## BUS CONTENTION

There will not be any bus contention for single byte instructions or the write command. However, for the Read command there could be contention. While the 8051 is still shifting out the instruction byte the X2444 begins to output data on the same line. Refer to Figure 5, just after the falling edge of clock eight.

The 8051 shifts out data at S6P2. If the data changes state from "0" to "1" a high current enhancement FET is turned on for two 8051 system clock cycles. This is used to provide a fast rise time. At the end of this two cycle period, the enhancement FET is turned off and the output is held HIGH by a depletion mode FET that essentially looks like a resistor pullup (Refer to Intel's *Microcontroller Handbook* [1984] pages 6-6 and 6-7). Note that the high drive circuit is enabled only for data state changes from "0" to "1"; therefore, if the output is already a "1" and another "1" is shifted out on P3.0, the high drive will *not* be turned on. This depletion FET can source a maximum of 250 $\mu$ A if the port pin is grounded.

The instruction table indicates that bit seven for the READ instruction should be a "1". The reason for this is to guarantee that the high drive period is off before the X2444 begins to output data. If bit seven were a "0", the 8051 would turn on the high drive circuit to return P3.0 to the inactive state, possibly generating a high current contention problem with the DO output of the X2444. Figure 6 illustrates the timing involved during clock eight. The high drive period of the 8051 is turned off well before the X2444 begins to output data.

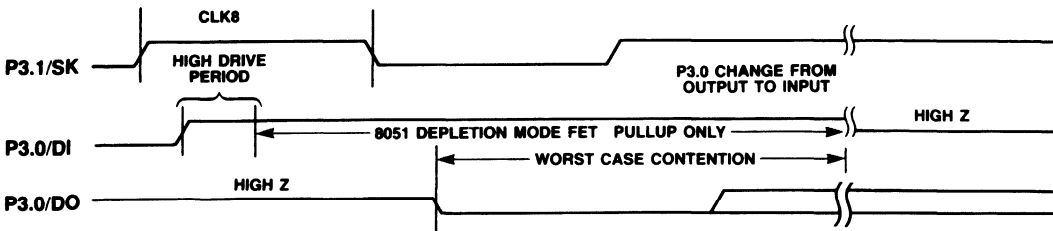


Figure 6. Worst Case Bus Contention

## VERSATILITY

The DO output of the X2444 is always in the high impedance state unless it is outputting data in response to a READ command. Therefore, the serial port of the 8051 need not be dedicated solely to a serial memory interface.

Figure 7 illustrates the versatility this affords. This figure depicts the basic system components required in a remote location controller. Notice that the 8051 serial port has access to both the X2444 and through the use of the CE control line maintains full use of the serial port as a UART. Therefore, it can receive downloaded parameters from a host, re-enable the serial port for X2444 communication, then store the data either temporarily in the X2444 RAM array or permanently in the X2444 E<sup>2</sup>PROM array.

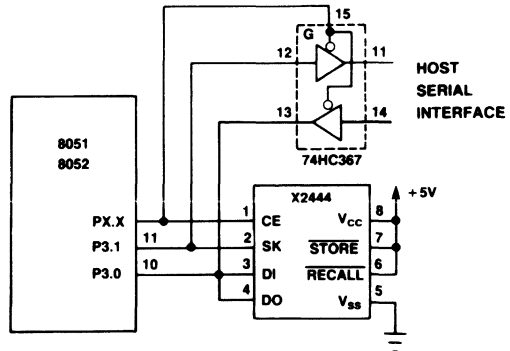


Figure 7. Shared Serial Port



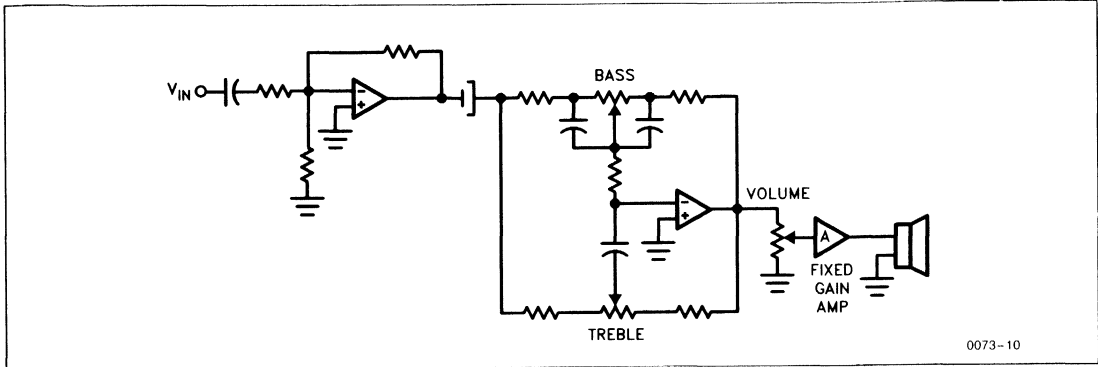
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## CONCLUSION

This application note has shown that with no extra hardware the X2444 interfaces directly with the 8051 family of microcontrollers, providing a non-volatile memory store and scratch pad memory and

maintaining full 8051 UART capabilities. It is the ideal solution for applications where extra memory is required but few port pins are available for implementation.

0003-6



# **E2POT™ DIGITALLY CONTROLLED POTENTIOMETER BRINGS MICROPROCESSOR CONTROL TO AUDIO SYSTEMS— ADDS FEATURES**

**By Jeff Randall**

## INTRODUCTION

Control of most audio circuits is still accomplished the same way it has been for the last fifty years or so. From the volume control knob to the sliders on an equalizer, the control is human, the feedback is through the ears, and the control element is the mechanical potentiometer. Microprocessors have entered nearly every other segment of electronics, and as they enter the audio segment, they slam head-long into the mechanical potentiometer.

While this article focuses on microprocessor control of conventional audio circuits through the use of digitally controlled potentiometers, it should become clear how these devices can be applied to many other applications as well.

## CONVENTIONAL AUDIO CONTROL

A look at conventional methods for audio control should help to illustrate the situation:

Designs incorporating mechanical potentiometers are still found in the majority of audio applications. For example, the volume control on most car stereos is a rotary potentiometer. Volume control circuits generally resemble Figure 1. In this design, the potentiometer is used to control the signal reaching a fixed gain amplifier section. A potentiometer in this application would likely have a logarithmic taper, since volume is a logarithmic function.

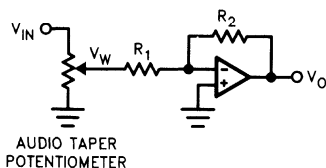


Figure 1: Conventional Potentiometer Volume Control

0073-1

Tone controls can vary from single pot and capacitor circuits to complex active filters. The Baxandall filter network has been the workhorse of the audio industry for years. This design, illustrated in

Figure 2, utilizes two linear taper potentiometers to control the gain of an active filter. In this configuration, the potentiometer replaces a portion of both the input and feedback resistors. By moving the position of the wiper, both resistors change in opposite directions.

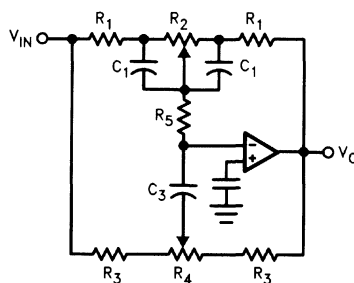


Figure 2: Baxandall Tone Control Circuit

0073-2

Graphic equalizers are one of the fastest growing modes of audio control. A graphic equalizer contains a group of band pass filters, usually seven. Each filter has a potentiometer controlling the gain to that band pass. Potentiometers generally appear as sliders on the face of the equalizer.

A typical graphic equalizer schematic is shown in Figure 3. EQs are used to compensate for the imperfections of a listening environment by boosting or cutting gain at specific frequencies. By using a spectrum analyzer and a "pink" noise generator, the response of an audio system can be customized for a particular room or concert hall. This is accomplished by inputting a desired response to the system—generally flat across the audio band, with some attenuation at higher frequencies, often referred to as "pink" noise. The equalizer is then adjusted until the system output, displayed on the spectrum analyzer, closely matches the pink noise input.

This process of matching a system to a room is often referred to as environmental calibration. It is a process requiring the listener to read the display of the spectrum analyzer and manually adjust the potentiometer/sliders of the equalizer.

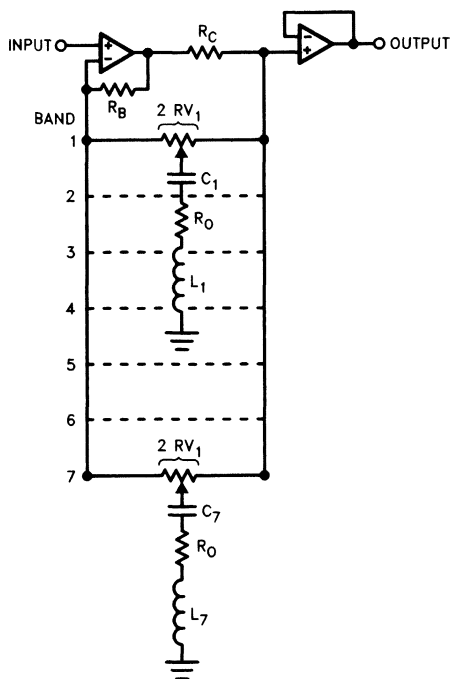


Figure 3: Graphic Equalizer Configuration

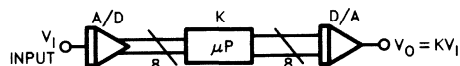
0073-3

The heart of the control of each of the circuits described earlier is the mechanical potentiometer. Automated control of these devices is a challenge. Clearly, microprocessor control of these functions is desirable. The control elements utilized for automated control are discussed below.

## AUTOMATED CONTROL ELEMENTS

While these devices are primarily used for industrial control applications, motorized potentiometers offer a relatively straightforward approach to simple audio control circuits. In these devices, a DC reference voltage, or a digital signal representing position is input to a small motor assembly that is linked to a rotary potentiometer. Drawbacks to this type of system are numerous, including noise caused by the motor assembly as well as the increased space and power requirements of placing a motor on an audio PC board.

D/A converters can also be used to control and manipulate analog circuit functions, but introduce more complexity. These devices are the choice of high fidelity digital audio controls due to their high precision. But for the analog circuit designer, they can be a little intimidating. For example, one way to control volume with D/A converters is illustrated in Figure 4. In this circuit, the signal is sampled with a A/D converter, manipulated by a microprocessor, and returned to the analog world with a D/A converter. This design entails sampling, real-time processing, as well as A/D and D/A conversions. Not only may the analog designer be faced with portions of his circuit that may be unfamiliar, the results may be overkill.



0073-4

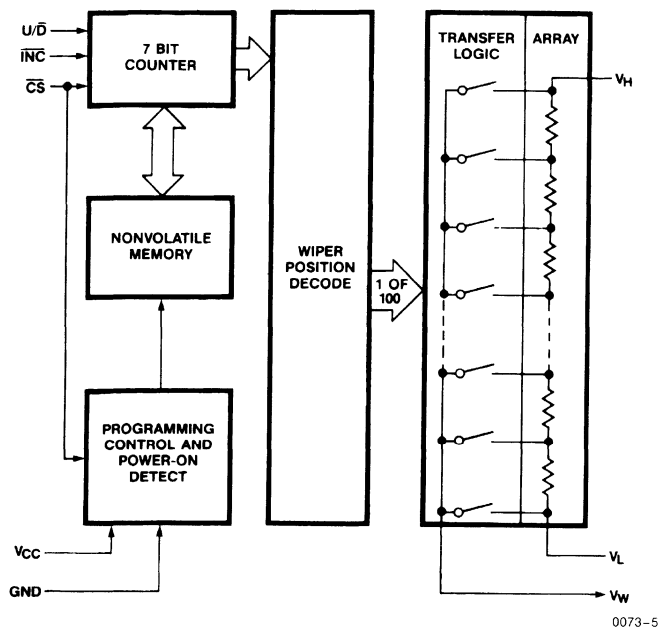
Figure 4: Volume Control Using D/A Conversion

An array of resistors with a wiper tap that can be selected with digital control offers many advantages of the microprocessor world without the complexity of D/A conversion. These are referred to as digitally controlled potentiometers. Logic circuits, counters, and memory circuits are often teamed up with resistor arrays to accomplish an approximation of potentiometer control. Recently, a few manufacturers have introduced devices which incorporate many of these functions in one device. Examples are Xicor's X9MME, Toshiba's TO9169AP, and National's LMC835.

The Toshiba and National parts are designed around specific audio applications and are distinctively different from the Xicor device. They incorporate features that lend well to audio designs, but are not intended for general purpose potentiometer replacement. Moreover, they offer only a limited number of wiper positions.

Xicor's X9MME combines a single 99 position potentiometer with three line digital controls. Figure 5 contains a functional diagram, pin description and mode selection for the device. In addition to the internal counter circuitry for wiper position control, this part also incorporates nonvolatile memory to retain wiper position. It has been designed as a digitally controlled replacement for the mechanical potentiometer. With its conventional three terminal potentiometer design, it integrates easily into existing analog designs.

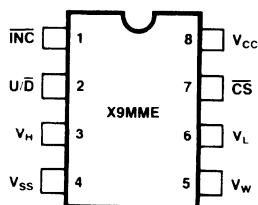
## Functional Diagram



## Mode Selection

CS	INC	U/D	Mode
L		H	Wiper Up
L		L	Wiper Down
	H	X	Store Wiper Position

## Pin Configuration



## Pin Names

V <sub>H</sub>	High Terminal of Pot
V <sub>W</sub>	Wiper Terminal of Pot
V <sub>L</sub>	Low Terminal of Pot
V <sub>SS</sub>	Ground
V <sub>CC</sub>	System Power
U/D	Up/Down Control
INC	Wiper Movement Control
CS	Chip Select for Wiper Movement/Storage

Figure 5: The X9MME Digitally Controlled Potentiometer

To illustrate digital control of potentiometer circuits, the X9MME from Xicor was used to replace mechanical potentiometers in a well known audio circuit. The following should demonstrate the ease of designing with the X9MME as well as the advantages of microprocessor control in audio circuits.

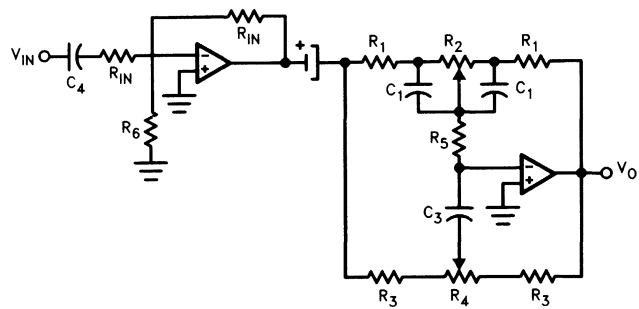
## THE X9MME IN AN AUDIO CIRCUIT

The Baxandall tone control circuit is the basis for the designs shown here. The following sections will discuss the principles behind the Baxandall circuit

and then walk through the design utilizing the X9MME. Special design considerations for the X9MME will be discussed, and the performance and operation will be evaluated.

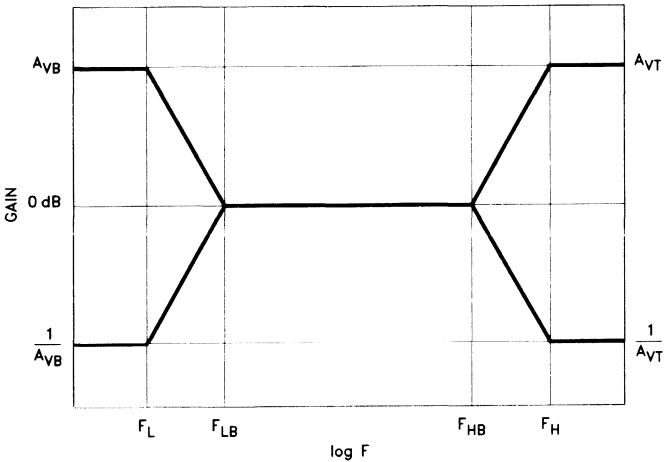
The Baxandall circuit, its response, and equations for gains and filter frequencies are shown in Figure 6. This circuit contains two active filters whose gain is controlled by two potentiometers. Figure 7 illustrates the bass portion of the circuit. The maximum gain of this circuit is at low frequencies, where the capacitors in the circuit can be considered to be open circuits. The capacitors have been omitted for clarity. (The treble portion of the circuit, not illustrated here, follows along similar lines.)

# Schematic



0073-7

# System Frequency Response

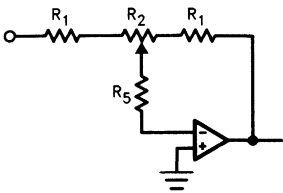


$$F_L = \frac{1}{2\pi R_2 C_1}$$
$$F_{LB} = \frac{1}{2\pi R_1 C_1}$$
$$A_{VB} = 1 + \frac{R_2}{R_1}$$

$$F_H = \frac{1}{2\pi R_3 C_3}$$
$$F_{HB} = \frac{1}{2\pi (R_1 + R_3 + 2R_5) C_3}$$
$$A_{VT} = 1 + \frac{2R_5 + R_1}{R_3}$$

Figure 6: Active Audio Preamplifier

With the addition of another potentiometer on the output of the Baxandall network, the system represents a single channel of an audio preamplifier. The circuit contains three potentiometers which control volume, treble and bass. These pots would appear as knobs on the face of a home or car stereo, to be adjusted by hand to control and shape the sound reaching the amplifier and speakers.



0073-9

$$A_{VB} = 1 + \frac{R_1 + R_2}{R_1}$$
$$\text{Maximum Bass Boost}$$

Figure 7: Bass Portion of Active Preamp Circuit

Neglecting the digital control lines and 5V power for the X9MME, the circuit is shown in Figure 8. The X9MME will replace bass, treble and volume potentiometers. Note that this does not alter analog design considerations.

It should be noted that  $R_2$  and  $R_4$  are both linear taper pots. Since the X9MME is also a linear taper pot, it is a direct replacement.  $R_V$ , the volume potentiometer, is specified as an audio taper pot, since it is used for volume control. By placing a small resistor from wiper to low on any linear pot, as shown in Figure 9, an audio taper can be approximated. In this case a resistor of one-tenth the total pot resistance is a close approximation of an audio pot (EDN Nov. 13, 1986).

This circuit is designed to have a gain of one across the entire audio range, with the potential for a boost or cut of 20 dB at the frequencies selected by the designer.

## THE DESIGN

The design chosen is intended for car stereo applications. It should therefore operate from a single ended, 12V supply and adapt well to speakers that

are commonly used in automobiles. Considering the limited bass response of most car speakers, the bass boost or cut should not be so low that the speakers cannot reproduce the sound.

The desired circuit would operate from a 12V power supply, have a  $\pm 20$  dB boost or cut at 100 Hz (bass) and 10 KHz (treble). The available resistor values for the X9MME are 10K, 50K, and 100K. The following steps outline the design:

1.  $R_2 = 50 \text{ K}\Omega$  (arbitrary, X9503)

The design must start somewhere. This value was actually determined after running through the design a couple of times and comparing the values determined for the potentiometers with those available.

2.  $A_{VB} = 1 + R_1/R_2$ ; for 20 dB (10),

$$R_1 = R_2/9 = 5.6 \text{ K}\Omega$$

The bass portion of the circuit must have a maximum boost of 20 dB. This is determined with the bass pot all the way to the input side. A quick look at Figure 8 will illustrate this.

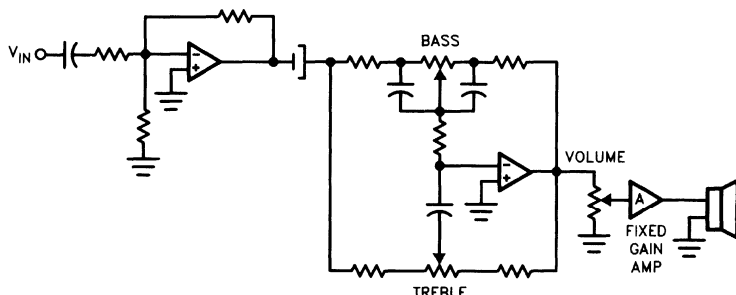
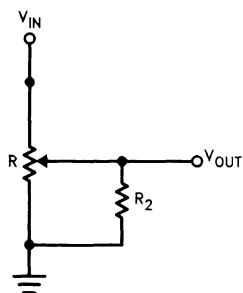


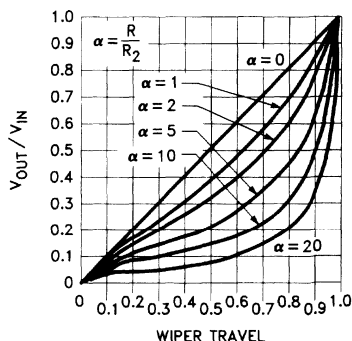
Figure 8: Active Preamp with Bass, Treble and Volume Controls

0073-10



0073-11

For Audio Taper, Use  $R_2 = \frac{R}{10}$ .



0073-12

Figure 9: Utilizing External Resistors to Vary Potentiometers Trim (EDN Nov. 13)

$$3. F_L = 100 \text{ Hz}, F_{LB} = 1 \text{ KHz}$$

$$C_1 = \frac{1}{2\pi F_{LB} R_1} = \frac{1}{2\pi(1000)(5.6K)} \\ = 2.84 \times 10^{-8} \text{ F}$$

Here, the formulas for the cutoff frequencies of the active filters are broken down to determine the element values to use.

$$4. R_5 = 2.2 \text{ K}\Omega \text{ (arbitrary)}$$

$$5. A_{VT} = 1 + \frac{R_1 + 2R_5}{R_3} = 10,$$

$$R_3 = \frac{R_1 + 2R_5}{9} = 1.1K$$

Use 1 K $\Omega$

Here, the maximum treble gain is calculated in similar fashion to the maximum bass gain.

$$6. C_3 = \frac{1}{2\pi F_H R_3} = \frac{1}{2\pi(10K)(1K)} = 1.6 \times 10^{-8}$$

$$7. R_4 \geq 10(R_3 + R_1 + 2R_5) = 110 \text{ K}\Omega$$

Use 100 K $\Omega$

$$8. R_V = 10 \text{ K}\Omega \text{ (arbitrary)}$$

The circuit with the X9MME inserted is shown in Figure 10. These are the values that were used in lab experiments and for demonstration purposes.

It should be noted that some considerations in the design had to be altered when the X9MME was inserted into the circuit. The X9MME is a source of high frequency noise. There are internal voltage generators on the device which are used to operate switches internally as well as to store information into the device's nonvolatile memory. The principle noise frequencies begin at approximately 150 KHz, and while this is beyond the audio range, it can still be a source of problems in the circuit. For this reason, capacitors were added around the X9MME to filter noise. These are included in Figure 10.

## DIGITAL CONTROL

The digital control lines of the X9MME are  $\overline{INC}$ ,  $\overline{CS}$ , and  $U/\overline{D}$ .  $\overline{CS}$  (chip select) allows the wiper to be moved.  $U/\overline{D}$  (Up/Down) determines the direction in which the wiper will move, and  $\overline{INC}$  (increment) initiates movement on its falling edge.  $\overline{CS}$  is also used to store the wiper position in nonvolatile memory. When  $\overline{CS}$  is returned high, a store operation is commenced.

When initially designing with the part, it was helpful to assemble a simple switch system for controlling the parts. A 555 timer was used to generate a fairly slow clock pulse and connected through a momentary switch to the increment pin of each X9MME. With pull up resistors on each digital line, a grounding switch was connected to  $U/\overline{D}$  and another to  $\overline{CS}$ . To move the wiper up,  $\overline{CS}$  was set to

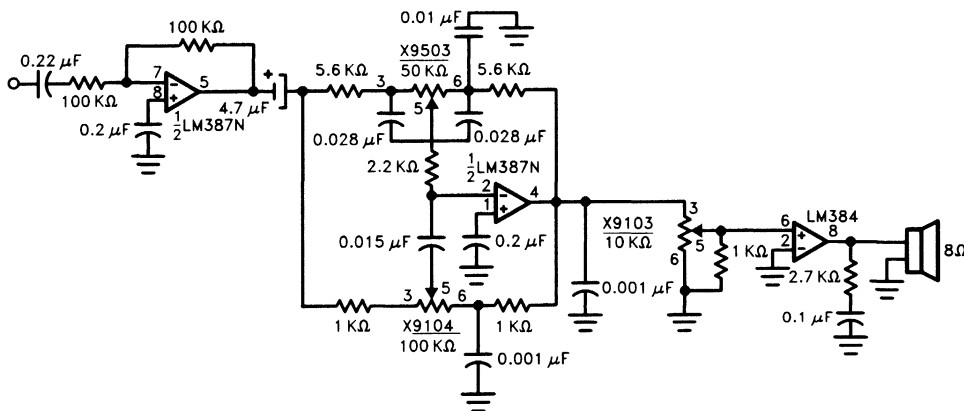


Figure 10: E2PREAMP with Three X9MME—No Digital Controls Shown



ground,  $U/\bar{D}$  to 5V and  $\overline{INC}$  pulsed with the clock. Each step of the clock produced a 1% change in wiper position. Figure 11 illustrates the switching network that was utilized for controlling all three X9MMEs.

This initial procedure allowed the analog portion of the design to be separated from the digital. Once the circuit was functioning adequately with the switch network controlling the X9MMEs, microprocessor interface was relatively simple.

## MICROPROCESSOR INTERFACE

With three devices on the board, 9 control lines are required. To simplify interface to an 8 bit microprocessor, the  $\overline{INC}$  lines for all three parts were connected to the same pin.

The pin configuration used for interface to the 6502 microprocessor system is as follows:

A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>
NC	$\overline{INC}$	$\overline{CS}_1$	$U/\bar{D}_1$	$\overline{CS}_2$	$U/\bar{D}_2$	$\overline{CS}_3$	$U/\bar{D}_3$

#1 = Volume  
#2 = Bass  
#3 = Treble

To move the wiper of a given pot, that pot's  $\overline{CS}$  is brought low, the  $U/\bar{D}$  for the appropriate pot is asserted H or L depending on the direction of wiper movement, and  $\overline{INC}$  is toggled. For example, to increase the volume the following two patterns are alternated to the port connected to the E<sup>2</sup>PREAMP.

NC	$\overline{INC}$	$\overline{CS}_1$	$U/\bar{D}_1$	$\overline{CS}_2$	$U/\bar{D}_2$	$\overline{CS}_3$	$U/\bar{D}_3$
1	0	0	1	1	1	1	1
1	1	0	1	1	1	1	1

Note that  $\overline{CS}$  has been selected,  $U/\bar{D}$  set to 1 and  $\overline{INC}$  toggled. Bass and treble settings are altered in a similar manner.

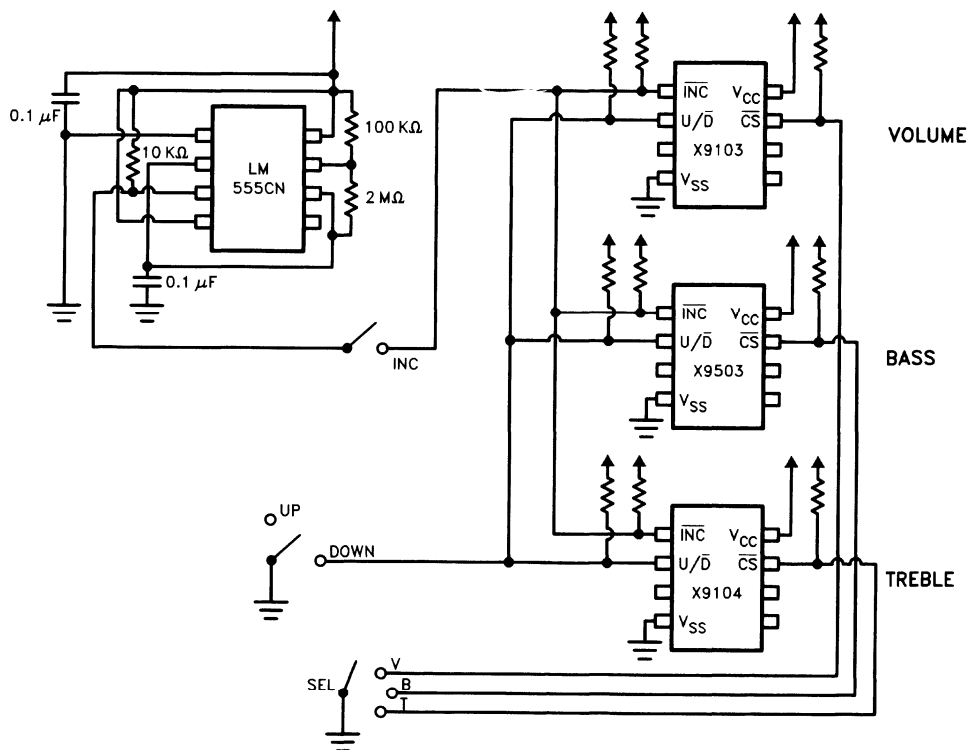


Figure 11: Switch Network for Manual Operation

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The microprocessor system used in the lab consists of a 6502 based keyboard monitor. The controlling program scans the keyboard for a recognized ASCII character which transfers control to the specified subroutine. For any given input, the appropriate increment is toggled 10 times before returning to the controlling program.

An example of a volume, bass, or treble adjusting program follows:

	LDX	#00	Load counter with zero
0333	LDA	0006	Load accumulator with first pattern
	STA	A000	Output pattern
	JSR	ED2C	5 ms wait
	LDA	0007	Load 2nd pattern
	STA	A000	
	JSR	ED2C	
	INX		
	CPX	0008	Compare counter to 10
	BNE	0333	
	RTS		

In addition to the adjustment subroutines, an initialization subroutine can also be called up. This subroutine sets the volume to zero and bass and treble to 50%. This is used to reset the controls. It would be used only during installation of the system.

This first section of the one time initialization program sets all pots to zero.

	LDX	#00	Load counter with zero
0111	LDA	0000	Load accumulator with first pattern (80h)
	STA	A000	Output pattern
	JSR	ED2C	5 ms wait
	LDA	0001	Load 2nd pattern (C0h)
	STA	A000	
	JSR	ED2C	
	INX		
	CPX	0008	Compare counter to 100
	BNE	0111	

This section sets the bass and treble pots to 50% and returns control to the controlling routine.

	LDX	#00	Load counter with zero
012C	LDA	0003	Load accumulator with first pattern (85h)
	STA	A000	Output pattern
	JSR	ED2C	5 ms wait
	LDA	0004	Load 2nd pattern (F5h)
	STA	A000	
	JSR	ED2C	
	INX		
	CPX	0005	Compare counter to 50
	BNE	0333	
	RTS		

## OPERATION AND PERFORMANCE

The E2PREAMP circuit operates much like many sophisticated home stereo systems today. All controls are digital switches—in this case, a keyboard for demonstration purposes only. There are no moving parts beyond the switches, and the entire system is relatively free from problems with vibration or jarring (potential hazards in mechanical pot systems).

Keys 1 through 6 on the keyboard represent the up down controls for the circuit. By depressing 1, the volume is increased by 10 steps. Key 2 decreases volume in the same way; 3 is treble up; 4 is treble down; 5 is bass up; 6 is bass down. The I key calls the initialization routine. Beyond allowing control of step size and the auto zero or initialize function, the present system does not take advantage of the versatility of microprocessor control.

Performance of the system was nearly identical to the same circuit with mechanical potentiometers. The X9MME is quiet to  $-65$  dB below a 1V signal, which is fair for audio quality devices. For audiophile quality, this number should be around  $-120$  dB, but in car stereo or communication equipment applications this device works adequately.

Aside from the obvious advantage of a lack of moving parts, the ability to choose step size in adjusting the controls has shown to be the most useful added feature. Ten steps per adjustment proved to be an easy value with which to work.

Having demonstrated the ability of the X9MME to replace mechanical potentiometers in analog circuits, more complex circuits may now be considered. With microprocessor control, advanced circuit design and digital control simply becomes an extension of the principles discussed so far.

Microprocessor control of this and other analog circuits is simple when utilizing a digitally controllable potentiometer. The gain of the entire circuit, or the boost or cut of a given frequency range is instantly alterable via microprocessor commands. Once control is assumed by the microprocessor, any parameter of the analog circuit that is controllable by a potentiometer is available to the programmer.

For example, the graphic equalizer/spectrum analyzer combination discussed earlier can easily be automated once microprocessor control is assumed. By controlling the position of potentiometers that control the gain of the individual equalizer bands, the system frequency response can be calibrated to any room or listening environment. Here is

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just one scenario: A "Calibration" button is depressed on the equalizing circuit. This activates a "pink" noise generator which sends a short burst of sound to the system. The spectrum analyzer in the system then decides which frequencies require adjustment, changes the positions on the appropriate potentiometers, and the system is calibrated. No sliders need to be adjusted; no separate (and expensive) spectrum analyzer; moreover, a relatively unsophisticated user can now perform an accurate environmental calibration of the system.

A simpler version of an auto calibration circuit could be incorporated into home and car stereos as a one time only installation adjustment. The scenario would be as follows. When a car stereo is first installed, the installer would push the calibration button on the back of the unit. This would adjust a compensation circuit, separate from the main tone controls. The settings would then remain in the non-volatile memory of the digital pots until the system were upgraded or installed into another car. Thus the same unit would be customized for different speakers, different amplifiers, and even different auto interiors.

## **X9MME ADVANCED FEATURES**

The Xicor device utilized in this design is suitable for audio applications, but it is a general purpose device that may be even better suited for other analog applications.

The X9MME has 99 steps across its range. In most audio applications, this high resolution is inaudible. However, when used in auto zero and balancing circuits, this resolution is invaluable.

The device's nonvolatile memory may be of limited use in some of the applications mentioned here, since a listener may not want to retain previous audio settings. But when used in a once-only calibration circuit, the nonvolatile memory eliminates any need for preventing a customer from changing the factory settings of a mechanical potentiometer. In a television cable decoder, for example, potentiometers abound. If cable companies used nonvolatile digital potentiometers in place of mechanical pots, the incessant headache of having to make adjustments because of jarred equipment or tampering could be eliminated.

The X9MME's convenient packaging and inherent digital control characteristics can be used to advantage on the assembly line. Manufacturing of devices requiring manual adjustment of potentiometers is always limited by the speed of the laborers and equipment used to set the pots. In addition, units often must remain partially assembled, or allow access holes for screwdriver adjustment of pots. The X9MME's conventional 8 pin DIP package can be automatically inserted with handlers used for other DIP devices, and trimmed to an appropriate value with an assembly line computer or by an internal microprocessor.

## **CONCLUSION**

Microprocessor control of analog circuits is now easier than ever. The X9MME from Xicor is more than a simple DAC. Not only can this device be used as a precision voltage source, it can replace any resistive element in nearly any analog circuit. Without altering existing analog circuit designs, the designer now has the ability to manipulate analog circuit functions with the digital potentiometer as his control element.

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## X28C010 Redundancy Repair

Richard Palm, Clifford Zitlaw, Edward Ng

### INTRODUCTION

As the leader in E<sup>2</sup> memory technology, Xicor has been the first to develop and offer many key features in response to our customers' needs. These include features which are now industry standards: RAM-like operation using only a single 5 volt supply, Page Mode Writes, Data and Toggle Bit Polling and Software Data Protect. With 1 Megabit and 512K level density E<sup>2</sup>PROMs, Xicor is offering an important new feature that allows in-system repair of failed bits and rows. This feature is easily accessible to the user through an extension of the JEDEC standard software data protection sequence.

The expected endurance of a typical X28C010 is well into the hundreds of thousands of cycles. However, a small percentage of devices might experience a single bit failure or possible half row failure during the expected useful lifetime. This would not normally be of concern in a system employing only a few devices or in a system that is rewritten infrequently. However, in a large memory array, frequently being updated, some form of row replacement may be needed to achieve the highest system reliability, regardless of the technology chosen.

All Xicor nonvolatile memories employ the Textured Poly Floating Gate (TPFG) technology, which uses a thick interpoly oxide layer for tunneling. This oxide layer is much more robust than the traditional thin oxides used for tunneling and has proven to be extremely screenable. That is, potential defective oxides (infant mortality candidates) can be detected and removed during the normal device test flows.

Manufacturers using the thin oxide technology, cannot screen for oxide breakdown because the tunneling voltage of the thin tunneling dielectric is very close to the breakdown voltage. Consequently, these manufactur-

ers have need of on-chip error correction circuitry. This is required to mask the unscreenable oxide breakdown failure mechanism. This method of masking failures works for single bit failures but does not address row failures. For more details, refer to *Comparison and Trends in Today's Dominant E2 Technologies*, a paper jointly published by Intel Corporation and Xicor, Inc.

### BACKGROUND

Xicor products have been used for years in data logging applications requiring high endurance. In working with its customers, Xicor has always recommended two basic concepts: spread the write operations evenly throughout the array (e.g. record data sequentially as it is made available); and provide some form of redundancy.

For data store applications the following redundancy scheme has been easily implemented: a few additional rows (pages as defined by the memory being used) are set aside as spares. After each page of data is written to the device a read-verify operation is performed: if the data compares correctly, the address is incremented and the next page is written. If at any time the data does not compare correctly, the failing row address is recorded in a nonvolatile lookup table and the page of data is then written to one of the extra rows. This requires maintaining a look-up table in a portion of the E<sup>2</sup>PROM.

Based on predicted single bit and row failure rates, Xicor has developed programs to determine system failure rates based on the array size and frequency of rewriting the array, both with and without redundant rows. The study shows that even in very large memory arrays just a few extra rows brings the system failure rate based on cycling oxide failures to an insignificant level, far below the failure rates for semiconductors due to other mechanisms.

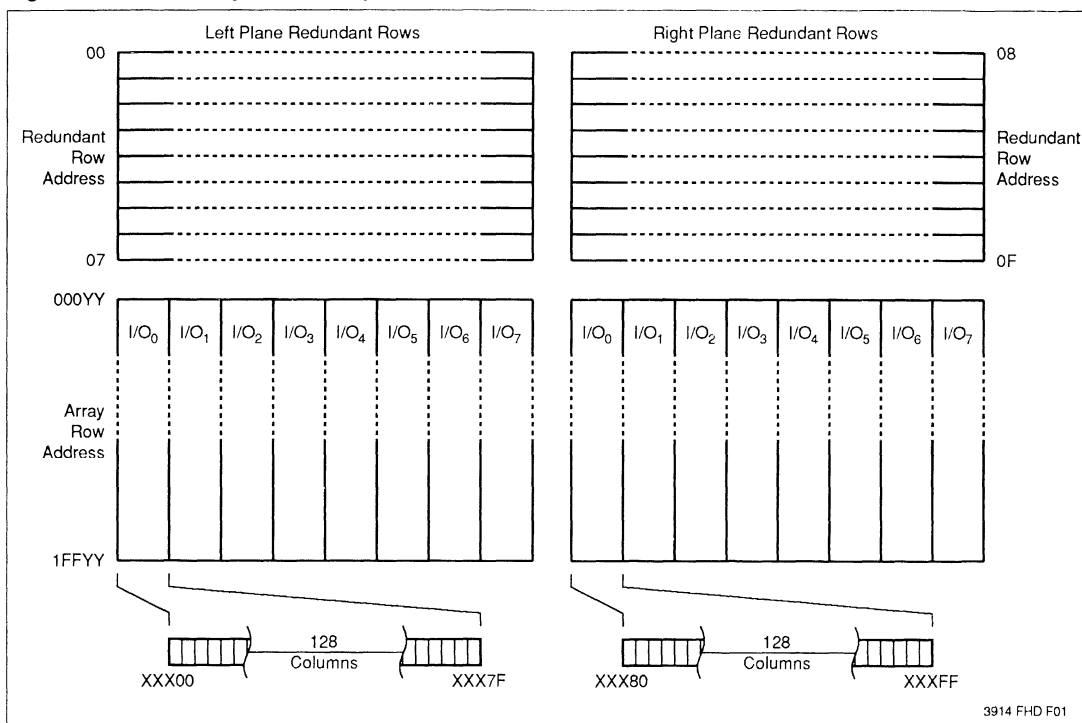
## X28C010 Redundancy Repair

### ARRAY ARCHITECTURE

The X28C010 contains two main array memory planes; the left plane and right plane, both configured 128 bytes wide by 512 rows deep. During normal read/write operations this split plane architecture is transparent to the user. As an example, the X28C010 provides a 256 byte page write capability. This page (address XXX00 to XXXFF, where X selects the page or row) spans both planes and the X28C010 independently, and transparently to the user, programs the data written to the memory into both planes.

In addition to the main array memory, each X28C010 contains 16 redundant rows of 128 bytes each; or 8 redundant rows for each array plane. Some of these redundant rows may be used by Xicor to repair failures detected within the main memory array during device screening. Redundant rows seven and eight in each half plane are reserved for end user repair. The split array architecture isolates one plane from the other. If an oxide failure occurs which disables a row in one plane, it does not affect the same row in the other plane. Therefore, the redundant rows need only be 128 bytes wide to facilitate a repair. Refer to Figure 1 below for a pictorial representation of the physical bit map.

Figure 1. X28C010 Physical Bit Map



### USING REDUNDANCY REPAIR

The redundancy repair feature of the X28C010 allows the user to swap out failed half rows and replace them with redundant half rows. The user accesses the redundancy repair mode with software that issues a special command sequence which is an extension of the software data protection sequence. The major advantages

of this repair capability are twofold: first, the user can design a system that is self-repairing in the field; second, since the repair is performed at the chip level, no address translation or look-up tables need to be examined and normal system throughput is maintained. This is extremely important in program store memory, where address continuity and fast access times are required to execute instructions properly.

# X28C010 Redundancy Repair

The following six step sequence is used to detect and replace a failed row with a redundant row:

- I) Failure Detection
- II) Enter Repair Mode
- III) Map Out Row If Redundant
- IV) Determine Which Rows Are Unavailable
- V) Select The Next Available Redundant Row
- VI) Swap Failed Array Row with Redundant Row
- VII) Exit Repair Mode

## I. Failure Detection

**Note:** All references to addresses and data will be represented in hexadecimal format. Other numeric values, such as numbers of rows or columns or bits are in decimal.

Determining the plane and row containing the failure is the first step. This is accomplished by performing either a standard byte or page write followed by a read-verify operation. If the data compares correctly no action is needed. If the data does not compare correctly, then the failing address location must be analyzed to determine which plane and row is failing. The state of A7 of the failing location indicates the plane in which the failure occurred: A7 LOW for the Left Plane; A7 HIGH for the Right Plane. The 9 most significant address bits (A8–A16) indicate the row in which the failure occurred (e.g. 000 = row 0 and 1FF = row 511) Refer to Figure 1 below, for a pictorial representation of the physical bit map of the main memory array

## II. Entering The Repair Mode

Once the failing plane and row have been determined, the system must access the repair mode. This is accomplished by issuing the six step SDP sequence illustrated in Figure 2. All the write operations within the sequence must conform to standard page write timings defined in the device specification.

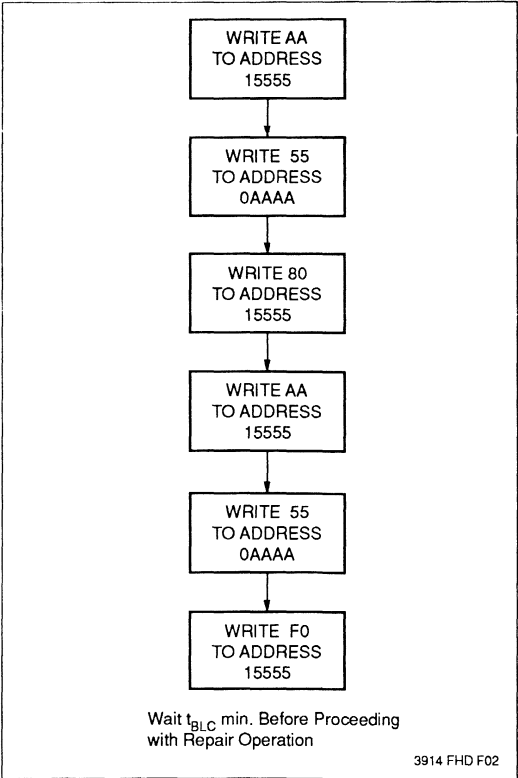
Upon entering the repair mode a number of functions are available to the user. Access to these functions is provided by either writing to or reading from specific addresses while in the repair mode. The functions are defined in Table 1 of appendix A.

## III. Map Out Row If Redundant

The row status of any row being repaired should be 07. If any other row status condition is returned, it indicates that the failure is in a redundant row which has already been replaced in the array. This row must first be removed, then replaced with another redundant row.

To remove this redundant row, perform a write of any data to address XXXR0H: R<sub>H</sub>=the actual redundant row address (0–F) as detected during the scan operation; XXX<sub>H</sub> = the array row address (000–1FF). This operation is a nonvolatile write and a 10ms (t<sub>WC</sub>) wait is required before proceeding with the repair. The redundant row should also be disabled to preclude its use in the future. This is done by writing data 00 to address 000R8: where R = the actual redundant row address (0–F). Again, this is a nonvolatile write operation and requires a 10ms (t<sub>WC</sub>) delay.

Figure 2. SDP Entry Into Repair



# X28C010 Redundancy Repair

## IV. Building A Redundant Row Status Byte

After entering the repair mode, two features are used to build a table describing the status of each redundant row. First, the redundant row status register is used to find out which redundant rows may have been disabled either at the factory or by the end user. Second, the array row scan function is used to determine which rows may have already been used for repair.

## 1. Redundant Row Status

Each plane has a redundant row status register which can be read in the repair mode. Depending on the plane being repaired, perform a read operation at either address 0003F (left plane) or address 000BF (right plane). I/O<sub>0</sub>–I/O<sub>7</sub> will return status bits indicating whether the redundant rows are disabled or are not disabled. I/O<sub>0</sub>–I/O<sub>7</sub> corresponds directly to a redundant row number for the selected plane, (I/O<sub>0</sub> = RR<sub>0</sub> and I/O<sub>7</sub> = RR<sub>7</sub>). A logic “1” indicates disabled and a logic “0” indicates not disabled. Disabled rows are not available for mapping into the array.

## STATUS TRANSLATION TO REDUNDANT ROW ADDRESS

Left RR Status	Actual RR Address	Right RR Status	Actual RR Address
0000 0000	N/A	0000 0000	N/A
XXXX XXX1	01	XXXX XXX1	08
XXXX XX1X	02	XXXX XX1X	09
XXXX X1XX	03	XXXX X1XX	0A
XXXX 1XXX	04	XXXX 1XXX	0B
XXX1 XXXX	05	XXX1 XXXX	0C
XX1X XXXX	06	XX1X XXXX	0D
X1XX XXXX	07	X1XX XXXX	0E
1XXX XXXX	08	1XXX XXXX	0F

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For example:

Read Address	Data Returned	Status
0003F	02	Left Plane RR <sub>0</sub> and RR <sub>2</sub> –RR <sub>7</sub> not disabled, RR <sub>1</sub> Disabled
000BF	48	Right Plane RR <sub>E</sub> and RR <sub>B</sub> disabled, other RRs not disabled

The value in the redundant row status register, for the half plane to be updated, can be placed in a status byte to track which redundant rows are not available for

mapping into the array. The bits in this status byte indicate the availability of each redundant row, with a 1 indicating the redundant row is not available.

# X28C010 Redundancy Repair

## 2. Scanning Array Row Status

The next step is to scan all the rows in the plane to be repaired to determine the status of individual main array rows (already replaced or original) and to determine which redundant rows are already used. This is accomplished by reading the row status register for each row within the plane. This read conforms to the read timing characteristics defined in the device specification.

Individual row status is determined by reading the row status register. The 8 LSBs of the address (these are the column address) during the status scan will remain the

same; only the 9 MSBs (row addresses) of the address need be incremented from 000 to 1FF. To read the left plane status the 8 LSBs should be 49 and to read the right plane should be C9.

For example to scan the left plane, the sequence would begin by reading 00049, then 00149, 00249 . . . . 1FE49, 1FF49. To scan the right plane the sequence would begin by reading 000C9, then 001C9, 002C9 . . . . 1FEC9, 1FFC9. The status returned is contained in the 4 LSBs (I/O<sub>0</sub> I/O<sub>3</sub>). The decoding of this information is as follows:

I/O <sub>3</sub> –I/O <sub>0</sub>	Left Array Redundant Row Status	Right Array Redundant Row Status
0XXX	Row Currently Scanned is the original	Row Currently Scanned is Original
1000	Row Currently Scanned is replaced by RR 00	Row Currently Scanned is replaced by RR 08
1001	Row Currently Scanned is replaced by RR 01	Row Currently Scanned is replaced by RR 09
1010	Row Currently Scanned is replaced by RR 02	Row Currently Scanned is replaced by RR 0A
1011	Row Currently Scanned is replaced by RR 03	Row Currently Scanned is replaced by RR 0B
1100	Row Currently Scanned is replaced by RR 04	Row Currently Scanned is replaced by RR 0C
1101	Row Currently Scanned is replaced by RR 05	Row Currently Scanned is replaced by RR 0D
1110	Row Currently Scanned is replaced by RR 06	Row Currently Scanned is replaced by RR 0E
1111	Row Currently Scanned is replaced by RR 07	Row Currently Scanned is replaced by RR 0F

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As an example, assume a scan of the left plane with the following status returned.

Address	Data	Interpretation
00049	07	Original Main Memory Row 0 [D]
00149	07	Original Main Memory Row 1 [D]
00249	08	Original Main Memory Row 2 [D], Replaced by Redundant Row 0
00349	07	Original Main Memory Row 3 [D]
⋮	⋮	⋮
1FD49	09	Original Main Memory Row 253 [D], Replaced by Redundant Row 1
1FE49	07	Original Main Memory Row 254 [D]
1FF49	07	Original Main Memory Row 255 [D]

When a row is found to be redundant the corresponding bit in the status byte is set to indicate that the row is not available for a repair operation.

## V. Select Available Redundant Row

The redundant row status byte now indicates all redundant rows which are disabled and / or not mapped into the array. The address R of the next available redundant row

(row 7 or row 8) can now be selected for use in step VI by searching the status byte for rows that are not disabled or mapped into the array. A redundant row acceptable for mapping is indicated by a 0 in the status byte.



# X28C010 Redundancy Repair

## VI. Replace Array Row With Redundant Row

To replace a row in the array with a redundant row, write any data to  $XXXR4_H$ ; where  $XXX_H$  = the array row address to be swapped out;  $R_H$  = the redundant row address to be swapped in on address lines  $A_4$ – $A_7$ ; and  $4_H$  = the command to exchange rows on address lines  $A_0$ – $A_3$ . During the actual repair operation the array row address does not specify the plane being repaired. The most significant bit of the redundant row address controls this: that is, when  $R = 0$ – $7_H$  the left plane is being repaired and when  $R = 8$ – $F_H$  the right plane is being repaired. For example:

Repair array row 0 (left plane) with the seventh redundant row for that plane, write  $XX$  to  $00064$

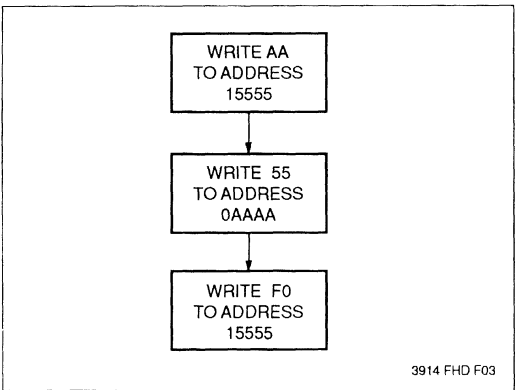
Repair array row 0 (right plane) with the eighth redundant row for that plane, write  $XX$  to  $000F4$

Note: This is a nonvolatile write operation and must be followed by a 10ms ( $t_{WC}$ ) wait before exiting this routine.

## VII. Exit Repair Mode

To exit the repair mode and return to normal system operation issue the command sequence illustrated in Figure 3.

Figure 3. SDP Exit from Repair



## SUMMARY

This paper has illustrated how a system can use the redundancy repair feature in the X28C010 for in the field repairs. Whenever the E<sup>2</sup>PROM is written, software routines automatically detect a failing bit or row, perform a repair operation and return to normal system operation. Since the repair is handled automatically as part of the software for writing to the E<sup>2</sup>PROM, its operation can be totally transparent to the rest of the system. Flow charts for this sequence of operations are shown in Appendix A and a software routine used to verify all the information in this paper is shown in Appendix B.

Appendix A

Figure 1. Basic Repair Flow

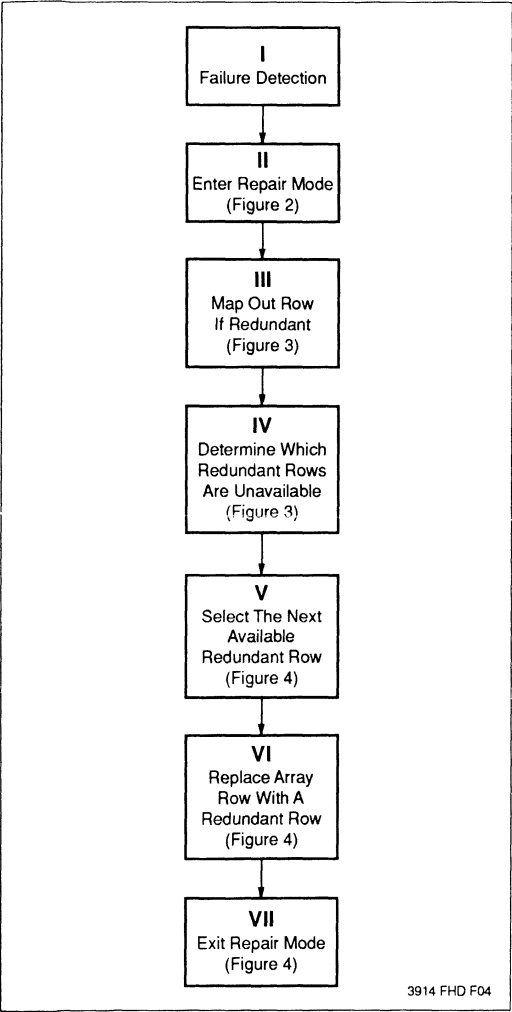
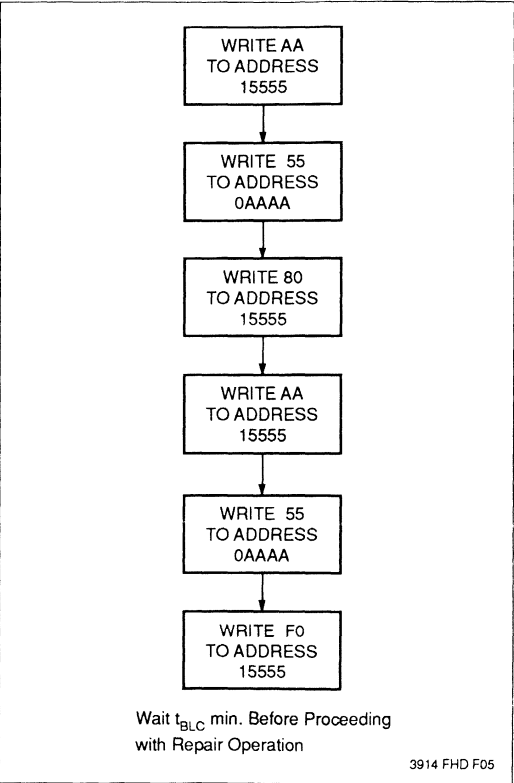
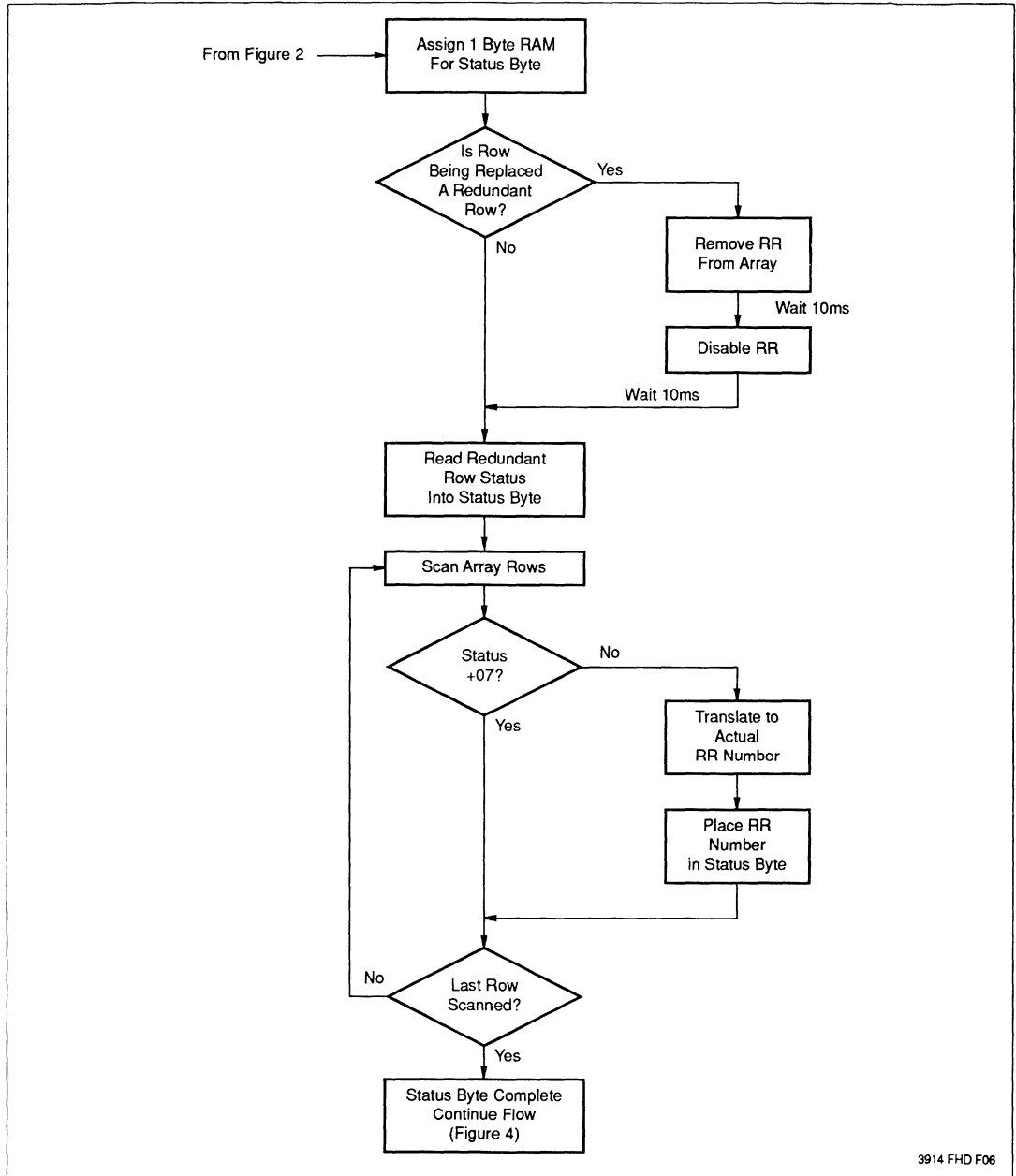


Figure 2. SDP Entry into Repair



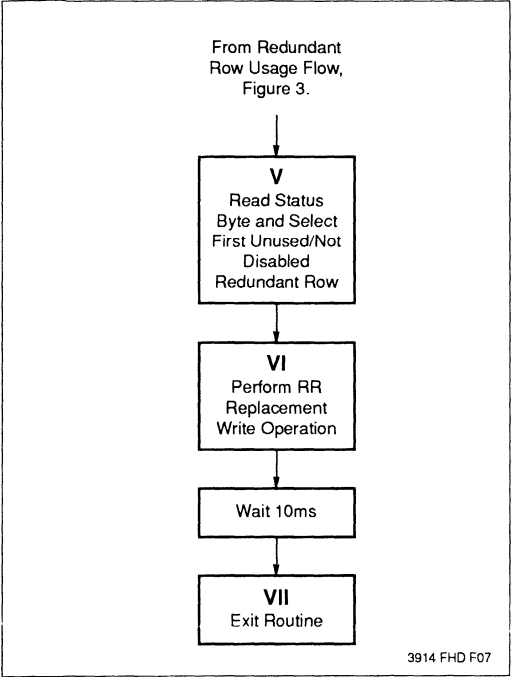
## X28C010 Redundancy Repair

Figure 3. Building a Redundant Row Status Byte



# X28C010 Redundancy Repair

Figure 4. Select, Repair and Exit Flow



## **X28C010 Redundancy Repair**

---

### **NOTES**

### Appendix B

---

```
/******  
/* This routine takes as input the address of a row to be replaced by  
/* redundancy. The specified row is replaced by a redundant row (if  
/* available). If the replacement is successful the routine returns  
/* the number of the redundant row mapped in, otherwise $FF is returned  
/* if no redundant rows were available.  
/*  
/* Points of interest :  
/*  
/* An "unsigned long" variable is a 32 bit integer. This type must be  
/* used because the 17 bit addressing on the 28C010 is greater than the  
/* normal 16 bit integer declaration.  
/*  
/* The key to understanding this routine is the usage of the variable  
/* "status". "status" is used to determine which redundant rows are  
/* available for replacement in the array. The bits in "status"  
/* indicate the state of the eight redundant rows (0 - row available,  
/* 1 - row not available for remapping). Each bit represents the state  
/* of one of the redundant rows (bit 0 - redundant row 0). To find  
/* which rows are available the routine looks at the "redundant row  
/* status register" which identifies bad redundant rows. Note that  
/* this register does not identify redundant rows that are being used  
/* in the array. Next the array is scanned to find any redundant rows  
/* that are being used. If a redundant row is found the corresponding  
/* bit is set in "status". After this two step sequence is followed  
/* variable "status" can be used to find a redundant row that is  
/* available to map into the array. If all redundant rows are used the  
/* routine exits the routine and passes back $FF. If a redundant row is  
/* available the row is mapped in and the routine passes back the row  
/* number that was used.  
/*  
/* The routines "shallow()" and "deep()" are used for the three and  
/* five step SDP sequences respectively. The parameter passed is  
/* written during the last step of the sequence.  
/*  
/* The routine "delay()" performs a pause for the number of milli-  
/* seconds indicated in the pass parameter.  
/******
```

```
unsigned char mapping(unsigned long bad_add) {
```

```
    unsigned char status;           /*redundant row usage byte*/  
    unsigned long row_add;          /*address pointer*/  
    int count;                      /*loop counter variable*/  
    unsigned char tdat;             /*temporary byte variable*/
```

## X28C010 Redundancy Repair

---

```
deep(0XF0); /*enter redundancy with*/
delay(20); /* 5 step SDP sequence*/
row_add = bad_add & 0x1FF80; /*generate mask to determine if*/
row_add = row_add | 0x00049; /* the bad address is redundant*/
tdat = read_byte(row_add);
if ((tdat & 0x08) != 0) { /*map bad row out if redundant*/
    row_add = bad_add & 0x00080; /*generate mask to map out*/
    tdat = tdat & 0x07; /* bad row*/
    tdat = tdat << 4;
    row_add = row_add | tdat;
    row_add = row_add | 0x00008;
    write_byte(row_add, 0x00); /*mask out bad row, this sets*/
    delay(20); /* the row's status reg bit*/
}
if ((bad_add & 0x00080) == 0) { /*read redundant status reg*/
    row_add = 0x00049; /* address to start array check*/
    status = read_byte(0x0003F);
}
else {
    row_add = 0x000C9;
    status = read_byte(0x000BF); /*0s in "status" indicate that*/
} /* the row is available*/
for (count = 1; count <= 512; count++) { /*see what redundant rows are*/
    tdat = read_byte(row_add); /* used in the array*/
    if ((tdat & 0x08) != 0) { /*set status bit if a redundant*/
        tdat = tdat & 0x07; /* row is found*/
        status = status | (0x01 << tdat);
    }
    row_add = row_add + 256; /*step to check next row*/
}
status = status | 0X03F; /*only use rows 6 and 7*/
if (status != 0xFF) { /*if no redundant rows are*/
    row_add = 0; /* available then exit*/
    while ((status & 0x01) != 0x00) { /*find an available*/
        status = status >> 1; /* redundant row (look for */
        row_add = row_add + 1; /* first 0 in "status"*/
    }
    row_add = row_add << 4; /*generate a mask to map in*/
    bad_add = bad_add & 0x1FF80; /* the new redundant row*/
    bad_add = bad_add | 0x00004;
    bad_add = bad_add | row_add;
    write_byte(bad_add, 0x00); /*map in redundant row*/
    delay(20);
    status = (bad_add >> 4) & 0x0000F; /*save the redundant row #*/
}
shallow(0XF0); /*leave redundancy with*/
delay(20); /* 3 step SDP sequence*/
return(status); /*return with row number or $FF*/
} /* if no rows are available*/
```



# Application Brief

## NONVOLATILE DATA INTEGRITY: INADVERTENT WRITE/STORE ELIMINATION

By Applications Staff

Xicor's nonvolatile memory products are backed by designed-in protection features which ensure data integrity. These include:

- **Onboard  $V_{CC}$  Sensor**  
All operations inhibited when  $V_{CC} \leq 3.0V$ .
- **Noise Filter**  
A feature which blocks noise spikes on control lines.
- **Orderly Power Transition**  
The device will not self-generate inadvertent write/store operations.
- **Write/Store Inhibited Control Pins**  
Multi-pin write/store command signal requirements provide both data security and design flexibility.

### New Design Features

- Software Write Protection
- Previous Recall Latch
- Command Sequence

With Xicor nonvolatile memories, data is maintained through power-on, power-off, power-down, system crash, and the entire range of system conditions when some simple design rules are observed. Often nonvolatile system designers are frustrated by inadvertent system command signals during power-up and power-down operations. Being nonperiodic in nature, these elusive culprits can lead the designers to the false conclusion that the memory device is malfunctioning. This, however, is rarely the case. The system is more often sending an unintended write/store command. This problem can be easily resolved as shown in this application brief.

### GIGO<sup>1</sup> Going to Sleep

Just as a person falling asleep at the wheel can inadvertently command his vehicle into an undesirable situation, digital systems transitioning from normal operation to a power-off state or vice versa can distribute random data, addresses, and control signals along the way.

Since Xicor nonvolatile memories accurately and reliably store data as instructed, data stored at power-down will be impeccably retained and available upon power-up. (That's nonvolatile GIGO.)

### Protection-Conscious Design

Data integrity is a major criterion with Xicor products and several superb features were designed into Xicor's memories to ensure it.

- **$V_{CC}$  Sensor**  
An onboard sensor establishes a threshold supply voltage of 3.0V below which write operations on E<sup>2</sup>PROMs and store operations on NOVRAMs are blocked. Above this voltage, write and store operations are available and therefore must be protected from unplanned instructions.
- **Orderly Supply Transitions**  
As a system powers up or down, the possibility of unintentional, internally generated control signals increases dramatically. The Xicor nonvolatile memory family has designed-in protection to eliminate self-generated write/store commands.
- **Noise Filter**  
An additional feature designed into Xicor's E<sup>2</sup>PROM family is a noise filter to prevent glitches on the WE line from initiating a write cycle. This feature filters pulses of less than 20ns duration insuring noise spikes are not misconstrued as write commands.



### ■ Write/Store Inhibit Control Pins

Xicor nonvolatile memories require combinational control pin conditions in order to execute a write/store command. By disallowing any one of the required pin conditions, the user can prevent unplanned nonvolatile data changes so that data integrity is maintained.

## Write/Store Pin Conditions

ARRAY RECALL <sup>2</sup>	STORE	STORE CAPABILITY
X	H	STORE OPERATION DISABLED
L	X	ARRAY RECALL BLOCKS STORE INITIATION (SEE FOOTNOTE 2)
H	L	STORE OPERATION EXECUTED <sup>3</sup>

Figure 1: X2200 NOVRAM Family

CE	OE	WE	WRITE CAPABILITY
X	X	H	(WE) WRITE INHIBIT*
X	L	X	(OE) WRITE INHIBIT
H	X	X	(CE) WRITE INHIBIT
L	H	L	WRITE OPERATION EXECUTED <sup>3</sup>

\* Hard to control during power cycling.

Figure 2: E<sup>2</sup>PROM Family

The Intersil<sup>4</sup> ICL 8211 programmable voltage reference is an inexpensive 8-pin mini DIP which will sense a selected voltage threshold and output a logic "0" when the supply is below that threshold. Conversely, as the sensed voltage rises above the selected threshold, the 8211 outputs a logic "1" following its supply voltage level.

### Solution II—"Hold-High" Protection

The second method of data protection during power supply transitions is to keep the NOVRAM STORE pin (or the WE and/or CE pins in the E<sup>2</sup>PROM family) near the power supply voltage. By preventing the low condition of these pins which is necessary for a write or store operation, inadvertent stores will be eliminated.

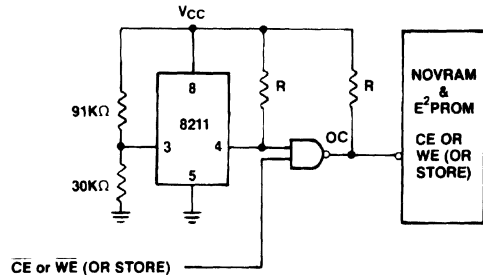


Figure 4: "Hold-High" Protection

## External Hardware Implementations

### Solution I—"Hold-Low" Protection

The simplest solution is to pull the  $\overline{OE}$  (or ARRAY RECALL) to a logic "0" whenever the supply voltage is below the (5.0-10%) system threshold.

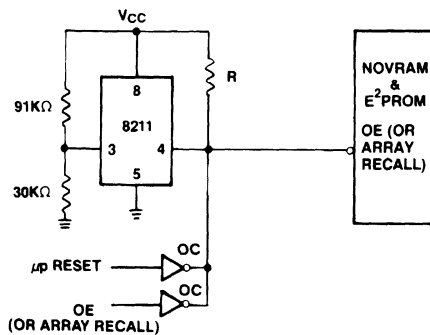


Figure 3: "Hold-Low" Protection

The graph in Figure 5 shows the performance of the Intersil ICL 8211. The top plot is a sawtooth which is connected to "5V supply" as shown in the Solution I and Solution II schematic diagrams. The bottom plot is the output of the ICL 8211. Note that when the supply is above 4.50V, the ICL 8211 output tracks it at logic "1". When the supply sawtooth is below 1.56V, the ICL 8211 output tracks the power supply. However, since the Xicor memory family has internal protection inhibiting write/store operations when  $V_{CC}$  is below 3V, no inadvertent write/stores will occur in this range. In the critical range between 3V, where internal protection stops, and 4.5V, where normal operation begins, the ICL 8211 insures a 0V output.

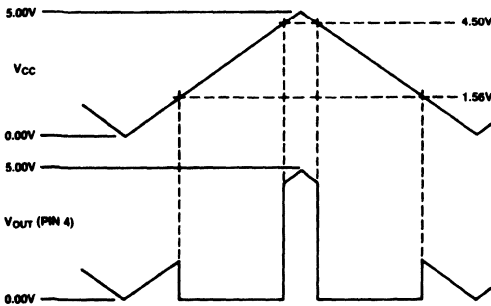


Figure 5: Intersil ICL 8211 Programmable Voltage Reference/Supply and Output Waveforms

As an alternate approach to the 8211, some designers may prefer to incorporate the SGS L487. This device is a 500 mA precision 5V voltage regulator which includes an open collector power-on, power-off reset output pin, which can protect the nonvolatile memories just as the 8211 does. The timing diagram in Figure 6 shows the voltage on this reset output pin as the supply voltage transitions through power-up and power-down.

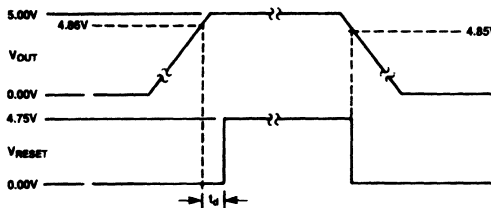


Figure 6: SGS L487 Precision Voltage Regulator/Output and Reset Waveforms

## New Protect Features

### Serial Device Protection X2444

A Previous Recall latch and Write Enable latch have been incorporated in the X2444 Serial NOVRAM.

Upon power-up, both latches will be in the reset state. Both latches must be set in order to enable either a write RAM operation or store to E<sup>2</sup>PROM operation.

A recall operation copies data from the E<sup>2</sup>PROM array into the RAM array. This operation places known data in all RAM locations and sets the previous recall latch. This prevents the user from inadvertently writing one word to RAM and performing a store operation with unknown data in all other locations.

The WREN instruction sets the Write Enable latch, enabling (if the Previous Recall latch is set) write and store operations. The WRDS instruction resets the latch, disabling write and store operations.

Therefore, total data integrity can be maintained through the use of software commands. The device is inherently protected during power-up and, through proper software control, is protected during power-down.

### X2404 Serial E<sup>2</sup>PROM

Due to the nature of the software protocol involved in writing to the X2404, inadvertent stores are highly unlikely. During power-up or power-down the possibility of the bus duplicating the start condition, slave address and transmitting data successfully is so remote as to be unmeasurable.

### Software Write Protection

Future E<sup>2</sup>PROM products will contain a register which is accessible through a software sequence algorithm. This feature provides the user control in selecting the level of write protection required by their application. Refer to the X28256 data sheet for details.

Figure 7 indicates the write protection features incorporated in all Xicor products.

GENERIC DEVICE TYPE	V c c  S E N S E	N O I S E  F I L T E R	S E L F - P R O T E C T E	I N H I B I T  C O N T R O L	P R E V I O U S  R E C A L L	S O F T W A R E  P R O T E C T I O N	C O M M A N D  S E Q U E N C E
X2201A	X	X	X	X			
X2210	X	X	X	X			
X2212	X	X	X	X			
X2001	X	X	X	X			
X2004	X	X	X	X			
X2444	X	X	X	X	X		
X2804A	X	X	X	X			
X2816A	X	X	X	X			
X2816B	X	X	X	X			
X2864A	X	X	X	X			
X2864B	X	X	X	X			
X2864H	X	X	X	X			
X28256	X	X	X	X		X	
X28C256	X	X	X	X		X	
X2404	X	X	X	X			X
X24C04	X	X	X	X			X
X24C16	X	X	X	X			X

Figure 7: Product Protection Matrix

### Footnotes

- <sup>1</sup> GIGO is an acronym popular in the computer world for "Garbage In Garbage Out".
- <sup>2</sup> ARRAY RECALL blocks all control inputs but does not halt a store in process.
- <sup>3</sup> These are the *only conditions* allowing nonvolatile data change.
- <sup>4</sup> See Intersil ICL 8211, ICL 8212 Programmable voltage reference data sheet in Intersil Data Book.

# REPLACING DIP SWITCHES WITH NONVOLATILE TECHNOLOGY

By Rick Orlando

One of the most prevalent applications for small nonvolatile memories is that of replacing DIP switches. The advantages of the nonvolatile memories is clear. They take up less room, are easier to use, and lend themselves to automated board assembly. 256 bits of information, or the equivalent of 32, 8-bit DIP switches can be implemented in a single package.

Xicor's new X2444 Serial NOVRAM adds yet another feature—low cost. When coupled with the serial device's minimal interface requirements, the X2444 takes DIP switches head on, and is obviously the cost/performance leader. The purpose of this brief is to describe how easy it is to replace a DIP switch with an X2444 NOVRAM.

## DIP Switch Interface

There are two common types of DIP switch interfaces.

## I/O Port

The first uses an I/O port with internal pullup resistors. Figure 1a shows a typical circuit that could be used either with a single chip microcomputer or with an I/O port on a microprocessor bus. In either case, the internal pullups present a logic "1" to the input as long as the DIP switch is open. To use an X2444 Serial NOVRAM in the DIP switch socket, one only needs to tie pins 14, 15, and 16 of the 16-pin socket to  $V_{CC}$ .

One then plugs an X2444 part in the uppermost half of the socket, and the circuit becomes that shown in Figure 1b.  $V_{CC}$ , STORE, and RECALL are tied hard to 5 volts, so that all nonvolatile operations are controlled through software. The four interface lines from the X2444 are connected to the four least significant I/O lines of the port.

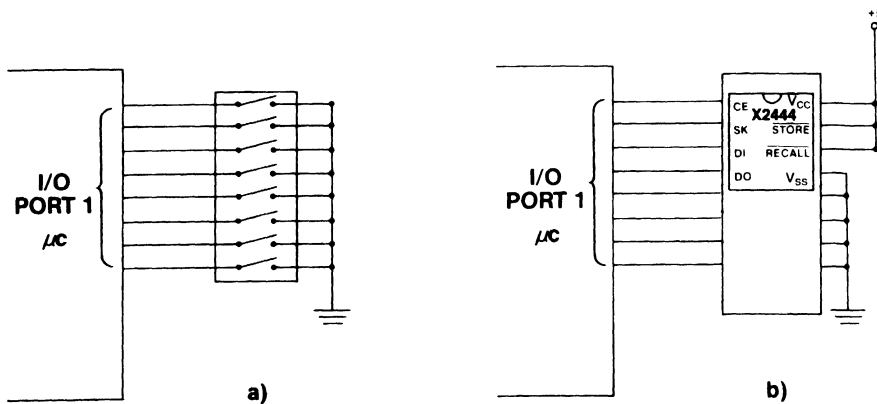


Figure 1. Microcomputer with Internal Pullups

## No Internal Pullups

The second type of interface uses ports which do not have internal pullups. In this instance, the X2444 can be plugged into the top section of the pullup resistor socket, with a jumper from pin 13 of the 16-pin site to ground, for the  $V_{SS}$  on the serial part.

Again,  $V_{CC}$ , STORE, and RECALL are tied to +5V through the connections used for the resistor pack. The DIP switch socket simply remains empty. See Figure 2.

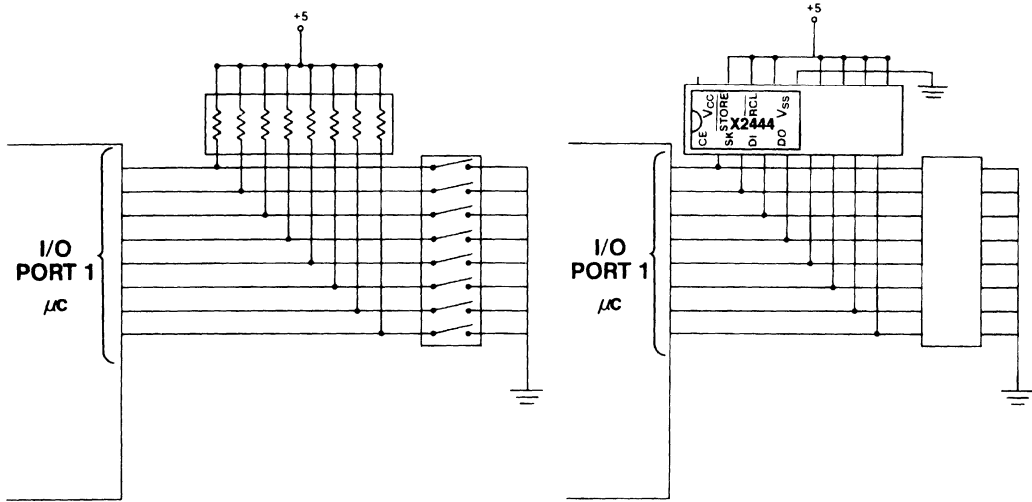


Figure 2. Microcomputer without Internal Pullups

Both of these implementations free up four more I/O lines to be used elsewhere. They also require the same software to drive the X2444.

Assume that the processor is a 6801 with the X2444 replacing a DIP switch. The procedure "INIT" initializes the port (see Section 1, "X2444 Driver Program for 6801").

Serial output is accomplished by loading the data to be output into the A Accumulator. A loop routine then shifts a bit into the carry, sets the serial data out (Data in for X2444) to either a "1" or "0" depending upon the state of the carry and toggles the clock.

(See Section 2 Procedure "SHIFT1" of X2444 Driver Program for further details).

The serial input is performed by a loop which examines the state of the serial data in, (Data out for X2444) sets the carry accordingly, shifts the carry into the accumulator and toggles the clock. (See Section 3 Procedure "SHIFTIN" of X2444 Driver Program for further details).

The complete software is as follows, and it occupies about 100 bytes of code. As one can see, the X2444 is indeed a value replacement for DIP switches.

```

; *****
;                               6801 X2444 DRIVER
;
;   ASSUME THAT PORT1 IS USED AS THE 2444 INTERFACE
;   PORT1'S REGISTERS ARE LOCATED AS FOLLOWS
;
;   DATA DIRECTION      HEX 0000
;   PORT                  HEX 0002
;
;
;   I/O 0      PORT1      SERIAL CLOCK      X2444
;   I/O 1      SERIAL OUT  SERIAL IN
;   I/O 2      SERIAL IN   SERIAL OUT
;   I/O 3      2444 SELECT  CHIP SELECT
;
;
;   COMMANDS ARE PASSED TO THE X2444 ROUTINE BY A PARAMETER IN THE
;   A ACCUMULATOR, WHILE THE ADDRESS IF NEEDED IS PASSED ON THE STACK
;   SERIAL DATA IN OR OUT USES THE TEMPORARY LOCATION TEMP1,
;   WHICH IS A SIXTEEN BIT WORD.  THE X2444 COMMANDS ARE ENCRYPTED AS
;   FOLLOWS.
;
;   COMMAND CODE      INSTRUCTION      OPCODE
;   0      READ      1AAAA11X
;   1      WRITE     1AAAA011
;   2      RSTFT WRITE ENABLE 11111000
;   3      STORE     11111001
;   4      SLEEP     11111010
;   5      SET WRITE ENABLE 11111100
;   6      RECALL    11111101
;
;   *1*' ARE USED INSTEAD OF DON'T CARE TO DISTINGUISH BETWEEN DATA AND
;   NON DATA OPERATIONS.
; *****

```

```

DIRECTION1 .EQU 00.
PORT1 .EQU 02.
TEMP1 .EQU 080H ;RAM STORAGE FOR DATA
COUNT .EQU 082H ;COUNTER VARIABLE
DATUM .EQU 084H ;DATA STORAGE
ADDRESS .EQU 086H ;ADDRESS STORAGE
ERRORDATA .EQU 088H ;ERROR DATA

```

## Section 1

```

; *****
;   PROCEDURE INIT
;
;   THIS PROCEDURE INITIALIZES THE X2444 INTERFACE
; *****
INIT  LDAA  $18H      ; E=1011, I/O 0-1 AND 3 OUTPUTS, 2 INPUT
      STAA  DIRECTION1 ; WRITE TO DATA DIRECTION REGISTER
      CLRA
      STAA  PORT1     ; SET CL TO 0 (INACTIVE), DOUT AND SR TO 0
      RTS

```

## Section 2

```

; *****
;   SHIFTER ROUTINE- SHIFT1
;
;   THIS ROUTINE TAKES THE DATA IN THE A ACCUMULATOR AND CLOCKS IT MOST
;   SIGNIFICANT BIT FIRST INTO THE X2444.  THE FLOW IS SHIFT A BIT, TOGGLE
;   THE SERIAL OUTPUT(6801) ACCORDING TO STATE, AND TOGGLE SERIAL CLOCK
; *****
SHIFTOUT  LDAB  $08.      ;LOAD THE BIT COUNT WITH 8
          STAB  COUNT      ;STORE IN COUNTER
SHIFT1    ROLA      ;SHIFT BIT INTO CARRY BIT
          LDAB  $14H      ;WE SET DATA OUT TO ZERO, WHILE GETTING CHIP
                          ;ENABLE.  SERIAL CLOCK IS LOW.
          BCC  TRANS      ;IF BIT IS A ZERO, THEN TRANSMIT
          ORAB  $02H      ;IF IT IS A ONE, THEN SET DATA OUT
          STAB  PORT1     ;STORE THE DATA INTO THE PORT
          ORAB  $01H      ;AND SET THE CLOCK FOR A TRANSITION
          STAB  PORT1     ;BY WRITING A 1 TO SERIAL CLOCK
          ANDB  $1AH      ;KEEP THE DATA VALID, BUT SET SR TO ZERO
          STAB  PORT1     ;AND STORE IN THE PORT
          LDAB  $14H      ;TOGGLE CLOCK DOWN, SET DOUT TO 0, BUT KEEP
          STAB  PORT1     ;X2444 SELECTED
          DEC  COUNT      ;DECREMENT THE BIT COUNTER
          BNE  SHIFT1     ;IF COUNT IS NOT ZERO, TRANSMIT NEXT BIT
          ROLA      ;ONE MORE ROTATE TO PREPARE INSTRUCTION
          RTS      ;RETURN FROM SUBROUTINE

```

## Section 3

```

; *****
;   SHIFTER ROUTINE
;
;   THIS SUBROUTINE SHIFTS IN 8 BITS OF DATA INTO THE A ACCUMULATOR FROM THE
;   X2444.  THE METHOD IS TO ENTER WITH THE CLOCK LOW, TOGGLE THE SERIAL CLOCK,
;   EXAMINE THE INPUT DATA, AND SHIFT IT INTO THE A ACCUMULATOR.  THIS IS DONE
;   8 TIMES.  THE ROUTINE IS EXITED WITH THE CHIP DESELECTED, AND THE BYTE
;   READ FROM THE CHIP IN THE A ACCUMULATOR
; *****
SHIFTIN  LDAB  $8.      ;LOAD THE BIT COUNT
          STAB  COUNT      ;AND STORE IT IN THE COUNTER
          ;AT THIS POINT THE X2444 SHOULD BE SELECTED
          ;THEREFORE, WE DO NOT NEED TO SELECT CHIP
          NEXT  LDAB  $04      ;MASK BIT FOR I/O 2 OF PORT
          BITE  PORT1      ;CHECK TO SEE IF INPUT IS A ONE OR ZERO
          CLC      ;CLEAR THE CARRY
          BFC  CLOCK      ;IF IT IS A ZERO, LEAVE CARRY AT 0
          SEC      ;OTHERWISE SET CARRY TO LOAD INTO A
          CLOCK  LDAB  $15H      ;SEND A CLOCK TO X2444, BUT KEEP CHIP SELECT HIGH
          STAB  PORT1      ;BY WRITING A 1 TO SERIAL CLOCK OUTPUT
          LDAB  $14H      ;SET UP TO CLEAR CLOCK, BUT KEEP X2444 SELECTED
          STAB  PORT1      ;AND STORE
          ROLA      ;ROTATE CARRY INTO LSB OF ACCUMULATOR A
          DEC  COUNT      ;DECREMENT COUNTER
          BNE  NEXT      ;IF NOT ZERO, THEN WE ARE NOT DONE, GET NEXT
          RTS      ;AND RETURN FROM SUBROUTINE

```

```

;*****
; X2444 DRIVER ROUTINE
; IT IS ASSUMED THAT THE INSTRUCTION IS PASSED IN THE A ACCUMULATOR.  AN
; ADDRESS, IF NEEDED, IS PASSED ON THE STACK (CURRENT SP-2)
; DATA TO BE READ OR WRITTEN WILL BE HELD IN TEMP1
;*****
DRIVE  CMPA    #0FBH      ;CHECK TO SEE IF IT IS READ OR WRITE
      BGE     NONDATA    ;IF NOT, THEN BRANCH AROUND
      TSX     ;TRANSFER STACK TO INDEX REGISTER
      ORAA    2,X        ;THE ADDRESS SHOULD BE SP+2
      JSR     SHIFTOUT   ;OUTPUT THE INSTRUCTION
      ANDA    #04H      ;CHECK TO SEE IF IT IS A READ OR WRITE
      BNE     RD         ;IF AC3J=1, IT IS A READ

WRT    LDAA    TEMP1      ;IF IT IS A WRITE, GET THE FIRST BYTE
      JSR     SHIFTOUT   ;WRITE THE FIRST BYTE
      LDAA    TEMP1+1    ;GET THE SECOND BYTE
      JSR     SHIFTOUT   ;WRITE THE SECOND BYTE
      BRA     DONE       ;WRITE INSTRUCTION COMPLETE

RD     JSR     SHIFTOUT   ;GET THE FIRST BYTE
      STAA    TEMP1      ;STORE IN TEMP1
      JSR     SHIFTOUT   ;GET THE SECOND BYTE
      STAA    TEMP1+1    ;STORE IN TEMP1+1
      BRA     DONE       ;READ COMPLETE

NONDATA JSR     SHIFTOUT  ;OUTPUT THE INSTRUCTION
DONE   CLRA
      STAA    FORT1      ;DESELECT THE X2444 BY MAKING CS 0
      RTS              ;RETURN FROM SUBROUTINE
;*****
; MAIN INSTRUCTION ROUTINES- COULD BE MACROS
;*****
; READ ROUTINE
; ASSUMES THAT THE ADDRESS IS IN THE A ACCUMULATOR, DATA IS LEFT IN X REGISTER
;*****
READ   ASLA                    ;SHIFT THE ADDRESS 3 TIMES TO LINE IT
      ASLA                    ;UP WITH THE INSTRUCTION FIELD
      ASLA
      PSHA                    ;PUSH ADDRESS ON THE STACK
      LDAA    #0B7H          ;LOAD INSTRUCTION INTO A ACCUMULATOR
      JSR     DRIVE          ;PERFORM INSTRUCTION
      LDY     TEMP1          ;GET THE RESULT IN THE INDEX REGISTER
      PULA                    ;CLEAN UP THE STACK
      RTS                    ;AND RETURN
;*****
; WRITE ROUTINE
; ASSUMES THAT THE ADDRESS IS IN THE A ACCUMULATOR, DATA TO WRITE IS IN THE
; X REGISTER.
; ALSO CALLS SET WRITE ENABLE LATCH ROUTINE(SWREN) TO ENABLE THE WRITE OPERATION
;*****
WRITE  ASLA                    ;SHIFT THE ADDRESS 3 TIMES
      ASLA
      ASLA
      PSHA                    ;PUSH ADDRESS ONTO THE STACK
      JSR     SWREN          ;SET THE WRITE ENABLE LATCH
      LDAA    #0B3H          ;LOAD WRITE INSTRUCTION
      STX     TEMP1          ;STORE DATA IN TEMP1
      JSR     DRIVE          ;PERFORM INSTRUCTION
      PULA                    ;CLEAN UP STACK
      RTS
;*****
RWREN  LDAA    #0FBH          ;LOAD THE INSTRUCTION
      JSR     DRIVE          ;AND EXECUTE
      RTS
;*****
STORE  LDAA    #0F9H          ;LOAD THE INSTRUCTION
      JSR     DRIVE          ;PERFORM OPERATION
      RTS                    ;AND RETURN
;*****
SLEEP  LDAA    #0FAH          ;LOAD THE INSTRUCTION

```

0006-4

## USING DATA POLLING IN AN INTERRUPT DRIVEN ENVIRONMENT

By Rick Orlando

The use of interrupt driven system design has become increasingly popular in many applications. Interrupt driven systems usually can achieve higher performance and improved user friendliness. An interrupt driven system can perform a variety of tasks while waiting for a certain condition to occur, rather than constantly looping and waiting for the occurrence. Writing to E<sup>2</sup>PROMs is no exception. Since the devices take a relatively long period to complete a Write Cycle, the system could perform a variety of tasks in the meantime.

DATA Polling was introduced on the X2864A to allow notification to the processor of Write Cycle completion. The manner in which it works is quite simple. The processor first writes a byte of data into the E<sup>2</sup>PROM. Any subsequent reads to any location of the chip will produce the complement of the data last written (hence, the name DATA Polling) until the E<sup>2</sup>PROM's internal Write Cycle is complete. At this point, reads to any location in the E<sup>2</sup>PROM will result in the valid data at that location. It can be seen that one can simply write a byte, and then perform frequent compares of the data in the location just written. The data will not be correct until the chip has completed its internal Write Cycle, and the Data circuitry is disabled.

In applications where the processor does not have anything to do during the Write Cycle, the software can simply perform compare loops until the Write Cycle is complete, and then write the next byte. In applications which are more processing time limited, a test loop can be placed in the main program loop, which will check the status of a previous Write Cycle on each pass through the main or outermost software loop. Almost all microprocessor applications software has such a top level loop. DATA Polling is obviously adequate in these environments.

The interrupt intensive applications may not have a main control loop nor can they usually afford the processing time for the processor to sit and loop until the Write Cycle is complete. In these applications, it would be ideal if the Write Cycle completion notification could be interrupt controlled. Although it is not obvious, DATA Polling can be used in these applications as well.

It should be noted that the whole reason for Write Cycle notification is because the typical write times for the E<sup>2</sup>PROMs are substantially shorter than the specified maximums. The magnitude of the delta between the typical and the maximum values determines the importance of the Write Cycle notification. One can easily see that if the maximum Write Cycle time and the typical were equal, one would only have to time a fixed interval for each Write Cycle, either from a software loop or a hardware timer. The hardware timer would generate an interrupt 10 msec after the Write Cycle was initiated, and the next byte could be written. Keep in mind that the discussion of write times for E<sup>2</sup>PROMs are in terms of msec rather than the  $\mu$ sec in which the processor executes instructions. A few  $\mu$ secs here or there are not important when compared to the Write Cycle time of about 10 msec.

DATA Polling does not require any additional hardware interface in order to be used. It is an exclusively software oriented method for determining Write Cycle completion. Even in an interrupt environment, no additional circuitry is required, since all of the interface to the chip occurs through the data and address bus.



In order to use DATA Polling in an interrupt driven system, one only needs a time-based interrupt generator. This could be a programmable timer or even something as simple as an AC frequency interrupt. The key is that the processor does not check to see if the device has completed the Write Cycle until the interrupt occurs. The interrupt routine simply compares the data last written to the E<sup>2</sup>PROM to the data coming from the E<sup>2</sup>PROM. If the two match, the device can be written again. If not, the processor simply returns from the interrupt routine to where it was and continues processing until the next interrupt. The interrupt source is maskable which prevents the overhead of servicing the periodic interrupt during the intervals when a write has not been performed.

A programmable timer or counter is the most elegant solution. Figure 1 shows the hardware configuration of a typical system with the E<sup>2</sup>PROM and the programmable timer on the bus. It should be noted that no unusual circuitry is needed from the E<sup>2</sup>PROM socket, which preserves its usefulness as a truly universal socket. The timer interrupt output drives one of the processor's interrupt lines. Many systems already have such a timer on the bus, and as a result require no additional hardware changes to implement this method.

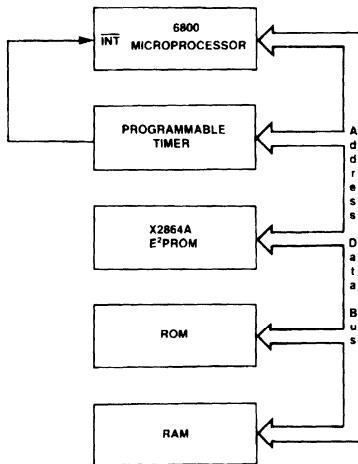


Figure 1: Hardware Configuration of a Typical System with the E<sup>2</sup>PROM and the Programmable Timer on the Bus

The software implementation is rather simple. Figure 2 shows an example of how it might be done using a 6800 microprocessor and a simple timer. The timer control and data registers are mapped into the memory locations described in the initial header along with the temporary RAM variables, which are used to store the last data written and its address.

The write routine (WEEPROM) initially checks to see if the E<sup>2</sup>PROM is ready to perform a write. If not, it simply exits with an error code to show that the write has not taken place. If the write is performed, the timer is loaded with the initial count for 4 msec, and the timer interrupt is enabled. The processor then goes off and performs its normal duties until the interrupt takes place. At that point, the interrupt routine (CKEEP) is entered. It first checks for the proper data that was written to see if the write is complete, using DATA Polling. If it is, the ready flag is set, and the routine is exited. If not, the counter is loaded with a smaller increment, such as 500  $\mu$ sec until the chip's Write Cycle is completed. This essentially allows the majority of the Write time to pass (4 msec) before the processor checks at the more frequent interval of every 500  $\mu$ sec.

Five hundred  $\mu$ sec has been chosen in this example for the interrupt granularity. The value used for a particular application should be chosen based upon the actual system requirements.

One can see that this implementation is rather easy and can be performed with hardware that already may exist in the system. By using the periodic interface approach, the system has the advantage of using an interrupt driven write algorithm, while maintaining only a software interface to the E<sup>2</sup>PROM. Most of the "bookkeeping" sections of the example code are the same as one would use with any method of write termination notification. The end result of using DATA Polling in an interrupt environment is optimization of the Write Cycle period as well as preservation of the pinout of the universal 28-pin socket for expansion through the 256K bit level for E<sup>2</sup>PROMs.

PAGE - 1 DATA\_COD  
File: :DATA.CODE.TEXT

# CODE FOR DATA POLLING IN INTERRUPT ENVIRONMENT, 6800 VERSION

```

0000:                                     .PROC DATA.CODE
Current memory available: 4380
0000: ;*****
0000: ; SAMPLE CODE FOR USING DATA POLLING IN INTERRUPT ENVIRONMENT
0000: ; THIS CODE SHOWS AN EXAMPLE OF HOW TO USE DATA POLLING IN A
0000: ; INTERRUPT DRIVEN WRITE MODE
0000: ;*****
0000: ; MEMORY LOCATIONS
0000: 0100: TIMER .EQU 0100H ;LOCATION OF TIMER DATA REGISTER(COUNT DOWN VALUE)
0000: 0102: CTIMER .EQU 0102H ;TIMER CONTROL REGISTER
0000: 0103: LASTA .EQU 0103H ;RAM LOCATION FOR LAST WRITTEN DATA
0000: 0104: TEMP .EQU 0104H ;RAM LOCATION FOR LAST ADDRESS WRITTEN
0000: 0106: ERROR .EQU 0106H ;ERROR FLAG FOR WRITE
0000: 0107: READY .EQU 0107H ;MEMORY READY FOR NEXT WRITE FLAG
0000: 0108: CONFIG .EQU 0108H ;TIMER CONFIGURATION BYTE
0000:
0000: .ORG 0F000H
0000: ;*****
0000: ; EEPFROM WRITE ROUTINE
0000: ; THIS ROUTINE WRITES A BYTE OF DATA PASSED IN THE A ACCUMULATOR INTO
0000: ; THE EEPFROM AT LOCATION POINTED TO BY THE VALUE IN THE X INDEX REGISTER.
0000: ; THE ROUTINE THEN INITIALIZES THE DATA IN THE COUNTER TO 4096, SINCE THE TIMER
0000: ; COUNTS AT A 1 MHZ FREQUENCY. THIS WILL TIME OUT THE INITIAL 4 MSEC OF THE WRI
0000: ; WRITE CYCLE. THE ROUTINE THEN ENABLES THE INTERRUPTS AND RETURNS CONTROL TO
0000: ; THE CALLING ROUTINE
0000: ;*****
0000: WEEPFROM LDA# 000H ;COMPARE TO SEE IF THE MEMORY IS READY FOR WRITE
0002: F1 0107 CMP# READY ;CHECK MEMORY LOCATION READY
0005: 27 ** BEQ WRITE ;IF READY THEN WRITE
0007: C6 00 LDA# 000H ;OTHERWISE SET THE ERROR FLAG
0009: F7 0106 STAB ERROR ;AND STORE IT IN ERROR
000C: 20 ** BRA EXIT ;AND EXIT
000E: A7 00 WRITE STAA 0XX ;WRITE THE DATA IN A TO LOCATION X
0010: B7 0103 STAA LASTA ;STORE DATA IN RAM AT LASTA
0013: F1 0104 STX TEMP ;AND STORE LOCATION IN EEPFROM AT TEMP
0016: C6 10 LDA# 10H ;LOAD THE FIRST BYTE OF 4096 HEX INTO B ACCUMULATOR
0018: F2 0100 STAB TIMER ;WRITE TO TIMER DATA REGISTER
001B: C6 00 LDA# 000H ;LOAD THE SECOND BYTE OF 4096 HEX
001D: F7 0101 STAB TIMER+1 ;STORE IN THE LSB OF TIMER REGISTER
0020: F6 0108 LDA# CONFIG ;GET THE TIMER INITIALIZATION CODE
0023: F7 0102 STAB CTIMER ;STORE IT IN THE TIMER CONTROL REGISTER
0026: 0E CLI ;CLEAR INTERRUPT MASK TO LET TIMER INTERRUPT
0027: 39 EXIT RTS ;RETURN FROM SUBROUTINE
0028: ;*****
0028: ; CHECK EEPFROM ROUTINE
0028: ; THIS ROUTINE CHECKS TO SEE IF THE EEPFROM IS DONE. IT IS ENTERED
0028: ; EVERY TIME THAT THE INTERRUPT IS GENERATED FROM THE TIMER. IT COMPARES
0028: ; THE DATA AT LOCATION TEMP IN THE EEPFROM WITH THE DATA THAT IS STORED IN
0028: ; LASTA LOCATION IN RAM. IF THE COMPARISON FAILS, THEN THE EEPFROM IS NOT
0028: ; DONE YET, ANDN THE TIMER IS RESET TO TIME 1/2 MSEC(OR 512 USEC). THE
0028: ; ROUTINE IS THEN EXITED.
0028: ;*****
0028: CKEE# LDA# LASTA ;GET THE LAST DATA WRITTEN
002B: F6 0103 LDX TEMP ;GET THE ADDRESS FOR THE BYTE IN EEPFROM
002E: FE 0104 CMP# 0XX ;COMPARE TO SEE IF THE WRITE IS COMPLETE
002E: A1 00

```

PAGE - 2 DATA\_COD  
File: :DATA.CODE.TEXT

# CODE FOR DATA POLLING IN INTERRUPT ENVIRONMENT, 6800 VERSION

```

F030: 26 ** BNE REINIT ;IF NOT EQUAL REINITIALIZE THE TIMER
F032: B6 00 LDA# 000 ;SET THE READY FLAG
F034: E7 0107 STAA READY ;AND STORE IT IN READY
F037: 20 ** BRA RET ;AND RETURN FROM SUBROUTINE
F039: B6 02 REINIT LDA# 002H ;LOAD THE FIRST BYTE FOR COUNTER
F03B: E7 0100 STAA TIMER ;WRITE TO TIMER DATA REGISTER
F03E: B6 00 LDA# 000H ;LOAD THE SECOND BYTE
F040: E7 0101 STAA TIMER+1 ;WRITE TO LSB OF TIMER DATA REGISTER
F043: 9B RET RTS ;RETURN FROM INTERRUPT
F044: ;*****
F044: .END

```

## SYMBOLTABLE DUMP CODE FOR DATA POLLING IN INTERRUPT ENVIRONMENT, 6800 VERSION

AB - Absolute	LB - Label	UD - Undefined	MC - Macro
RF - Ref	DF - Def	FR - Proc	FC - Func
PB - Public	PV - Private	CS - Consts	RS - Residents

CKEEP	LB F02B:	CONFIG	AB 0108:	CTIMER
LASTA	AB 0103:	READY	AB 0107:	REINIT
WEEPFROM	LB F000:	WRITE	LB F00E:	

AB 0102:	DATA_COD	FR ----:	ERROR	AB 0106:	EXIT	LB F027
LB F039:	RET	LB F043:	TEMP	AB 0104:	TIMER	AB 0100

Figure 2: Software Implementation for 6800 Microprocessor and a Simple Timer

## NOTES



# Application Brief

## E<sup>2</sup>PROM PROVIDES THE SOLUTION TO FIELD ALTERABLE SOFTWARE

By Rick Orlando

The advent of the 5-volt E<sup>2</sup>PROM has brought about many changes in the manner in which the designer views his software. Such devices allow for in-field reprogrammability, which greatly reduces the cost and impact of software changes or upgrades. The 5 volt E<sup>2</sup>PROM allows the designer the capability to completely upgrade or change his software from a remote location rather than through the replacement of the system ROMs or EPROMs, a costly and inconvenient method at best. Complete in-field programmability requires that the entire program store of the system be implemented in E<sup>2</sup>PROM. An alternative is a "hybrid" system.

A "hybrid" approach refers to a design which utilizes both EPROMs or ROMs in conjunction with E<sup>2</sup>PROMs to yield a design which features the best of both approaches: the low cost of a full ROM implementation, while maintaining the flexibility of a full E<sup>2</sup>PROM approach.

The secret to this approach is to analyze the software requirements of the end system from two distinct levels. That of the machine code routines which perform the simple tasks, and that of the higher level routines which call the lower level routines to perform an algorithm. The order in which the low level routines are called is determined by the higher level routines or program flow. This "Top-Down" programming approach is more efficient and structured, and is the basis for many high level languages. The fact that it can be used in machine language coding should not come as a surprise to designers, since the decomposition of a complex task into many simple tasks is quickly learned in programming, even if it is not called "structured programming" per se. The decomposition of the end task can sometimes lead to many different levels of program structure, but for the simplicity of discussion, this brief will limit itself to the most simple approach, that of two level program structure.

The lower level code consists of the machine

dependent routines such as that required to fetch a character from an I/O link. The buffering of multiple characters from this link might also be a low level routine. The interpretation of the buffered character string will be implemented in the higher level code, since it simply calls the lower level routines and determines the action to take based upon their results.

A basic example is that of the executing of multiple character command entered by the operator from a keyboard. The lowest level routine simply gets a character from the keyboard if a key is depressed. The next level of the software "buffers" the input to make the system more "user-friendly". This routine looks at the input string, eliminates misplaced blanks or other characters, and forms a character string which the high level program can understand. As a result, the "parsing" task is broken into three distinct levels.

The first involves the inputting of a single character from the keyboard into a character buffer. The second level continually calls the first routine until an end-of-input character is detected (such as a Carriage Return). The top most level of the code takes the parsed command and determines if it is a valid command by searching a table of valid commands. If the command is valid, the address of the routine to execute is fetched out of the table, and the processor performs a jump. Most of the input processing is handled at the lowest level, thereby reducing the overhead in the outermost routine.

As more and more of the processing tasks are pushed "down" into low level routines, the main procedure in the high-level segment becomes very short and simple. In fact, it can be reduced to a simple list of jump-to-subroutine instructions. This structured approach not only eases the software development task, but it also minimizes the debugging time required for the software since it is built upon other routines which have already been debugged.

If one completely decomposes the task to be performed by a particular segment of the systems main program, it becomes a list of procedure calls to lower level segments. This method lends itself very well to a system which can use E<sup>2</sup>PROM. Since the "outermost" program store is quite compact, it can be implemented in E<sup>2</sup>PROM while the majority of the machine code in the lower levels can be implemented in ROM or EPROM. Changes to the software then become as simple as changing the jump location in the E<sup>2</sup>PROM, and the order of execution of the lower level routines can be altered in such a manner.

Using this method, one can also reserve a section of the E<sup>2</sup>PROM for low-level "patch" alterations to the software. If a low level routine is found to be in error or needs updating, the new version of the machine code is loaded into the reserved section of the E<sup>2</sup>PROM. The jump instructions in the high level code in the E<sup>2</sup>PROM are simply changed to "jumps" to the new routine now residing in the E<sup>2</sup>PROM as opposed to the old routine in the ROM or EPROM. Figure 1 shows a typical memory map where the E<sup>2</sup>PROM is used to store the high-level routines which perform a variety of jump to subroutines to control the program flow. The low level machine language routines are stored in the EPROM as shown. Figure 2 shows how a patch is made to

replace the old routine in EPROM called "PARSE" with a new version loaded into the E<sup>2</sup>PROM. The jump-to-subroutine addresses in the E<sup>2</sup>PROM are updated to point to the new routine in E<sup>2</sup>PROM. The actual update or "patch" can be performed remotely, thereby eliminating the need for in field EPROM replacements for both the remedying of software bugs as well as the upgrading of systems in the field to take advantage of new features or capabilities.

Since both the valid character and the valid command tables reside in the E<sup>2</sup>PROM, new entries can be made to allow for additional command selection. New command character strings are simply added to the valid command list. The low-level code for the new command can either be loaded into the E<sup>2</sup>PROM patch area or utilize routines which already exist in the ROM or EPROM. The appropriate address is appended to the new command string.

If an error is discovered in an existing command, the valid command list is updated to point to the new command routine which is loaded into the patch area of the E<sup>2</sup>PROM. Figure 3 depicts the memory map after such a change has been made.

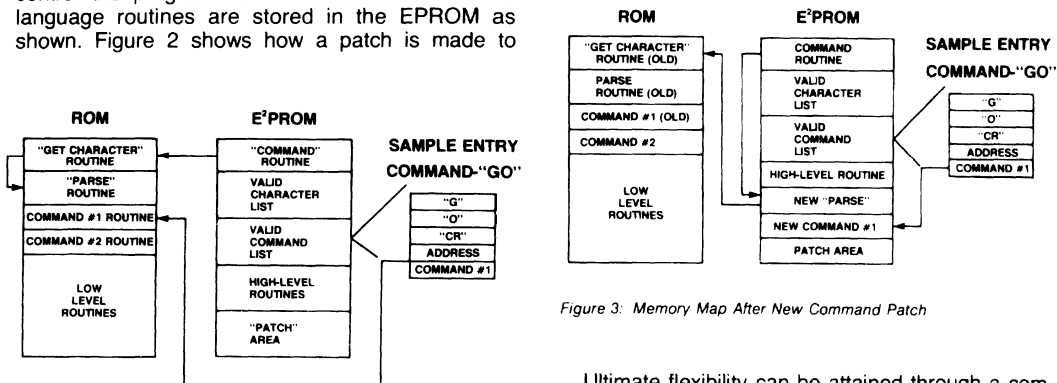


Figure 1: Memory Map Original Configuration

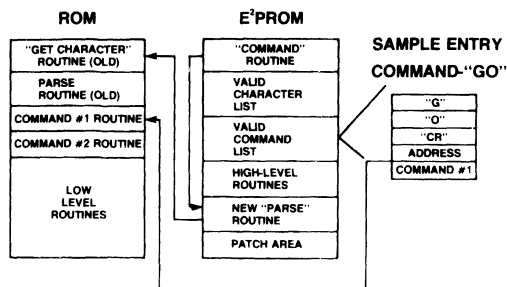


Figure 2: Memory Map After Routine Patch

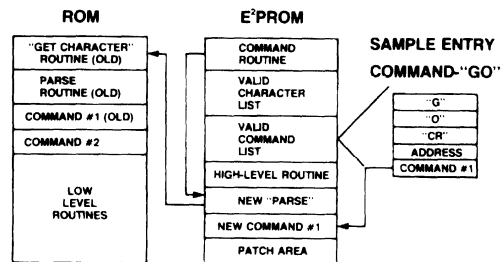


Figure 3: Memory Map After New Command Patch

Ultimate flexibility can be attained through a complete E<sup>2</sup>PROM design. It can also be shown that a minimal amount of E<sup>2</sup>PROM can add great flexibility to the system not only in terms of software alteration, but also in its intrinsic ability to store user alterable parameters such as configuration data. The actual ratio of EPROM to E<sup>2</sup>PROM must be determined based upon the systems' requirements. The advantage of the "hybrid" approach is that it requires that only the "top level" portion of the code be resident in E<sup>2</sup>PROM, and as such is usually limited to a series of procedure calls, which are very code efficient.

In the cases where the software is to be updated remotely, perhaps through the use of a modem, certain factors must be considered. The key point is that while the processor is executing programs in the E<sup>2</sup>PROM, it is inadvisable to write into that particular device. The reason for this is that while the device is performing the write cycle, any reads, such as an opcode fetch, will result in a high impedance bus.

The important issue is that the download of the new code must not reside in the E<sup>2</sup>PROM to be modified.

This can be accomplished in two different ways. The first implements the download program segment in the low level ROM or EPROM. In this case, the actual instructions will be present from the memory throughout the download sequence. Figure 4 shows such an approach where the download software is kept in the ROM. This routine writes the new bytes into the E<sup>2</sup>PROM and then enters a software loop to time out the E<sup>2</sup>PROM write cycle.

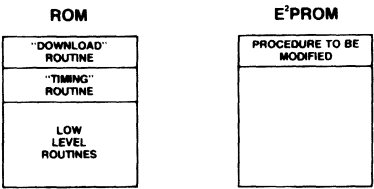


Figure 4: Memory Map-Download and Timing Resident in ROM

In some applications, this method may not be adequate, especially if the actual download routine is to be modified. In these cases, this program segment must be stored in the E<sup>2</sup>PROM, and hence, cannot be directly executed from the E<sup>2</sup>PROM to be modified. In this situation, a possible approach is to copy the download program segment from the E<sup>2</sup>PROM into RAM. The program then jumps to the RAM location, where the copy of the old code resides. This RAM routine loads the new program segment into the proper E<sup>2</sup>PROM locations, timing out the necessary E<sup>2</sup>PROM write cycle. Once the download is complete, the program executing out of the RAM then jumps back to the main program, and the download routine section of the E<sup>2</sup>PROM will contain the new code. Figure 5 shows the various stages of this operation in terms of the contents of the various memories and the program execution flow.

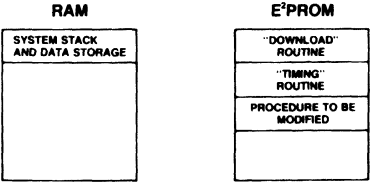


Figure 5a: Memory Map Prior to Download

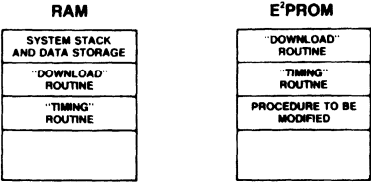


Figure 5b: Memory Map Download Routine Transferred to RAM

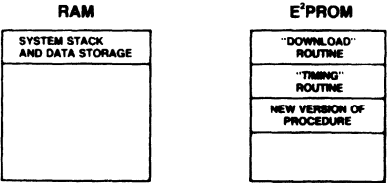


Figure 5c: Memory Map RAM Erased After Transfer Complete

As one can see, the "hybrid" approach to software design, utilizing a combination of both E<sup>2</sup>PROMs and ROMs or EPROMs, can result in a system which exhibits the advantages of the field alterability of E<sup>2</sup>PROMs. As the cost of the development and maintenance of the system software becomes more dominant in the overall cost of the system, such methods as those presented in this brief will become more commonplace in system design.

## NOTES



# Application Brief

## “ $t_{DV}$ ”—WHAT IS IT?

By Richard Palm

E<sup>2</sup>PROMs, RAMs and EPROMs all being memory devices have similar specifications. However, one of the specifications unique to E<sup>2</sup>PROMs is  $t_{DV}$  (Data Valid Time).

The E<sup>2</sup>PROM requires a relatively lengthy period of time to tunnel charge onto or off of the floating gate to complete the write cycle. This time is specified as  $t_{WC}$ . In order to more closely emulate RAM write timing, Xicor introduced “self timed” write operations. Xicor E<sup>2</sup>PROMs latch the address on the falling edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever occurs last, and latch data on the rising edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever occurs first. The falling edge of the write operation not only latches the address of the byte (or page) to be written but also starts a number of internal timers that control the programming cycle.

In page mode, subsequent  $\overline{WE}/\overline{CE}$  falling edges will restart the timers. But it is these timers that require specifying  $t_{DV}$ .

In most microprocessor based systems,  $t_{DV}$  can be ignored because  $t_{WP}$  will be less than  $t_{DV}$ . However, in applications employing slower microprocessors and microcontrollers  $t_{WP}$  might be quite long. The actual internal programming cycle could begin before either  $\overline{CE}$  or  $\overline{WE}$  returned high, thereby missing valid data even though  $t_{DS}$  was met.

Once the internal timers initiate the programming cycle, the I/Os will be disabled. Therefore, valid data must be present on the bus before the I/Os are disabled. As an example, refer to Figure 1 illustrating the sequence of events.

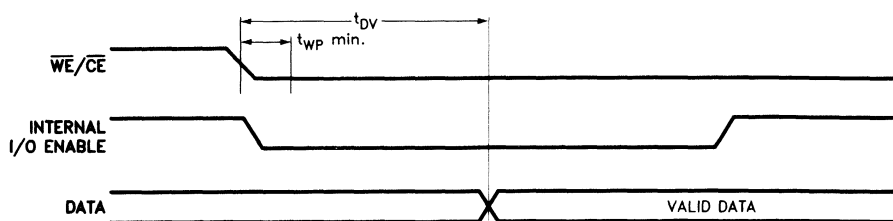


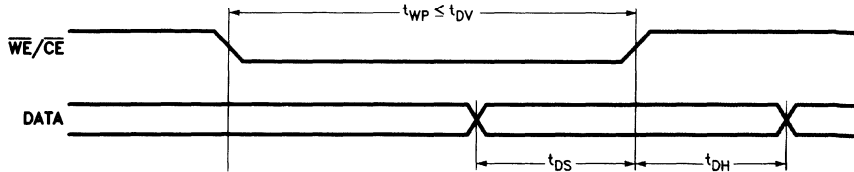
Figure 1: External/Internal Timing

0060-1



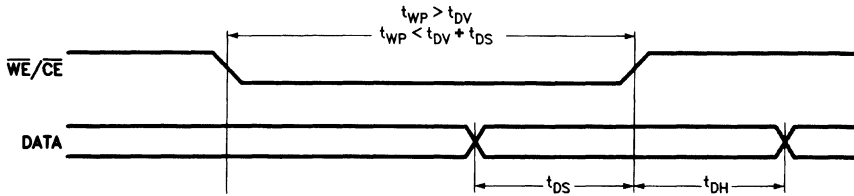
$t_{DV}$  is the maximum time to elapse from the falling edge of  $\overline{WE}$  or  $\overline{CE}$  (whichever occurs first) before valid data have to be presented to the E<sup>2</sup>PROM.

How does this impact your design? The following timing diagrams cover the three possibilities. Notice that in all the examples  $t_{DH}$  must still be met.



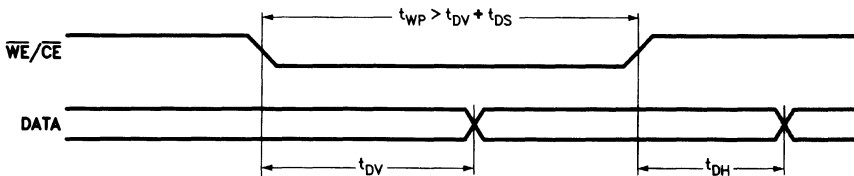
Example 1: If  $t_{WP}$  is equal to or greater than  $t_{WP}$  min but less than  $t_{DV}$ , then  $t_{DS}$  and  $t_{DH}$  must be met.

0060-2



Example 2: If  $t_{WP}$  is greater than  $t_{DV}$  but less than  $t_{DV}$  plus  $t_{DS}$ , then  $t_{DS}$  and  $t_{DH}$  must be met.

0060-3



Example 3: If  $t_{WP}$  is greater than  $t_{DV}$  plus  $t_{DS}$ , then  $t_{DV}$  and  $t_{DH}$  must be met.

0060-4

In summary, the data must be valid on the bus for the worst case timing parameters; whether that is  $t_{DV}$  or  $t_{DS}$  and always valid for  $t_{DH}$ .

## Glossary

$t_{DV}$	Data Valid Time
$t_{WC}$	Write Cycle Time
$t_{DS}$	Data Setup
$t_{WP}$	$\overline{WE}$ Pulse Width
$t_{DH}$	Data Hold



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# Understand your application in choosing NOVRAM, EEPROM

Richard Orlando, Xicor Inc., Milpitas, CA

*As appeared in EDN Magazine*

*May 12, 1983*

# Understand your application in choosing NOVRAM, EEPROM

*Examining how NOVRAMs and EEPROMs serve various applications illustrates the memory devices' capabilities and simplifies device selection.*

**Richard Orlando**, Xicor Inc

If your system design calls for electrically erasable nonvolatile data storage, you can simplify the selection of semiconductor memory for that task by choosing from among four basic types—NOVRAM, EEPROM, EAROM and battery-backed CMOS RAM. Assuming that you've examined the system-level tradeoffs among these memory types (EDN, April 14, pg 135) and have narrowed your choice to the first two, use the information presented here to understand the detailed tradeoffs and design considerations underlying NOVRAM and EEPROM use. In some application classes, either memory type functions adequately; in others, you have a clearcut choice. And in still others, consider taking advantage of both—an approach that often results in cost reductions and enhanced features.

## **NOVRAMs use multiple technologies**

First, however, understand how each memory type works. Nonvolatile static RAM (NOVRAM) combines two memory technologies on one monolithic chip. In **Fig 1**, the NOVRAM shown contains 1k bits of static RAM and 1k bits of electrically erasable PROM (EEPROM). The device comprises cells that in turn each contain one cell of each memory type, rather than housing two separate memory arrays (see box, "Anatomy of a NOVRAM cell").

In this NOVRAM, data gets read and written exactly as in a standard static RAM. In addition, the Store signal transfers each RAM cell's data into a shadowing EEPROM cell; EEPROM-stored data gets reloaded into the RAM via the Recall signal. Note that the EEPROM-cell portion is accessible only through the RAM portion.

One of this device type's most powerful features is its ability to transfer the entire RAM contents into

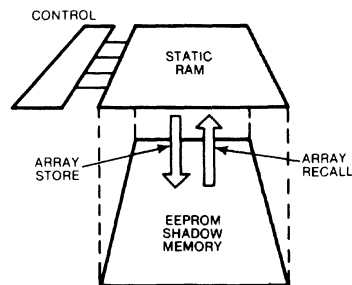
nonvolatile storage in one operation, initiated by bringing the TTL-compatible Store LOW. The operation takes less than 10 msec, and once data is stored in this manner, only another store operation can alter it—even if the chip loses power.

Generating Store in the event of a power failure therefore saves the RAM contents, subject only to power remaining on the chip for the next 10 msec. RAM data can also be changed without disturbing the shadowing EEPROM, allowing the system to manipulate two separate groups of data.

## **EEPROMs offer greater density, fewer features**

EEPROM, your other major memory choice, resembles UV-erasable EPROM. Unlike EPROM, however, it can be written electrically in circuit; it needs no prior erasure by exposure to ultraviolet radiation.

First-generation EEPROMs are merely electrically



**Fig 1—Nonvolatile static RAM (NOVRAM) is organized so that each static-RAM bit is overlaid on a bit of nonvolatile electrically erasable PROM (EEPROM).**

Careful analysis simplifies the EEPROM vs NOVRAM choice

alterable ROMs (EAROMs). They're reprogrammable only after an entire memory array (or at least one page) is electrically erased. Similarly, second-generation devices require erasure of individual bytes before programming. Third-generation EEPROMs, however, automatically and internally erase a to-be-written byte as part of the write cycle; they also contain much of the required voltage-generating and pulse-shaping functions on chip.

Two examples of third-generation EEPROMs currently in production are the Intel 2817 and the Seeq 5213. The 2817 latches the data to be written and eliminates the need for prewrite erasure. However, it requires an external high-voltage supply as well as a timing capacitor for deriving internal timing signals.

TABLE 1—EEPROM/NOVRAM COMPARISONS

	NOVRAM (X2212)	EEPROM (X2816A)
Density (bits)	1024	16,384
Price (1k level)	\$9.00	\$23.00
Cost/bit	\$0.0088	\$0.0014

The 5213 generates the high voltage on chip but requires external latches that hold the data and address valid during erase and write operations.

Fourth-generation EEPROMs are characterized by

Anatomy of a NOVRAM cell

NOVRAM-cell operation depends on a phenomenon termed Fowler-Nordheim tunneling. In the NOVRAM, a layer of oxide isolates a gate from an underlying section of polysilicon. Applying a large positive voltage to this floating gate while holding the underlying polysilicon near ground programs the gate.

Specifically, electrons attracted to the floating gate's significantly higher potential tunnel across the separating oxide. As a result, the floating gate acquires a net negative charge from the tunneled electrons.

The cell is erased in a similar manner: The floating gate is held at a low potential while the potential of the top polysilicon layer is raised; the electrons then tunnel across the oxide from the floating gate to the neighboring polysilicon sandwich.

The EEPROM technology employed in Xicor's NOVRAM uses a 3-layer polysilicon sandwich that, when coupled with a 6-transistor static-RAM cell, results in the NOVRAM circuit shown in Fig A. The state of the static-RAM cell determines whether the EEPROM

cell is programmed or erased during a store cycle.

Capacitance ratios are the key to the data transfer from RAM to EEPROM. If node N<sub>1</sub> is LOW, Q<sub>7</sub> is turned off, allowing the junction between capacitors C<sub>3</sub> and C<sub>4</sub> to

float. Because the combined capacitance of C<sub>3</sub> and C<sub>4</sub> is larger than C<sub>p</sub>, the floating gate follows the Store-node voltage. When the voltage on the floating gate is sufficiently high, electrons tunnel from POLY<sub>1</sub> to POLY<sub>2</sub>, and the

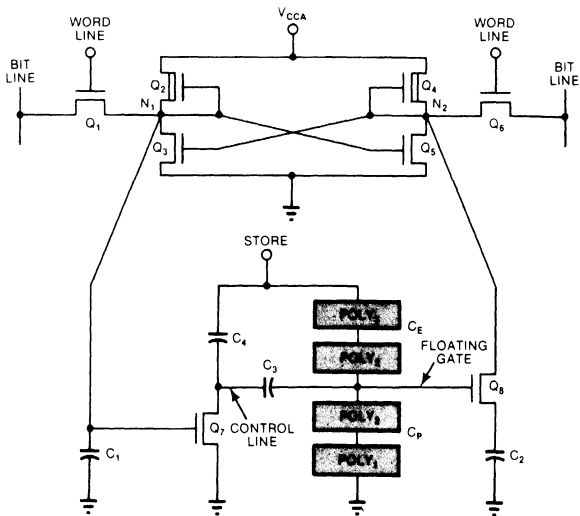


Fig A—A NOVRAM cell consists of two sections: a 6-transistor RAM and a shadowing 2-transistor EEPROM.

on-chip generation of all high-voltage and wave-shaping functions in addition to their use of on-chip latches and self-timing features. Their byte-write requirements are identical to those of static RAM except that the EEPROM write cycle, once initiated by normal static-RAM timings, takes as long as 10 msec. Once a byte-write operation begins, the EEPROM is self supporting, freeing the processor and all external circuitry for other tasks. Read timing to the EEPROM is identical to that of a standard EPROM, RAM or ROM.

An important feature of a fourth-generation EEPROM is its compatibility with currently used RAM, EPROM and ROM. An EPROM- or ROM-based system needs only an additional Write Enable line to

each socket to provide retrofitting for EEPROM. This control line allows the changing of data tables and program store without removing the component from the system, as required with EPROMs.

### Choosing between NOVRAM and EEPROMs

Many application requirements can be satisfied by either of the two memory types. However, note that although NOVRAM is the most versatile in terms of features and capabilities, the price you pay for its greater intelligence is increased cell size.

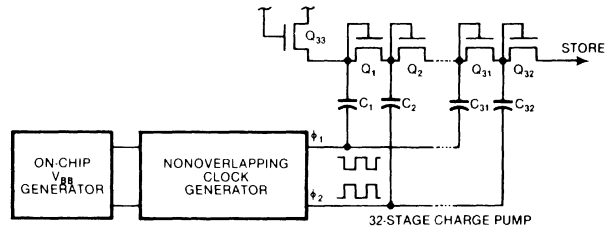
Specifically, a fourth-generation EEPROM's cell is small and simple, allowing much higher density storage than in a NOVRAM. The EEPROM is also more efficient as memory-array area increases, thanks to the

gate becomes negatively charged.

If node  $N_1$  is HIGH,  $Q_7$  turns on, grounding the junction between  $C_3$  and  $C_4$ .  $C_3$ , larger than  $C_6$ , holds the floating gate near ground when the Store node gets pulled HIGH. This action creates a sufficiently large field between  $POLY_2$  and  $POLY_3$  to tunnel electrons away from the floating gate, leaving it with a positive charge.

The recall operation also depends on capacitance ratios.  $C_2$  is larger than  $C_1$ . When the cell receives the external Recall command, the internal power supply ( $V_{CCA}$ ) first goes LOW to equalize the voltages on  $N_1$  and  $N_2$ . When  $V_{CCA}$  is allowed to rise, the node with the lighter capacitive load rises more rapidly. The flip flop's gain causes the lightly loaded node to latch HIGH and the opposite side to latch LOW. If the floating gate has a positive charge,  $C_2$  is connected to  $N_2$  through  $Q_8$ , and  $N_2$  latches LOW. If the floating gate has a negative charge,  $Q_8$  gets turned off and  $N_1$  experiences the heavier loading.

A major task in the development of the NOVRAM was to reduce the



**Fig B—A 32-stage charge pump** internally generates a NOVRAM's high Store voltage, allowing the device's NOVRAM and EEPROM sections to operate from 5V.

amplitude and simplify the waveform of external voltages needed for programming or erasure. Earlier devices required carefully shaped pulses with amplitudes exceeding 20V.

The first step in the cell design was to reduce the internal voltage level presented to the cell to initiate electron tunneling. The voltage magnitude required for programming a floating gate is related to the intensity of the electric field generated at the oxide-polysilicon interface by that voltage.

Electric-field strength at the oxide-polysilicon interface can be

increased by using an extremely thin oxide, on the order of 100Å. A second technique uses textured polysilicon to locally enhance the field at the surface and achieve Fowler-Nordheim tunneling. It achieves better data retention.

Once the internal voltage-level requirement was reduced, a key achievement in device design was the on-chip generation of the high-voltage pulses needed to program or erase an individual cell. A Store-voltage generator (**Fig B**) provides the solution; it uses a 32-stage capacitor/transistor charge pump.

# Each NOVRAM cell combines RAM and EEPROM

TABLE 2—EEPROM/NOVRAM  
DATA-CAPTURE SPEEDS

	NOVRAM (X2212)	EEPROM (X2816A)
Byte-Write Time	256 × 1 μsec	256 × 10 msec
Store Time	10 msec	0
Total Time	10.26 msec	2.56 sec

decrease in the relative proportion of support-circuitry area required. Therefore, EEPROMs are more likely to be the device of choice if your application needs large amounts of memory.

The larger cell size and more extensive on-chip support that gives NOVRAM its added capabilities also results in a higher cost per bit, which might not be justified in applications that don't require all of a NOVRAM's features. Consider, for example, the cost-per-bit comparison between the X2212 256×4-bit NOVRAM and the X2816A 2k×8-bit EEPROM (Table 1): NOVRAM cost per bit is more than six times greater than that of EEPROM.

However, cost-per-bit ratios can be deceiving for systems requiring a minimum amount of nonvolatile memory. Lower density nonvolatile memories often are more cost effective in a NOVRAM configuration. The smallest NOVRAM currently available, the 64×4 X2210, is also the least expensive 5V device.

Another selection factor to consider is the required write time. An EEPROM requires a relatively long write time (10 msec/byte max), while NOVRAM write

time is that of a typical static RAM. Therefore, NOVRAMs are more suited for applications requiring frequent memory-data changes, while EEPROMs most suit applications calling for infrequent memory writes.

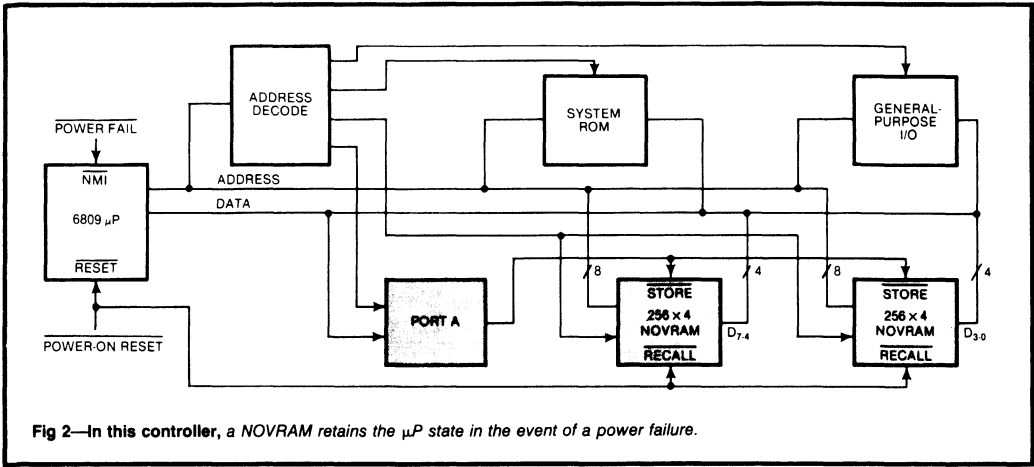
A NOVRAM is also better suited to data-capture applications. Table 2 compares two 256×4-bit NOVRAMs organized in a byte-wide configuration with a 2k×8 EEPROM in terms of the time needed to store 256 bytes of information. These times assume a 1-μsec/byte max processor write-cycle time. You can see that the NOVRAM's single-store operation makes it much faster. A NOVRAM system can update and store 10,000 bytes of data in the time needed to store two bytes of EEPROM information.

Another important NOVRAM feature is the device's ability to initiate and complete a nonvolatile store of data under external-signal control. This feature can be a key decision criterion in real-time applications such as power-fail re-entrant systems.

## Both types serve power-fail-tolerant controllers

As noted, however, many applications can profitably use either device type. One common application in this class centers on retaining important system information in the event of a power loss. In most systems, power failures require reinitialization of the entire system, necessitating the temporary loss of system operation. In real-time control applications, this loss of control can cause expensive and sometimes dangerous failures of the process or equipment being controlled.

Such an application's main requirement is therefore some type of nonvolatile storage upon power failure. A prime consideration in this type of environment is the storage of a fixed amount of data upon receipt of an



```

;*****
; AN EXAMPLE OF THE POWER-DOWN AND POWER-ON CODE FOR THE 6809 USING
; THE NOVRAM FOR PROCESSOR STATUS STORAGE.
;*****
; LOCATION DEFINITIONS
NOVRAMB3 .EQU 0000H
NOVRAMB1 .EQU NOVRAMB3 + 256.
; THE NOVRAM IS LOCATED AT THE BOTTOM OF THE 6809 MEMORY MAP
DIRTYV .EQU NOVRAMB1 ;TEST BYTE FOR POWER FAIL CONDITION
OLDSTK .EQU NOVRAMB1-6 ;STACK POINTER NONVOLATILE LOCATION
STACK .EQU NOVRAMB1-7 ;PROCESSOR STACK BEGINNING LOCATION
TEMP1 .EQU NOVRAMB1-1 ;IMPORTANT PROCESS PARAMETERS
TEMP2 .EQU NOVRAMB1-2
TEMP3 .EQU NOVRAMB1-3
PORTA .EQU 0000H ;LOCATION OF DATA REGISTER FOR PORT
.ORG 0000H
;*****
; POWER FAILURE ROUTINE
;*****
PFAIL STS OLDSTK ;WRITE CURRENT STACK POINTER INTO NOVRAM
; AT THIS POINT, THE POWER FAIL INTERRUPT HAS PUSHED ALL OF THE
; CURRENT VALUES OF THE PROCESSOR REGISTERS ONTO THE STACK. THE
; STACK POINTER POINTS TO THESE VALUES.
LDA #005H ;LOAD ACCUMULATOR WITH POWER FAIL FLAG
STA DIRTYV ;STORE FLAG IN NOVRAM
LDA #00. ;WRITING A 0 TO THE PORT GENERATES
STA PORTA ;A STORE SIGNAL TO THE NOVRAM
LOOP BRA LOOP ;BIT AND WAIT UNTIL POWER DISAPPEARS
;*****
; POWER-ON RESET ROUTINE
;*****
RESET LDA #00FFH ;SET ALL OUTPUTS TO A "1"
STA PORTA ;WRITE TO PORT TO KEEP STORE HIGH
LDA DIRTYV ;LOAD FLAG TO SEE IF POWER FAILED
CMPA #005H ;IT WILL BE A 005H IF IT DID
BNE INIT ;IF NOT DO NORMAL INITIALIZATION
LDA #000H ;CLEAR THE POWER FAILURE FLAG
STA DIRTYV ;IN THE NOVRAM
LDA #000H ;AND GIVE A STORE SIGNAL
STA PORTA ;TO STORE THE NEW FLAG
LDA #00FFH ;RESET PORT.
LDS OLDSTK ;LOAD OLD STACK VALUES
RTI ;RETURN FROM POWER FAIL INTERRUPT
INIT ;NORMAL INITIALIZATION CODE
;
;
;
;
;*****
.ORG 0000H
.MWORD PFAIL ;POWER FAILURE INTERRUPT VECTOR
.MWORD RESET ;POWER-ON RESET INTERRUPT VECTOR
.END

```

Fig 3—A power-failure-tolerant controller's 6809- $\mu$ P assembly-language routines handle both failure store and recovery. NOVRAM handles the stack and other temporary storage.

## NOVRAM doubles as bootstrap and global memory

external Power Fail signal. You can use an EEPROM for this purpose if the processor has sufficient time to recognize the power failure and respond by writing the data into memory. Otherwise, a NOVRAM is the device of choice because it captures data in one nonvolatile store operation.

**Fig 2** shows a simple controller that uses a NOVRAM to retain the state of a  $\mu\text{P}$  in the event of a power failure. The Power Fail signal generates a  $\mu\text{P}$  interrupt, and the NOVRAM stores the contents of all RAM including the  $\mu\text{P}$  stack.

Upon interrupt acknowledgement, the  $\mu\text{P}$  registers are pushed onto the stack as program control branches to the interrupt routine (**Fig 3**). The routine writes the current stack pointer and a test byte to the NOVRAM, signifying that a power failure has occurred, and then generates a Store signal. The power supply is designed to ensure that the  $V_C$  level remains above 4.5V for 10 msec after it generates the Power Fail signal.

Once power is restored, the Power-On Reset signal generates a Recall signal to the NOVRAM. The power-on routine in the  $\mu\text{P}$  checks the state of the test byte to see if a process was interrupted by a power failure. If so, the stack pointer gets loaded with the address of the saved processor state, a return from interrupt is executed, and the process resumes.

### NOVRAM stores terminal configurations

An application in which NOVRAM is the device of choice lies in the storage of terminal-configuration information, consisting of such parameters as baud rate, data format and parity method. The conventional

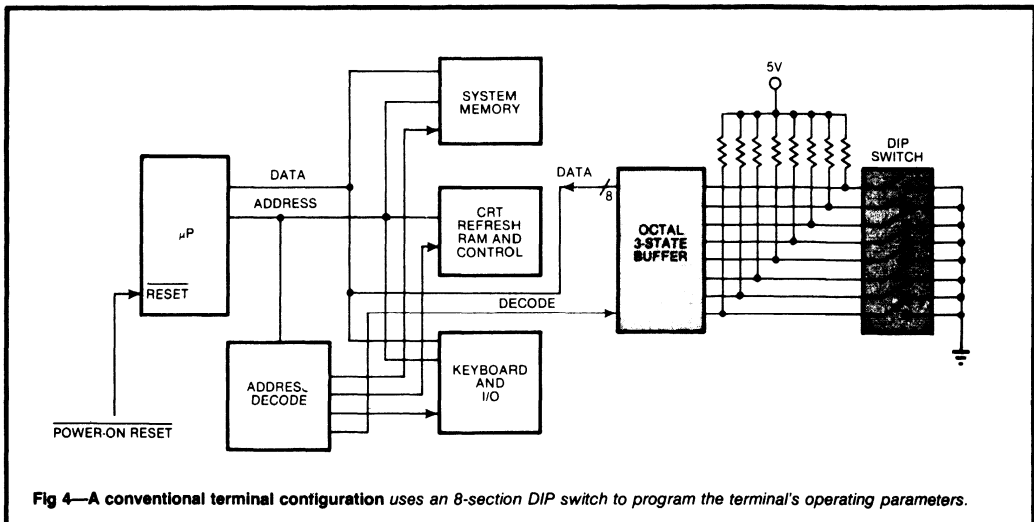
approach to this task (**Fig 4**) stores data in DIP switches on a pc board somewhere in the terminal; the user must have a terminal manual handy for decoding switch settings to change any of the preset features.

One alternative uses menu-driven configuration modes to set the terminal and a NOVRAM to store the terminal-configuration parameters. The user can easily change the configuration information for specific tasks and retain this data until the terminal loses power.

Upon power-up, a set of predefined default parameters stored in the NOVRAM's EEPROM section goes to RAM, and the terminal is configured. The NOVRAM also allows the user to change default parameters for subsequent sessions by transferring the modified RAM data to EEPROM—in either a general or privileged user environment. The NOVRAM's ability to manipulate two sets of data proves important here because the terminal software operates on the data in the NOVRAM's RAM section, regardless of whether the terminal is in the default configuration or a user-entered one.

In **Fig 4's** conventional approach, an 8-section DIP switch holds the configuration information. If a switch position is open, the pull-up resistor causes a ONE to appear at the buffer input; a closed switch denotes a ZERO. Decoding the buffer's address and reading the data provides the switch information. If the system needs more than eight bits, the design requires additional switches, resistors, buffers and logic.

If a block of memory addresses is reserved for configuration information, the granularity of the address decoding increases with the number of DIP



**Fig 4**—A conventional terminal configuration uses an 8-section DIP switch to program the terminal's operating parameters.



# In-system data modifications make EEPROMs more versatile than EPROMs

switches required. And you can change the default data only by altering individual switch positions.

The NOVRAM implementation of this system (Fig 5) permits the storage of 1k bits of configuration information in one 18-pin X2212. If you reserve an 8k memory-address block for configuration storage, the NOVRAM requires only a single chip-select decode. The only restriction in this arrangement is that four parameter bits get read simultaneously, rather than eight. Note that storing the same amount of information using the conventional approach calls for 128 DIP switches and octal buffers, 1024 resistors and sufficient address decoding to provide 128 separate locations within the 8k field—an address granularity of 64.

A terminal user employs the keyboard to enter operational parameters into the NOVRAM. The user enters a configuration mode when the terminal is in the off-line or local mode. A menu display shows the current terminal configuration; the user moves the cursor and/or strikes a control key to alter the current values. Once the configuration is established, the user exits the configuration mode, and the terminal operates according to the new parameters. The user can also change the default parameters by entering a control signal that places the new configuration mode in the NOVRAM's EEPROM section.

In this application, very few terminals would ever require the NOVRAM's full storage capacity for

configuration information. You could therefore employ the unused portion to store other operational and maintenance parameters.

## NOVRAM loader provides reusable memory

A system that employs a bootstrap loader during initialization is another prime NOVRAM application candidate. Examples of such applications include single-chip  $\mu$ Cs operating in external-memory modes and full-blown systems requiring the maximum allowable memory space. A common approach to this requirement stores the bootstrap program in ROM or EPROM. However, the program occupies memory space that might be used for other purposes during system operation. Because most initialization routines use a relatively small amount of memory space, this approach can be particularly wasteful in space-limited systems.

As an alternative, you can preprogram the bootstrap into the EEPROM section of a NOVRAM. Upon reset, the system generates a Recall signal to the NOVRAM, loading the bootstrap into RAM. The bootstrap program executes, and the NOVRAM RAM section then becomes free for other uses. This design feature even allows bootstrap-program alteration via external control for servicing or software updates.

Fig 6 shows a simple disk-oriented system that uses NOVRAM as a bootstrap memory. After booting, the NOVRAM becomes a global RAM. The device—and

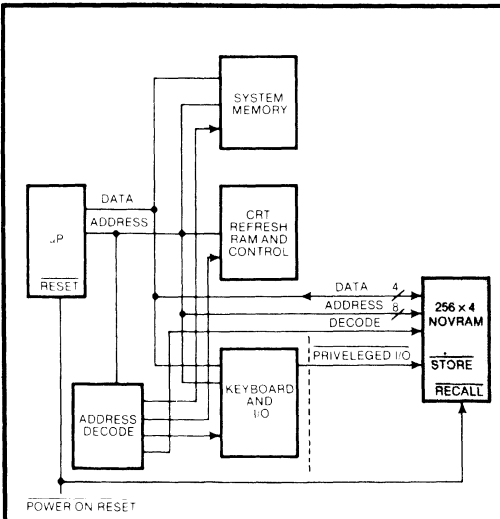


Fig 5—Replacing a DIP switch with a NOVRAM results in greater versatility for programming terminal operating parameters.

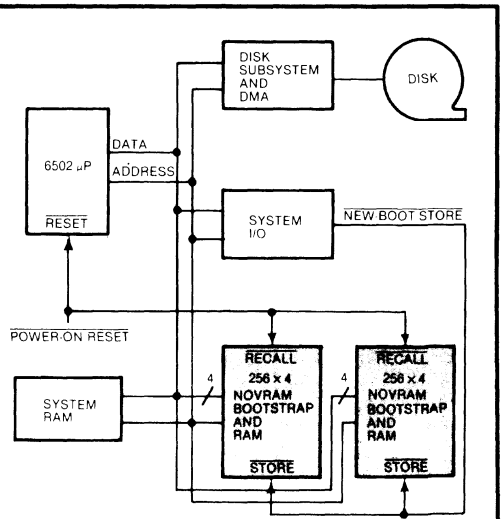


Fig 6—This disk-oriented system uses two NOVRAMs as bootstrap memory. Once loading is complete, the NOVRAM functions as global RAM.

```

;*****
; THIS PROGRAM SEGMENT DEMONSTRATES THE OPERATION OF A SYSTEM WHICH
; USES A BOOTSTRAP PROGRAM PRELOADED INTO THE NOVRAM'S EEPROM. UPON
; POWER-ON RESET, THIS BOOT IS RECALLED INTO THE EEPROM'S RAM. THE
; BOOTSTRAP PROGRAM CONFIGURES THE SYSTEM, AND THEN USES THE NOVRAM'S
; RAM AS REGULAR RAM. THE NOVRAM IS LOCATED AT THE BOTTOM OF THE
; 6502'S MEMORY MAP SO THAT THE HIGHEST LOCATIONS CAN CONTAIN THE
; PROCESSOR'S INTERRUPT VECTORS. ACTUAL LOADING OF THE OPERATING
; SYSTEM INTO MAIN MEMORY IS ACCOMPLISHED BY A DMA CONTROLLER, WHICH
; LOADS THE PROGRAM FROM THE DISK.
;*****
DMADATA      .EQU    0C000H    ;DMA DATA REGISTER
DMACTRL      .EQU    0C001H    ;DMA CONTROL REGISTER
PROGRAM      .EQU    00200H    ;START OF PROGRAM MEMORY

        .ORG    0FF00H

; THIS PROGRAM SECTION IS LOADED INTO THE EEPROM SECTION OF THE
; NOVRAM, AND IS RECALLED UPON POWER-UP.
BOOT     LD%      #0FFH        ;LOAD THE % INDEX REGISTER WITH FF
        TXS                ;TRANSFER TO STACK POINTER AT 01FF

CONFIGUR ; THIS CODE SECTION CONFIGURES THE DMA CONTROLLER,
        ; AND SETS THE INITIAL LOAD LOCATION AT 0200H, SO
        ; THAT PROGRAM DATA WILL NOT OVERWRITE THE STACK.

SEEK     ; THIS CODE SECTION TELLS THE DMA CONTROLLER WHAT
        ; DISK SECTION IT SHOULD GET THE PROGRAM FROM, AS
        ; WELL AS HOW MUCH DATA TO LOAD.

GO       LDA      #01          ; 01 IN THE DMA CONTROL REGISTER
        ; WILL INDICATE DISK DATA LOADING
        STA      DMADATA      ; STORE IN THE DMA CONTROL REGISTER
        LDA      #0ASH        ; WRITE TO TEST BYTE TO SIGNIFY BOOT
        STA      TEST        ; IF WE SEE A #0ASH, WE ARE IN BOOT

LOOP     JMP      LOOP        ; LOOP UNTIL DMA CONTROLLER INTERRUPTS
;*****
; NMI FROM DMA INTERRUPT WILL VECTOR HERE. THIS ROUTINE CHECKS THE
; STATUS FROM THE DISK-SUBSYSTEM AND DMA CONTROLLER TO INSURE THAT
; THE REQUESTED DATA HAS BEEN LOADED. ONCE A SUCCESSFUL BOOT HAS
; TAKEN PLACE, THE SYSTEM CAN CHANGE THE NMI VECTOR SINCE THE NOVRAM
; NOW FUNCTIONS AS A REGULAR RAM.
;*****
INTERRUPT LDA      DMACTRL    ; CHECK TO SEE IF THE DESIRED PROGRAM
        ; HAS BEEN SUCCESSFULLY LOADED. IF SO,
        ; ALL WILL BE ZEROES EXCEPT D0 WHICH
        ; WILL BE SET TO SIGNIFY THAT AN
        ; INTERRUPT WAS GIVEN.

        CMP      #01          ; ARE WE LOADED?
        BNE      BOOT        ; IF NOT, WE HAVE AN ERROR, RE-BOOT.
        LDA      TEST        ; GET TEST BYTE TO SEE IF IN A BOOT.
        CMP      #0ASH        ; IF SO, TEST BYTE WILL BE AS HEX.
        BEQ      PROGRAM     ; AND JUMP TO PROGRAM BEGINNING.
        ; OTHERWISE WE HAVE AN ERROR.

ERROR    .BYTE     00          ; A ZERO IS STORED IN TEST INITIALLY.
        .ORG      0FFFAH

NMI      .WORD     INTERRUPT ; NMI WILL GO TO SYSTEM START ROUTINE.
RESET    .WORD     BOOT      ; POWER-ON RESET WILL CAUSE AUTO BOOT.

```

**Fig 7—A 6502- $\mu$ P assembly-language boot routine is located temporarily in NOVRAM, which forms the highest 256 bytes of memory in this system.**

## Use EEPROM if data changes are byte size and infrequent

hence the bootstrap routine—is in the highest memory segment so it can hold all the interrupt vectors.  $\mu$ Ps such as the 6502 and 6800 use these locations for reset and interrupt pointers.

In the bootstrap program (Fig 7), the reset vector for the 6502  $\mu$ P points to the boot routine. Fig 6's two NOVRAMs reside in the highest 256 bytes of the address map. Upon power-up, the NOVRAM's EEPROM section gets loaded into the device's RAM section. The  $\mu$ P then initializes the stack pointer, and the DMA controller begins a data transfer from the disk. A test byte gets set to show that a boot process is under way.

Once the DMA transfer begins, the  $\mu$ P loops until an interrupt signifies that the operation is complete. The  $\mu$ P vectors to the interrupt-handling routine, which determines if a valid DMA has occurred. If an error has occurred, the program causes a jump to location Program, where the first byte of the loaded program resides. The NOVRAM RAM is then free for general use. Note that you must take care not to accidentally overwrite the interrupt and reset vectors, located in the highest memory locations.

### EEPROM stores controller parameters

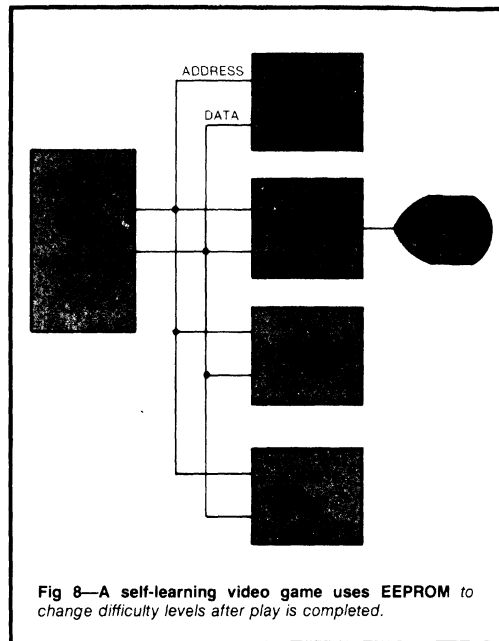
Turn now to some applications in which an EEPROM is the device of choice. One such task is the storage of coefficients in PID (proportional integral-differential) controllers.

Modern control applications such as the PID algorithm are characterized by two basic qualities. First, they are computationally intense. Second, their ability to precisely control a set condition is based on their knowledge of the effects of their outputs. This knowledge results from deriving the various controller coefficients via calculations: Each controller output must be calculated with reference to the previously defined term.

If a PID system loses power, it must resynthesize all data before it approaches the level of performance exhibited before the power loss. The data tables for each control task are fairly large and require a substantial amount of memory. Therefore, a controller might use EEPROM for algorithm-coefficient storage.

Note also that most PID-controller deviations result from the sensitivity of the system's sensors as well as the response time and accuracy of the control outputs. These variables might change in a particular unit but are usually the same when power returns to the controller; they need only be updated occasionally as the system runs. An EEPROM's slow write time and fast read time make it ideally suited for this infrequent-write application.

Finally, note that parameters stored in EEPROM are



available to the system whenever it's running—whether programmed into the system during initialization or resulting from previous system operation. An EEPROM implementation of such a system thus results in shorter system-interrupt recovery time as well as self-recalibration upon component replacement.

### Self-learning video games use EEPROMs

Another potential EEPROM application centers on the storage of self-teaching or self-modifying code, through which a process or algorithm can tailor itself based on the results of previous executions. Such applications are characterized by updates to program storage, which usually occur relatively infrequently. This high read-to-write ratio of memory access, as well as the densities required in the program store, generally dictate an EEPROM implementation.

An example of this application category is a self-learning video game (Fig 8). Such a game's success depends largely on its ability to keep a player interested by continually increasing the level of challenge after repeated plays.

At the end of a certain period (Fig 9), the game analyzes the scores and modifies its program (including timing loops and difficulty factors) to present a more complex play to the next group of players. The learning algorithm also makes the game easier to play under

certain conditions, preventing unwarranted increases in difficulty.

The initial game code includes several routines that

make the game progressively more difficult to play. These routines get bypassed in the initial program execution by always-executable branch instructions. At

```

;*****
; THIS IS AN EXAMPLE OF 6809 GAME CODE WITH BRANCH NEVERS
;*****
PLAY          ;THIS SECTION OF CODE IS THE EASIEST
;
;
SECT1          BRA      SECT2    ;WE START OUT BY BYPASSING THIS SECTION
;THIS SECTION OF CODE IS MORE DIFFICULT
SECT2          BRA      SECTN    ;WE ALSO BYPASS THIS SECTION
;
SECTN          BRA      ENPLAY    ;WE HAVE N DIFFICULT ROUTINES
;
ENPLAY         LDA      TEST      ;CHECK THE END OF GAME FLAG
CMPA           #0FFH    ;IT WILL BE AN FF IF GAME IS OVER
BNE            PLAY      ;IF GAME NOT OVER, GO BACK TO MAIN LOOP
BRA            FINISH     ;IF IT IS, GO TO FINISH SECTION

FINISH         ;THIS IS THE AREA FOR THE END OF THE GAME CODE. IT MAY
;CALL PROCEDURES TO MAKE THE GAME HARDER IF THE
;ANALYSIS OF PAST SCORES WARRANTS.
;*****
; THIS SECTION OF CODE INCREASES THE DIFFICULTY LEVEL OF THE GAME BY
; REPLACING ONE OF THE BRANCHES AROUND THE MOST DIFFICULT ROUTINES
; WITH A DUMMY BRANCH OR BRANCH NEVER INSTRUCTION. THIS ROUTINE ALSO
; INCREASES A GLOBAL DIFFICULTY FACTOR, ON WHICH MANY OF THE GAME
; PLAYING ALGORITHMS ARE COMPUTED, BY ONE.
;*****
DIFFULT        .BYTE    00      ;DIFFICULTY FACTOR
;
TABLE          TABLE OF BRANCH LOCATIONS
               .WORD    SECT1
               .WORD    SECT2
;
;
TABLEND        .WORD    SECTN

MAKEHARD       LDX      #TABLE    ;START LOOKING THROUGH TABLE AT THE TOP
LOOK           CMPX     #TABLEND  ;ARE WE AT THE END OF THE TABLE?
BEQ            NEXT            ;IF SO, GAME CAN'T BE MADE HARDER!
LDA            [X++ ]          ;LOOK AT THE OPCODE AT THE BRANCH, AND
                               ;INCREMENT INDEX REGISTER FOR NEXT LOOK
                               ;(AUTO INCREMENT BY 2 INDEXED)
CMPA           #21H            ;CHECK TO SEE IF IT IS A BRANCH NEVER
BNE            LOOK            ;IF NOT, THEN CHECK THE NEXT ONE
STA            [0,X]           ;OTHERWISE MAKE THE GAME HARDER BY
                               ;INCLUDING A ROUTINE BY SWAPPING A BRANCH
                               ;NEVER (INDEXED INDIRECT)
INC            DIFFULT         ;INCREMENT DIFFICULTY FACTOR

ATTRACT        ENTER    THE ATTRACT MODE FOR THE GAME
;
;
NEXT           ;WE CAN'T MAKE THE GAME HARDER, SO WHAT DO WE DO??
               .END

```

**Fig 9—**Written in 6809- $\mu$ P assembly language, this self-learning video-game program changes branch instructions based on previously obtained scores.

## EEPROM and NOVRAM could team up in some cases

the end of each play, the system determines from the score whether to make the algorithm more difficult. If so, it eliminates some of the branches around difficult parts of the game software. A simple table stores all of these branches. Other features, including speed parameters and energy levels, can also be stored to make the game more difficult as scores improve. Storing them in EEPROM provides the additional advantage of easy updates and changes in the basic table.

### EEPROM and NOVRAM team up

As a final example, consider how you might combine EEPROM and NOVRAM in an automobile navigational system that could direct a driver to a location within a specific city or area. Proponents of this approach envision beacons located throughout an area, notifying each in-car computer of the car's current location. Provided with this information, a local electronic map and the desired destination, the computer would direct the driver along the most efficient route.

Data-storage requirements would be extensive, implying the use of EEPROM. After all, the system must not only be programmed with a map of the area roads but must also be able to select between many possible alternatives based upon continuously changing factors such as time of day and known construction areas. Using EEPROM would allow the car's driver to load the navigational computer upon entering a location such as a filling station.

A NOVRAM would also prove critical to this application. It would contain rapidly changing current information, which would get transferred to the NOVRAM's EEPROM section upon reaching a destination. The approach allows power removal from the system while the car is parked, eliminating battery

drain. Restarting the vehicle would transfer the current data from the NOVRAM's EEPROM section back to its RAM section.

Fig 10 shows how the hardware could be implemented. Map information, stored in EEPROM, gets changed as necessary via the map-download controller, a serial interface over which the data is transmitted. The transmission rate is low because the map data is written into EEPROM, which specs a slow write cycle.

The system has two main interfaces—to the driver and to the vehicle. The former consists of a keyboard for input and a CRT for display of the map and other information. The latter receives data such as mileage and speed so that the system can monitor the driver's progress along a given route.

EDN

### Author's biography

**Richard Orlando** is product marketing manager at Xicor (Milpitas, CA), where his duties include product development. He is a member of the IEEE Computer Society, the ACM, Tau Beta Pi and Eta Kappa Nu. Rick holds a BS degree in computer-systems engineering from the University of Massachusetts at Amherst. His interests include research in the areas of distributed processing, reconfigurable processor architectures and  $\mu$ P applications.



Article Interest Quotient (Circle One)  
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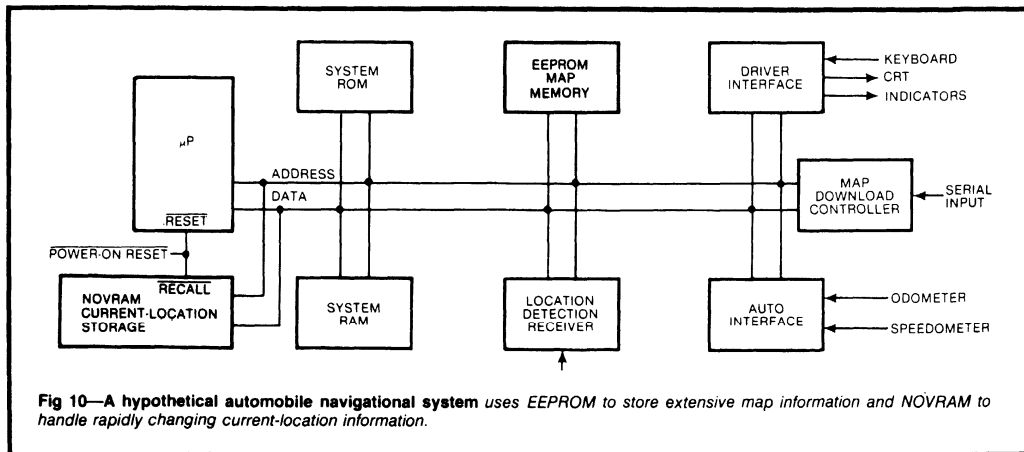


Fig 10—A hypothetical automobile navigational system uses EEPROM to store extensive map information and NOVRAM to handle rapidly changing current-location information.

# Non-volatile memories keep appliances out of the dark

Richard Orlando, Xicor Inc., Milpitas, CA

Appliance design has undergone a revolution in recent years. The advent of the low-cost, single-chip microcomputer has opened many applications for these small computers in the appliance market. Initial applications were based upon new types of appliances where digital control was a necessity. Today one sees even the venerable "white goods" using single-chip microcomputers to add features and capabilities to the end products. With this migration to digital control, a need for non-volatile memory has developed, and many new non-volatile memory devices have been made available to the designer.

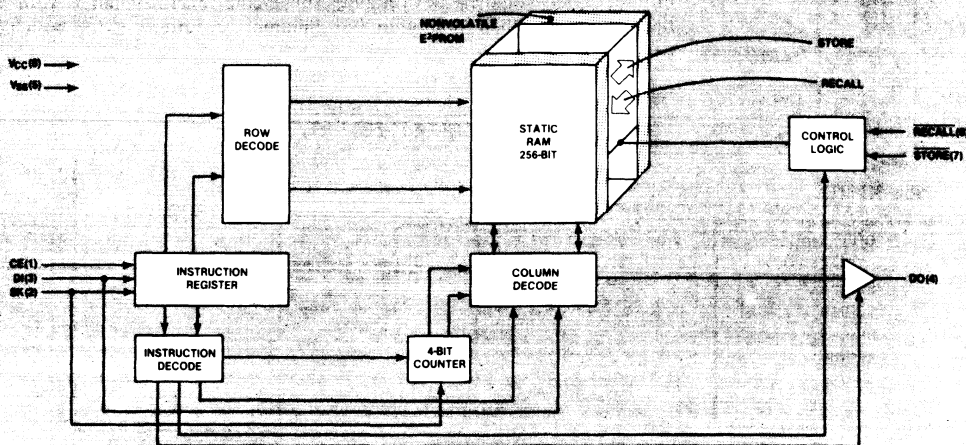
Appliance control applications have gone through an orderly evolution. The design methods of the past used electromechanical devices, such as switches, relays, mechanical timers and, of course, wafer switches. The requirements of older appliances could be easily satisfied by these devices. Washing machines, for example, using multi-plane wafer switches driven by a simple timer could initiate, time and terminate the different cycles of the laundry washing process. And the electronic range allowed simple electromechanical timing of a cooking cycle.

Since the appliance industry has

been subject to the whims and attitudes of the consumer, the desired capabilities of appliances have grown as a function of added features. A simple example is the evolution of the home stove controller: first, accurate control over cooking temperature, then the ability to turn off the oven after a programmed time, and, finally, the complete programmable oven that not only turns itself off after a programmed time has elapsed, but also initiates the cooking cycle at a certain time of day.

The increased capabilities of the appliances coupled with the availability of low-cost, single-chip micro-

Fig. 1  
FUNCTIONAL DIAGRAM  $\times 2444 (16 \times 16)$



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computers has led to the final step in the evolution, that of full digital control. The use of the microcomputer as a control mechanism allows the designer increased flexibility, reliability and precision in the control process, not easily attainable with the older design methods. Decreased development costs are also possible since a flexible digital controller can be used in a variety of different products, or models of the same product.

Microcomputer designs were not free of their own unique problems, however. The microcomputer interface required to perform the actual control functions was somewhat complex. New issues had to be addressed in terms of product reliability, since the semiconductor devices introduced different failure modes than those exhibited by electromechanical devices. The microcomputer also had a major disadvantage over prior design techniques due to its inherent volatile nature: when the power was removed from the appliance, the microcomputer not only stopped functioning, it lost any data it had maintained based upon the current state of the system.

One advantage that the older electromechanical timers possessed

was that if the power went off to the appliance, the control system would maintain the state it was in when the power was interrupted. When the power was restored to the appliance, it would continue from where it left off. One can easily appreciate the irritation of a homemaker who, having left a roast in the oven, returns from errands to find that it had not resumed cooking after a blackout.

### Emergence of non-volatility

With many appliance designs, there is a definite need to prevent such untoward situations. Some type of non-volatility is a necessity in appliance design. Since the cost of the appliance is a great concern, this non-volatility must be cost-effective. One of the earlier approaches was that of battery backup on the microcomputer itself, or on a separate CMOS memory in the system. The disadvantages of this approach are based simply on the limitations of batteries and the cost of implementation. Unfortunately, there were not many alternatives until now.

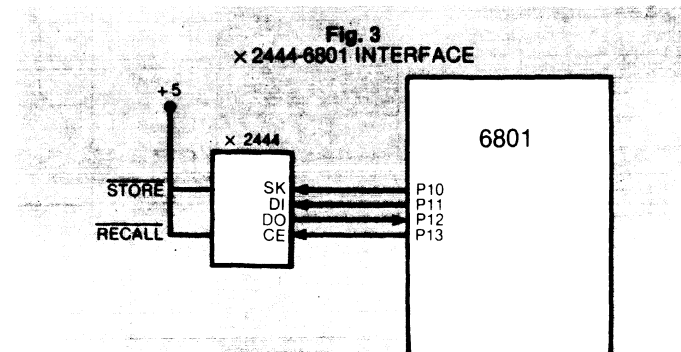
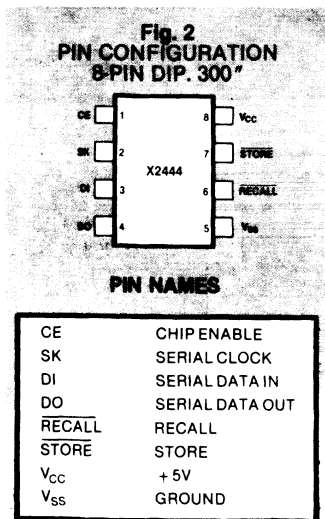
The past five years have seen a remarkable evolution in the emergence of semiconductor non-volatile memories. Unlike the battery backup of the data in either on-board or external RAM, these devices were able to retain data without the external power, in a manner similar to that of an EPROM. The main difference between these devices and the EPROM was their ability to be

"rewritten" in-circuit, as opposed to being removed from the circuit, erased, and then "reprogrammed" before they were put back into the circuit.

Unfortunately, these early devices were expensive and difficult to use. They required multiple "programming" voltages, extensive support circuitry, and were quite unreliable. These devices, for the most part, were organized for microprocessor "bus" applications, and as such required too many I/O lines for efficient interfacing to single-chip microcomputers, where I/O lines are a precious commodity.

The development of 5v floating-gate, NMOS non-volatile memories eliminated many of the disadvantages of semiconductor non-volatile devices. These devices not only decreased the support circuitry required for their use, but increased the reliability of the devices. Unfortunately, these devices were also designed for "bus" applications and were relatively expensive due to their large densities (>1k bits). A need was recognized in the appliance and other industries for an inexpensive and reliable non-volatile memory designed exclusively for interfacing to single-chip microcomputers.

The Xicor X2444 answers this need. The device is a low-cost  $16 \times 16$  non-volatile static RAM (NOVRAM for short) which features serial interface designed for interfacing to a single-chip microcomputer with a minimum requirement for both I/O



lines and software. Housed in an eight-pin mini-DIP, the X2444 provides inexpensive non-volatile data storage for both operational and configuration parameters. Its low cost (less than \$4.00 in unit quantities) makes it the least expensive non-volatile storage on the market, even rivalling the DIP switch in unit cost, while providing the equivalent of 32 DIP switches in terms of data capacity.

## The NOVRAM concept

The NOVRAM idea is not new. Xicor invented this type of memory more than three years ago. The concept is quite simple. Figure 1 shows a block diagram of the X2444. It consists of a 256-bit (16 × 16) static RAM with a 256-bit 5V E<sup>2</sup>PROM array overlaid bit for bit in a "shadow" type manner. Two signals, STORE and RECALL, control the transfer of data between the E<sup>2</sup>PROM array and the static RAM. The STORE function replicates the data which is currently in the RAM into the non-volatile E<sup>2</sup>PROM array. In a similar manner, the RECALL function transfers the non-volatile data in the E<sup>2</sup>PROM array into the RAM. One can see that by simply performing a STORE during power failure, the data is then retained in the non-volatile E<sup>2</sup>PROM, and can be restored to the RAM using the RECALL once power is returned to the system.

The X2444's serial interface method is ideal for microcomputer applications. Figure 2 shows the pinout and signal designation for the X2444. The four-line serial interface consists of a Chip Select (CS), a Serial Clock (SC), a Data In (DI) line, and a Data Out (DO) line. The Data In and Data Out timings are designed to allow the implementation of a single Serial Data line by typing both Data In and Data Out to a single I/O line from the microcomputer, reducing the I/O lines to three. All data transfer to and from the X2444 are performed over this serial interface by either synchronous 8-bit instructions or 16-bit data operations. The X2444 has two external pins, STORE and RECALL, for performing the non-volatile

operations via hardware control in the event of power failure. The X2444 also includes distinct STORE and RECALL instructions over the serial interface to allow only software control over the non-volatile operations.

The serial interface is accomplished using discrete "bit-banging" from the single-chip micro. An instruction is performed by loading an accumulator with the proper bit pattern, and shifting it out through an I/O line while toggling the serial clock low and then high again between each bit.

The software for this interface is simple, and an example of a 6801 implementation is shown in Figure 3. The software assumes that the X2444 is connected to bits 0, 1, 2 and 3 of the 6801 I/O Port 1. The interconnect between the 6801 and the X2444 is shown in Figure 4. The three main parts of the software segment are three subroutines, SHIFTIN, SHIFTOUT and DRIVE. The SHIFTOUT routine takes the eight bits of data in the A accumulator, and shifts it out through Bit 1 of Port 1. Between each data bit output the clock is toggled. This routine is used for either instruction or data output to the X2444.

The SHIFTIN subroutine gives the X2444 eight clock cycles, and shifts the data from the X2444 into the A accumulator. This routine is used only in the READ instruction. The DRIVE subroutine actually provides the driver to interpret the desired operation and issue the proper sequence of commands to the X2444. It should be noted that this sample interface uses the software-controlled STORE and RECALL commands and leaves the X2444 STORE and RECALL inputs tied to Vcc.

## E.g. . . . microwave oven controller

One of the newest appliances in the consumer environment is the microwave oven. This also proves to be an ideal example for the application of a non-volatile memory.

The microwave oven started with a control mechanism which was no

more than the simple electromechanical timer borrowed from electric ranges. Since the microwave oven cooks in times which are orders-of-magnitude faster than a conventional stove, it became apparent that an accurate and precise control mechanism was needed. The microwave was one of the first appliances to embrace full digital control using a single-chip microcomputer.

Figure 5 shows a typical microwave oven control system based upon the 6801 microcomputer. The user interface includes a keyboard, alarm and display, while the oven interface includes the magnetron control, door interlock, and an optional temperature probe. Non-volatile memory has been added to the system design through the use of an X2444. The interface method to the 6801 and the driving software are similar to that above. The key difference to note is the addition of an external signal to drive the STORE input. This allows the controller to automatically store the data in the RAM into the E<sup>2</sup>PROM upon Power-Failure. The circuitry in the power supply senses a loss of power by monitoring either the ac or unregulated dc levels. Once a power failure has been detected, the power supply circuitry pulls the STORE input low. The power supply circuitry need only ensure that Vcc is held valid to the X2444 for 10 msec, and all of the data in the RAM will be stored into the E<sup>2</sup>PROM array. Upon Power-on-Reset, the 6801 issues a RECALL command to the X2444, and all of the data is restored.

The remainder of the microwave control circuitry is fairly standard. A 4 × 4 keyboard provides an input mechanism for the user, while the status indicators and display provide visual feedback. A two-line magnetron control allows the use of variable power levels in the cooking process. Timing is performed using the 6801's internal 16-bit timer which is driven off the 60-Hz reference from the power supply. Standard features include a safety door



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interlock and alarm. Optional features are provisions for a temperature probe for magnetron control or temperature-based cooking algorithms. The a-d converter used for temperature sensing has a serial interface similar to that of the X2444, and is placed on the same serial bus. Distinct chip selects enable the X2444 or the a-d converter to be accessed. Many such devices are currently on the market including the new TLC540 from Texas Instruments.

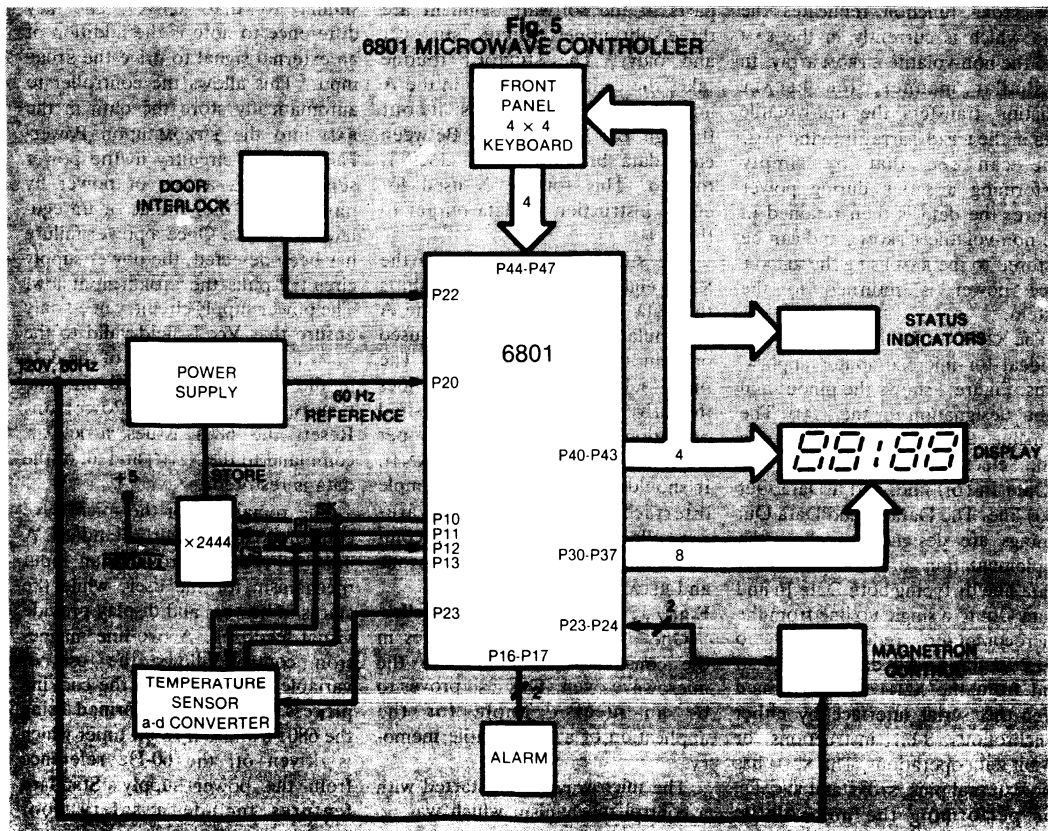
The X2444's non-volatile memory serves many functions in this application. Frequently used recipes or cooking sequences can be stored so that the microwave will sequence through a complex cooking algorithm automatically. The X2444's ability to store the data currently in the RAM into the E<sup>2</sup>PROM is very useful here. As the cooking process takes

place, the 6801 keeps a copy of the preset time and power setting in the X2444's RAM. As cooking time elapses, a location in the X2444 is updated to show the elapsed time. In the event of a power failure, the current values of these variables are automatically stored into the E<sup>2</sup>PROM section of the X2444. Once power is restored to the microwave, the data in the E<sup>2</sup>PROM is loaded into the RAM section of the X2444, and cooking continues from where it was interrupted. Intelligence can be added to the control algorithm to compensate for the continued cooking (due to retained heat) that occurs after the power outage.

The X2444's unique NOVRAM architecture makes such an application feasible. Since current E<sup>2</sup>PROM technology has limitations on the number of times that the non-volatile data

can be changed, one would not want to change the contents of the E<sup>2</sup>PROM each time the timer was incremented. If one were to use a typical E<sup>2</sup>PROM with a write limitation of 10,000 writes, the device would be worn out in a relatively short period of time at a write rate of one per second. Instead, the X2444 allows the system to update the E<sup>2</sup>PROM section of the chip only in the event of a power failure while using the unlimited RAM write capability of the X2444 every time the counter value changes.

The X2444's can also be used for a variety of other purposes in microwave design. As was mentioned earlier, one can save development time and money if a universal controller is designed. Many different models could use the same controller simply by adding circuitry



CODE AS OF AUGUST 22, 1983 Minimal Driver for X2444, 6801 Version 3.0

```
0000: .TITLE "X2444 DRIVER PROGRAM FOR 6801"
```

Checks for procedure code : 7999 verify

Current memory available: 7992

```
0000:                                .ORG 1000H
```

```

1000: ;*****

```

```

1000:          ;          DATA DIRECTION          HEX 0000
1000:          ;          PORT                      HEX 0002
1000:          ;                                PORT1          X2444

```

```

1000:                                     ; I/O 3                2444 SELECT        CHIP SELECT
1000:                                     ;
1000:                                     ;
1000:                                     ; COMMANDS ARE PASSED TO THE X2444 ROUTINE BY A PARAMETER IN THE

```

1000:	;	FOLLOWS.		
1000:	;	COMMAND CODE	INSTRUCTION	OPCODE
1000:	;	0	READ	1AAAA11X

```

1000:          ;          4          SLEEP          11111010
1000:          ;          5          SET WRITE ENABLE 11111100
1000:          ;          6          RECALL          11111101

```

```

1000: 0000      DIRECTION1      .EQU      00.
1000: 0002      PORT1          .EQU      02.
1000: 0080      TEMP1          .EQU      080H  ;RAM STORAGE FOR DATA

```

```
1000: 0080          ERRORDATA          .EQU          0080H          ;ERROR DATA
```

```

1000:                                ;XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
1000:                                ;
                                PROCEDURE INIT

```

```

1002: 97 00      STAA      DIRECTION1      ; WRITE TO DATA DIRECTION REGISTER
1004: 4F         CLRAR      ;SET CE TO 0(INACTIVE), DOUT AND SK TO 0
1005: 97 02      STAA      PORT1           ;AND STORE IN DATA PORT

```

```

0008      ; THIS ROUTINE TAKES THE DATA IN THE A ACCUMULATOR AND CLOCKS IT MOST
0008      ; SIGNIFICANT BIT FIRST INTO THE X2444.  THE FLOW IS SHIFT A BIT, TOGGLE

```

PAGE - 2 X2446

File: X2444 CODE AS OF AUGUST 22, 1983 Minimal Driven for X2444, 6801 Version 3.0

```
1008: C6 08          SHIFTOUT LDA#      #08.          ;LOAD THE BIT COUNT WITH 8
```

100F:	24	xx			{ENABLE, SERIAL CLOCK IS LOW,
1011:	CA	02	PCC	TRANS	{IF BIT IS A ZERO, THEN TRANSMIT
1013:	D7	00	ORAE	#02H	{IF IT IS A ONE, THEN SET DATA OUT
1015:	C6	01			
1017:	D7	00			
1019:	C4	1A	ANDE	#1AH	{KEEP THE DATA VALID, BUT SET SR TO ZERO
101B:	D7	02	STAE	PORT1	{AND STORE IN THE PORT
101D:	C6	14	LDAE	#14H	{TOGGLE CLOCK DOWN, SET DOUT TO 0, BUT KEEP
101F:	D7	02			
1021:	7A	0002			
1024:	26	EA			
1026:	49		ROLA		{ONE MORE ROTATE TO PRESERVE INSTRUCTION
1027:	39		RTS		{RETURN FROM SUBROUTINE

```

1028| *****
1028| !
1028| * TUBE ALUMINATE THE BATTERY IN ORDER OF DATA WITH ONE A ACCUMULATED FROM THE
1028| ** TO ENTER WITH THE CLOCK FOR

```

external to the 6801 microcomputer. Configuration information can be stored in the X2444 at time of manufacture which the 6801 can then determine upon Power-on-Reset to control the features and functions of its particular microwave. Additional X2444s can be added on the serial bus as user or model options. These optional X2444s require only an additional chip select, and can be used for such features as increased recipe storage or operational modes. The X2444's non-volatile memory also can be used for calibrating the temperature probe and storing the response time of the magnetron to allow quick calibrations or more complex and precise temperature-control algorithms.

### **General applications**

There are many other areas in the appliance field which are natural applications for the X2444. Since most electronic appliance controllers utilize the single-chip microcomputer, the X2444's serial bus is the ideal solution their non-volatile storage needs.

"User-programmable" parameters such as favorite stations, cooking algorithms or preset time-of-day events all make the appliances more "user-friendly" especially if these parameters are retained in the event of power loss. System configuration parameters can be stored in the X2444 to allow the design of appliances in a modular fashion, substantially reducing development costs while

increasing the reliability of each new product. System status saved in the X2444 in the event of a power failure is restored upon Power-On so that the system can complete interrupted tasks as well as ensure that the appliance is left in a safe and stable state.

The availability of the new 5V non-volatile memories allows the appliance designer to add more features and capabilities for a minimum cost. Whether it be used for power-failure data storage, or as user set-up information, the X2444 will make appliance designs less complex, more cost-effective, more fault-tolerant, and easier to use. □

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# NONVOLATILE MEMORY GIVES NEW LIFE TO OLD DESIGNS

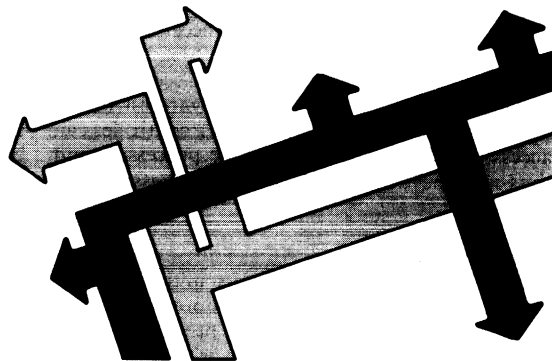
**Terminals and other equipment can be made more flexible, and product life can be extended by upgrading and customizing with NOVRAMs and EEPROMs.**

by **Richard Orlando**, *Xicor, Inc., Milpitas, Calif.*

The recent appearance of low cost, 5-V nonvolatile memories has led to design applications that can be broken into two distinct classes. One class uses nonvolatile memory to store such data as configuration or calibration parameters. This information can be updated and then stored in the device for access on power-up. The second application uses nonvolatile memory for program storage. Here, the nonvolatile memory's main advantage is that content can be updated or changed remotely, rather than by device replacement.

Unfortunately, many end products completed prior to the availability of these devices are threatened by newer designs. The latter take advantage of the added flexibility and features afforded by nonvolatile memory. There are, however, ways to add nonvolatile memory to existing designs without a major redesign.

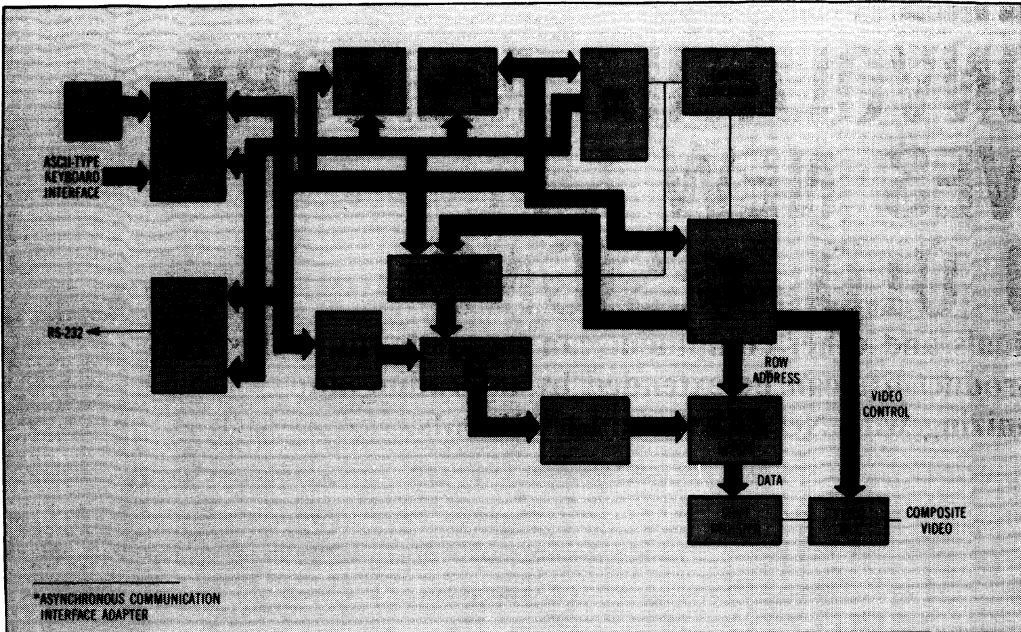
For example, consider the schematic of an intelligent terminal design, which will be used to illustrate methods that improve the flexibility of almost any microprocessor-based design (Fig 1). Here, the 6800 processor is the source of the "intelligence" in



the design. The serial communication channel is through a 6551 asynchronous communication interface adapter (ACIA), which features an onchip baud rate generator. A 2716 erasable PROM is the program store for the 6800, and the two 2114 RAMs provide 1 Kbyte each of buffer, stack, and parameter storage. The keyboard is an ASCII-encoded type whose inputs are fed through one port of a 6821 peripheral interface adapter (PIA). The other port of the 6821 receives the dual inline package (DIP) switch settings for such user-defined operational parameters as baud rate, parity, and protocol selections.

Video control is provided by a 68045 (or 6845) CRT controller. The display RAM interface is set up as a tightly coupled, shared RAM interface. The timing

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**Fig 1** The original terminal design has dual inline package (DIP) switch settings that must be read by the processor. They are then parsed to determine setup parameters invoked from the terminal program contained in the EPROM.

is such that the CRT controller only accesses the data in the display RAM during the bus “dead” time of the 6800. This allows the processor to access the data in the display RAM at any time, regardless of the state of the CRT controller. The CRT controller can access the RAM transparent to the processor, and thus can relieve the processor of any access arbitration tasks.

### Improving the design

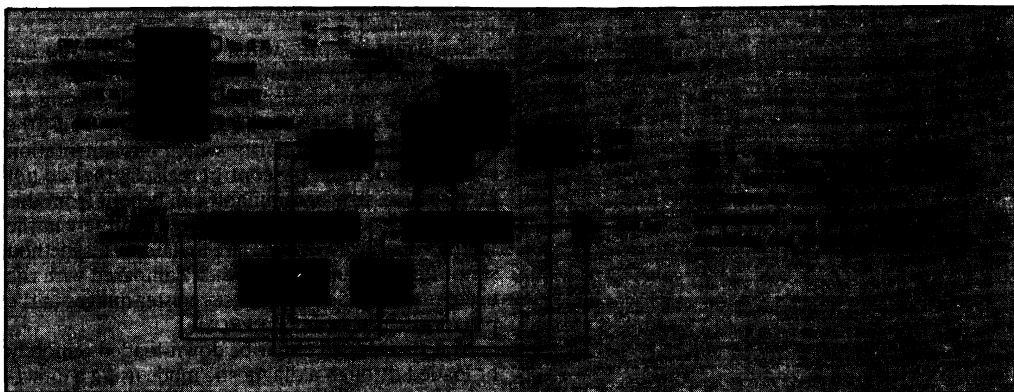
Although the design serves its initial purpose, several areas, which will make it more flexible and possibly extend the life of the product, can be improved. Intended for use in a variety of applications, the original design relies primarily on software for its characteristics and “feature set.” Simple changes to the erasable PROM containing the 6800’s software allow such terminal “customization.” This approach is adequate when end-user needs are known prior to manufacture. However, if a user wants to upgrade an existing terminal, someone must perform a costly EPROM change in the field. The same penalty applies to the manufacturer who wishes to “upgrade” the software of the existing units in the field, in order to increase performance or to eliminate possible errors.

The second area in need of improvement is the DIP switch used for the input of user-definable parameters. It creates many manufacturing problems, since most DIP switches cannot be

handled by automated assembly equipment, such as insertion machines and wave solderers. Additionally, because someone must manually toggle the switch through a sequence of positions in order to fully test the boards, DIP switches slow down automated board testing. Also, to change parameters, a DIP switch requires the terminal user to remove an access panel and manipulate switch toggles while referring to a manual. As the range of user-definable parameters expands to include such features as emulation modes, the problem becomes even more awkward.

In the example terminal, added features and enhancements can be made in two ways. The first involves replacing the DIP switch with an X2443 serial NOVRAM, which is used to store user-defined setup and configuration parameters. The second replaces the EPROM with an electrically erasable PROM.

The NOVRAM, a 256-bit serial device, is organized as 16 words of 16 bits each. All communication between the device and the processor is done in a bit-serial fashion using the data in input, data out output, and the synchronous clock lines shown in Fig 2. All operations are controlled by the microprocessor through the serial interface. Read and write operations are executed through the transmission of a specific 8-bit instruction code with an embedded address of the word to be accessed. In the write operation, the processor follows the write command with 16 bits of data to be written. In the



read operation, the processor supplies the read instruction, and then gives the X2443 16 clock cycles, which the device uses to output the data to be read. The NOVRAM also includes several non-data types of instructions to control the nonvolatile operation of the part, the part's power consumption, and the write/store lockout feature.

The X2443 is designed to interface with single-chip microcomputers when the main consideration is minimizing I/O lines and software overhead. This device also works well in microprocessor-based designs requiring upgrading with minimal design changes. It consists of a serial static RAM overlaid or "shadowed" bit-for-bit with a 5-V EEPROM array, as shown in Fig 2. The execution of a store operation, either from the input STORE or by the execution of the software store instruction, transfers the current contents of the SRAM *en masse* into the nonvolatile EEPROM array. In a similar manner, the execution of a recall operation, via the RECALL

input, transfers the contents of the nonvolatile EEPROM array into the SRAM array. On power-up, the contents of the EEPROM array are automatically loaded into the RAM array for a default configuration.

When using the X2443 to replace an existing DIP switch, it is advantageous to drop the NOVRAM into the existing switch "footprint." Fig 3 shows the simple conversion of the existing site or socket (a) to accept the X2443 (b). Four of the eight 6821 I/O lines used to read the DIP switch are already mapped into pins 1 through 4 of the NOVRAM. These lines originally input the current settings of the DIP switches, but can be configured through the 6821's data direction register to serve as the three outputs and one input needed for interfacing the NOVRAM. Since hardware STORE and RECALL signals are not needed in this application, they are simply tied to VCC. All nonvolatile operations occur through software control, whose requirements are relatively

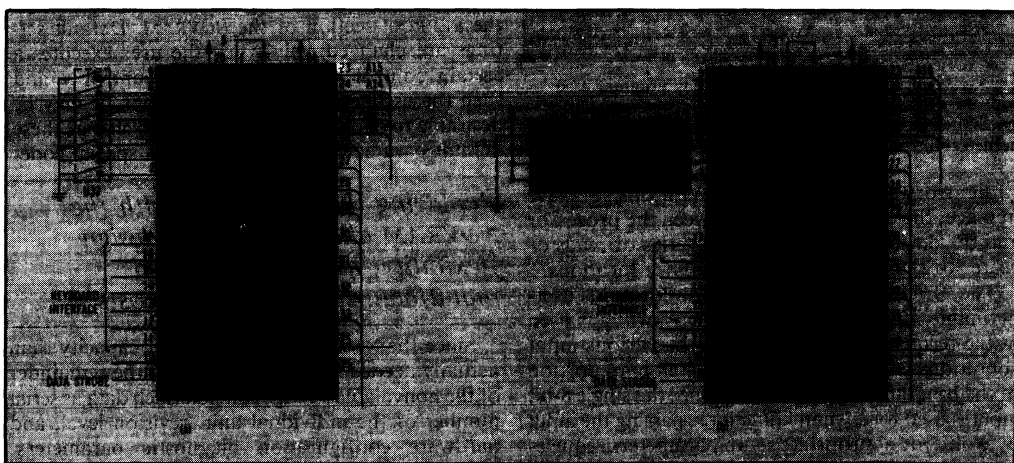


Fig 3 Within both the original DIP interface (a) and the X2443 implementation (b), the interface is serial. Therefore, only the clock, enable, data input, and data output lines need to be used.



PROCEDURE RESET							
THIS PROCEDURE IS RESPONSIBLE FOR CONFIGURING THE TERMINAL TO THE MODES SPECIFIED AT POWER-UP TIME ON THE FUNCTION DIP SWITCHES TIED TO PIA PORT A.							
BITS	7	6	5	4	3	2	1
PORTA	PARTY	AUTOLF	AUTOLF	DUPLEX	LINE	BAUD	RATE
ODD/EVEN PARITY							
0=ODD PARITY							
1=EVEN PARITY							
AUTO LINE FEED							
0=NORMAL							
1=AUTO LINE FEED							
(FOR ALWAYS FOLLOWED BY LF)							
AUTO NEW LINE							
0=NORMAL (INPUT STOPS AT LINE END)							
1=AUTO NEW LINE (INPUT WRAPS AROUND)							
FULL/HALF DUPLEX							
0=HALF DUPLEX							
1=FULL DUPLEX							
LINE/LOCAL							
0=LOCAL							
1=LINE							
BAUD RATE SELECTION							
000= 50 BAUD							
001= 110 BAUD							
010= 300 BAUD							
011= 600 BAUD							
100=1200 BAUD							
101=2400 BAUD							
110=4800 BAUD							
111=9600 BAUD							
SUBROUTINE PROCEDURES: HOME							
CLEAR							
GLOBAL VARIABLES							
USED: NONE							
ALTERED: CAPIA							
CE-PIA							
D-PIA							
DE-PIA							
HEAD							
TAIL							
AUTOLF							
NEMCM							
FULLDP							
LOCAL							
CMACIA							
CMACIA							
A ACCUMULATOR							
B ACCUMULATOR							

Fig 4 When using a header for a parsing program used with the DIP switch configuration, the possible parameters are limited to 8 bits, and an elaborate software routine is needed to interpret them.

straightforward (as described). With this software in place, the communication between the processor and the device simply becomes a series of reads or writes to the appropriate serial device locations.

The original design only allowed eight user-definable inputs, since only one DIP switch is used in the terminal. The meaning of the various input conditions is shown in the DIP switch map portion of the program header in Fig 4. Since the single 8-bit input is used for so many functions, parsing the input byte into the appropriate setup parameters requires an extensive piece of code. The problem with this implementation is the extensive software required

to make switch operation straightforward in the user's manual.

Replacing the DIP switch with the NOVRAM has several significant advantages. The 256-bit nonvolatile storage leaves adequate room for storing an "image" of all interface circuit registers. Thus, the parsing problem of the DIP switch implementation is eliminated. Even the control registers that do not need to be user-programmable can benefit from this imaging, since they can be changed remotely in the field for hardware or software updates. This method simplifies field upgrading when compared with the usual method of storing these register images in the program store ROM or EPROM.

New images can either be down-loaded remotely or loaded through a diagnostic mode using a direct-connect RS-232 interface. Examples of where this capability is beneficial are numerous, and include changing interface protocols, data formats, or other hardware, interface, or networking options.

The use of the device for storing setup parameters also allows a more user-friendly operator interface. Software in the original design includes routines that allow random placement of the cursor or text through the use of a "go to X-Y" routine. It becomes a fairly trivial task to implement a menu-driven setup mode. After entering a certain escape sequence, the user is placed in the configuration mode, which presents an English menu.

The return key increments the cursor position to the next setup area where the current setting is displayed, and the spacebar key increments that setting through all possible choices. Once the user has set up the parameters for a particular session, depressing the escape key writes the current settings into the RAM section of the NOVRAM. With this operation, the user can set up a temporary configuration without changing the default parameters in the EEPROM section of the NOVRAM. Default settings are changed only when the user executes a certain control sequence (such as control X and then the escape). In some applications, it may be desirable to allow only certain users to change these default parameters before entering a special code.

### *Replacing the DIP switch with the NOVRAM allows increased design flexibility, as well as reduced manufacturing and testing costs.*

Since the X2443 has a much larger capacity than actually needed for this application, the remainder of the nonvolatile storage can hold such data as serial number of the individual unit, revision level, and hardware configuration diagnostic parameters. Otherwise, it can be reserved for future expansion. The Table shows a sample address map for the

Location	Bit map	Interpretation
0	XXXXXXXXWWXB88B	S = Stop Bit Control WW = Word Length B88B = Baud Rate
1	XXXXXXXXPPPETTRD	PPP = Parity Check Controls E = Normal/Echo Mode TT = Transmit Controls R = Receiver Interrupt Enable D = Data Terminal Ready Control
2	XXXXXXXXEEEEEEEE	E = Emulation Designator (1 of 256)
3	SSSSSSSSSSSSSSSS	S = Serial Number
4	AAAAAAAAAAAAAAAA	R = Revision Level
5	XXXXXXXXXXXXXXXXXX	L = Latch data from keyboard on high-to-low or low-to-high

X = Don't Care

device, with the associated data stored in each of the 16-bit locations. The end results of replacing the DIP switch with the NOVRAM are increased design flexibility, as well as reduced manufacturing and testing costs.

### Program storage considerations

The second aspect of improving the terminal design involves the program store for the 6800 microprocessor. The original design uses a 2716 EPROM since the software requirements for the terminal are not extensive. The feature set of the X2816A EEPROM makes the replacement easier because EEPROMs of the X2816A generation incorporate high voltage generation, address and data latching, and the write-cycle timing circuitry on the memory chip. During read operations, the device functions just like the 2716 EPROM in its use of chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) signals. During a write operation, the X2816A latches the addresses on the bus during the high to low transition of the write enable ( $\overline{WE}$ ) signal, and then latches the data to be written on the rising edge of the  $\overline{WE}$  signal.

The duration of this signal is not important, since the EEPROM only uses it to initiate the write cycle; the timing for the write operation is generated on-chip. The processor needs only to ignore the EEPROM for 10 ms during the write cycle, and the device does the rest. The latched and self-timed nature of the X2816A allows it to be placed in a 16-K SRAM socket and be read and written with the same signals used for the SRAM.

The read operation of the X2816A is the same as that of the 2716 EPROM, so this part of the EEPROM operation is of no concern. The only changes required to the existing circuitry involve the write operation. The first change allows the processor to write to the EEPROM, and the second protects the EEPROM from unwanted write operations during power-up and power-down.

The memory map for the original design was not very full, so only large blocks of the address map

are decoded for each memory device and I/O chip on the bus. The 2716 logically resides at addresses F800 through FFFF since the 6800 reset vectors must be included. The physical decoding for the 2716 includes the address range of F000-FFFF since only the microprocessor's two most significant address lines A15 and A14 are used for the decoding.

Since line A14 is used to drive the  $\overline{OE}$  line of the 2716, the EPROM is selected whenever A15 is a logical one. Possible conflict with the system RAM residing at 8000-81FF is avoided by restricting the processor's access to the 2716 in the logical F800-FFFF range. Since the processor can now read and write to the logical address range of the 2716 socket, the  $\overline{CE}$  must also be derived from the A15 and A14 address lines. And, since  $\overline{CE}$  is active low and the address line is active high, a simple NAND gate will suffice (Fig 5). Luckily, an extra NAND gate in the

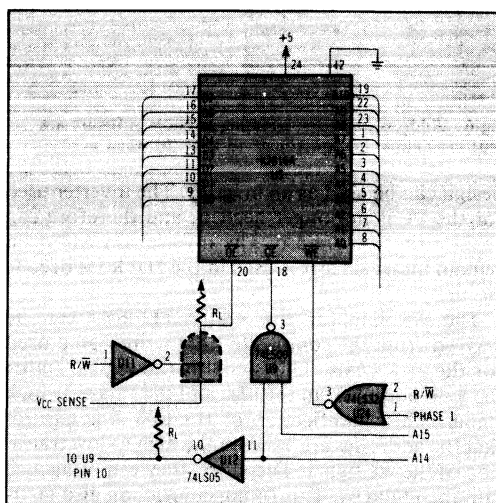
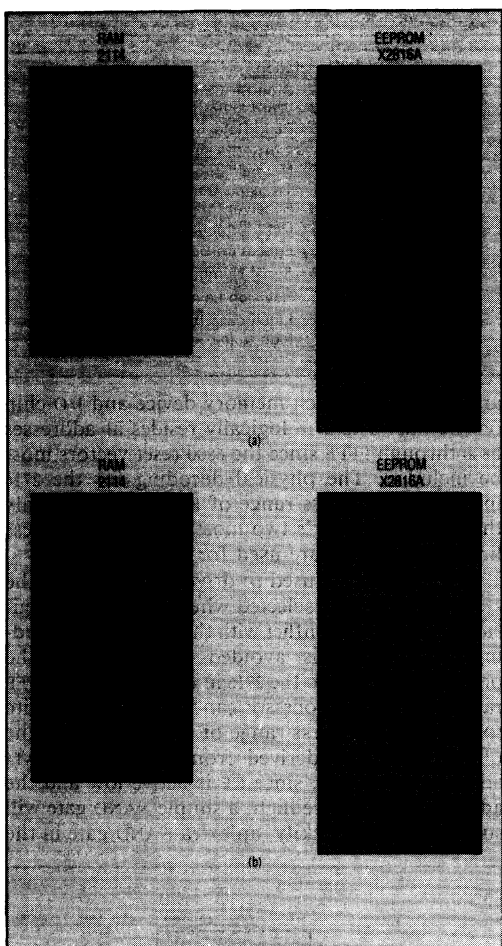


Fig 5 The EEPROM control logic uses the processor's high order address lines to map the device into the proper address range and enable it at the same time.





**Fig 6** Address maps for updating EEPROM software are kept in EEPROM (a) and copied to RAM (b) when needed.

design can be used as an inverter. The inverter used for the  $\overline{CE}$  is no longer needed, and therefore can replace the NAND gate. The inverter on A14 must remain intact since it is used in the 2114 RAM decode circuit.

The  $\overline{WE}$  line for the X2816A EEPROM can be derived from the composite RAM write signal used for the 2114 RAMs. This signal is the logical OR or the  $R/\overline{W}$  output from the 6800 and the Phase 1 clock signal. This qualification of the  $R/\overline{W}$  line ensures that the addresses are valid on the high to low transition of the  $\overline{WE}$  signal. Therefore, they can be latched into the EEPROM. This ORing connection also guarantees that the data to be written is valid on the rising edge of the composite  $\overline{WE}$  signal. The  $\overline{OE}$  signal on the EEPROM can simply be driven from the complement of the  $R/\overline{W}$  signal from the processor. This

technique requires that all accesses to the EEPROM be made in the logical address range of F800-FFFF to avoid bus contention with the system RAM.

Discussion of the circuitry needed for the  $\overline{OE}$  signal also must include another important issue: ensuring that the chip does not experience an accidental write cycle during power-up or power-down. Even though the chance of  $\overline{CE}$  and  $\overline{WE}$  going low during power-up or power-down is rather remote, the possibility must be eliminated.

The EEPROM simplifies write protection by including an onchip voltage sensor that monitors the  $V_{CC}$  input level and automatically disables writes from occurring when  $V_{CC}$  falls below 3 V. Also, a noise filter on the  $\overline{WE}$  input prevents a write from being initiated by a low spike. Functional interaction of the control inputs on the chip allows a low level on the  $\overline{OE}$  to disable any write operations regardless of the state of the  $\overline{CE}$  and  $\overline{WE}$  inputs. By holding  $\overline{OE}$  low while  $V_{CC}$  is between 3 and 4.75 V, inadvertent write cycles are inhibited.

The power supply must be modified to generate an active low signal whenever  $V_{CC}$  is below a specific level. This signal disables the write operation during both power-up and power-down. Because this signal is wire-ANDed with the control signal driving the  $\overline{OE}$  signal, all writes to the chip are disabled when  $V_{CC}$  is below the 4.75-V limit.

### Software modification

Once hardware changes have been made, in-factory modifications and in-field modifications must be addressed in order to take full advantage of an X2816A. In-factory modifications can be handled in many ways. If the terminal configuration is known at assembly time, the appropriate software can be loaded into the EEPROM through the use of a standard PROM programmer. However, this method does not take full advantage of the features of the in-circuit reprogrammability inherent in the X2816A. A more advanced approach also makes automated board testing easier.

For example, the EEPROM can be initially installed with a diagnostic program for testing the completed terminal board with an automated test system. Once the board has been tested, the tester controls the 6800 processor by holding it in a quiescent state such as reset or halt. The tester then assumes control over the terminal bus and writes the actual terminal software into the EEPROM. This greatly reduces the overhead required to manufacture a variety of different configurations or "models" on a single assembly line. In-line programming also allows for the verification of the EEPROM write operation and control circuitry.

The real advantages of the EEPROM surface when it comes to modifying software in the field. In this case, the terminal is placed in a down-load mode,

and the software revision is loaded through the RS-232 interface, either from a service "box" or remotely via a modem. The X2816A allows the terminals in the field to be called over phone lines for loading new operating software, thereby greatly reducing the cost and impact of a software update.

Although full-featured EEPROMs such as the X2816A simplify this task significantly, there remains one software issue to be resolved. While the EEPROM is performing its internal write cycle, it is unavailable for further writes or reads. For example, the processor, executing out of a program stored in the EEPROM, might perform a write cycle to the chip and then fetch the next instruction. Since the X2816A is occupied with its internal write cycle, the next instruction fetch will yield a high impedance bus. The processor will take this data as its next instruction and enter the "catch fire and die" mode of operation.

To avoid this situation, a very compact routine fetches the byte to be written into the EEPROM from a given location, writes the byte into the EEPROM, and then enters a timing loop to wait the 10-ms period required to complete the write. Since the RS-232 interface supports full handshaking, there is no chance of overrun from the down-loaded data. This routine is initially loaded into the EEPROM, but it is never executed from this device. Instead, another

"copy to RAM" routine copies the routine from EEPROM into RAM, from which it is executed.

Since the terminal has 1 Kbyte of RAM capacity, there is ample room for storing such a routine during the EEPROM write cycle. Fig 6 shows address maps for both the EEPROM (a) and the RAM (b) prior to and during the execution of the EEPROM write routine. This method works especially well with the 6800 since its architecture is that of a von Neumann machine, and can therefore execute program segments out of the memory space reserved for RAM data storage.

In-field terminal upgradeability has two important benefits. If the terminal software is upgraded or revised after the unit is sold, the new software can be added to the existing units in the field at minimal cost. This method also eases the addition of optional hardware in the field, since the new software supporting the hardware option can be down-loaded instead of replacing the terminal EPROM.

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## NOTES

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# EDN

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

## Save volatile data during power loss

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# Save volatile data during power loss

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*Nonvolatile-storage devices give you a medium in which to store data during power loss. By combining these devices with power-sensing circuits and supplying the necessary control signals, you can design a system that transfers data securely between volatile and nonvolatile memory during power loss.*

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*Xicor, Inc.*

To protect volatile data during power loss, you need to transfer that data reliably to nonvolatile memory during the transient and return it to RAM after power is restored. A system that performs this function includes two subsystems. The first reports power status, indicating when power is lost and when it is restored; the second handles the data transfer, using the power-status signal to generate the appropriate store and retrieve commands.

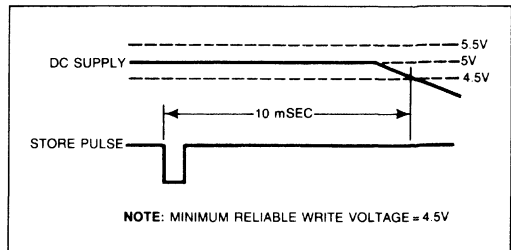
## **Sense power failure**

To transfer data reliably after power loss, a system must have enough time to copy data from RAM to nonvolatile memory before the supply voltage drops below a certain level. The sensing circuit must recog-

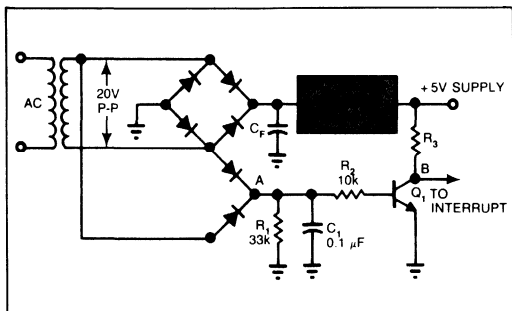
nize the power loss and generate a power-loss signal promptly, giving the storage subsystem enough time to effect the data transfer. In fact, in some systems, you may have to complete your transfer within a single write cycle to ensure a reliable transfer.

Your first step in designing the sensing subsystem is to choose a sensing point. You could use the 5V regulator's output as a sensing point, but this output will not indicate power loss as quickly as will either the ac input line to the power supply or the unregulated dc voltage supplied to the regulator.

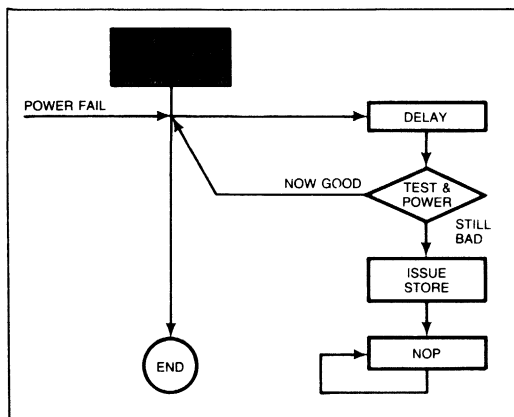
To sense ac loss on the power supply's ac input line, you can monitor either the input or the output to the power transformer. If you monitor the transformer's input side, you must electrically decouple the sensing circuit's signal from the system's dc portions (by using optoelectronic isolators, for example). If you monitor



**Fig 1—The system characterized by this timing diagram must detect a power loss early enough to allow it to generate a store pulse 10 msec before the dc supply drops to 4.5V.**



**Fig 2—This zero-crossing detector** monitors power-supply status at the transformer's ac output. The two diodes isolate the detector from the main power supply's unregulated dc bus.

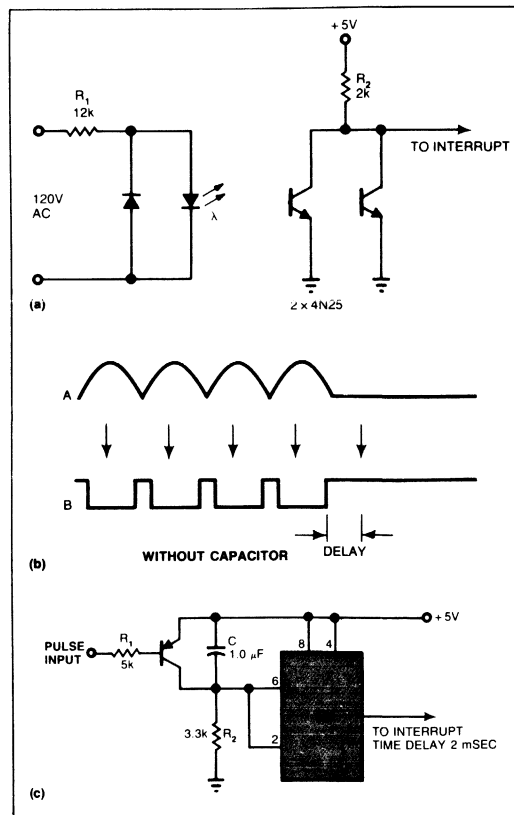


**Fig 3—In a typical  $\mu P$  system** that tests for power loss, once the processor receives an interrupt indicating a power loss, the system initiates a subroutine that tests for a true power loss. The subroutine first produces a delay of about 2 msec; then the system looks again at the power detector's output. If that output is still asserted, the system decides that the power loss is real and sends a store pulse to the nonvolatile RAM.

the output side, you must isolate the detector circuit from the main power supply's filtered unregulated dc circuit, because that circuit's response to a line fault is slow. To isolate the circuit, you can use either a separate transformer tap or two extra diodes between the bridge and the detector.

Alternatively, you can use the unregulated dc voltage ahead of the regulator as a sensing point. The regulator maintains its regulated output as long as its input voltage remains within a certain range. To make sure that the system will have time to respond to a power loss, you should set your trip point below the normal input voltage. This allows you to send your store signal early enough to ensure a reliable transfer to nonvolatile memory. Consider, for example, the timing diagram in Fig 1 and assume that the minimum reliable write voltage of the memory in the system it characterizes is 4.5V. Because this system's dc supply drops to 4.5V 10 msec after initiation of the store pulse, the system must complete a write operation to nonvolatile memory within this 10-msec period.

Once you've chosen a sensing point, you must choose a detector. If you've chosen to detect ac loss, consider one of the following four methods. The first is a low-cost zero-crossing detector (Fig 2), in which two diodes isolate the detector circuit from the filter capacitor ( $C_F$ ) that's ahead of the regulator. When a power loss occurs, the full wave's rectified ac drops to zero, inhibiting base current to transistor  $Q_1$ . This causes  $Q_1$ 's output to go high, thereby generating an interrupt signal at point B.



**Fig 4—You can connect a detector like this one**, (which contains optoelectronic isolators with their diodes connected back-to-back) directly to the ac line through a resistor (a). The circuit produces an output pulse that can interrupt a  $\mu P$  each time the input waveform crosses zero, or every 8.3 msec (b). Instead of allowing the sensor to interrupt the  $\mu P$  every 8.3 msec, you can feed these pulses first to a 555 timer that's configured as a missing-pulse detector. It issues an interrupt only when the input pulse train is interrupted (c).

*To ensure that you'll be able to transfer data reliably from RAM to EEPROM, you need to maintain power for at least 10 msec after a power loss.*

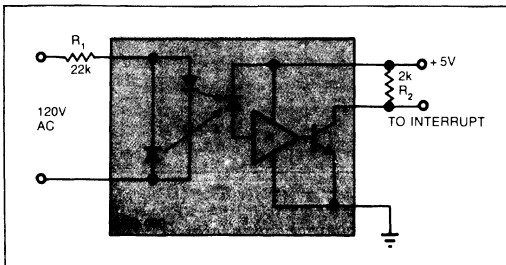
When it receives an interrupt, the system initiates a subroutine that tests for a true power loss (Fig 3). The subroutine delays the store signal for about 2 msec and then looks at the detector again. If the output is still high, the system decides that the power loss is real, and it sends a store pulse to the nonvolatile RAM. Resistor  $R_2$  in Fig 2 limits the transistor base current.

Capacitor  $C_1$  is essential in this circuit because it filters the power supply's half-cycle pulses before they're applied to  $Q_1$ . (If you were to fail to filter these pulses, the  $\mu P$  would receive an interrupt signal every 8.3 msec, whether or not a power loss had occurred. Without  $C_1$ , as much as 25% of your available processor time would be spent responding to false interrupts generated by the power-loss detector.) The value that you choose for  $C_1$  depends on the power supply's holdup time, the values of  $R_1$  and  $R_2$ , and the delay that you want between the loss of ac and the triggering of the store signal.

#### Use optoisolators

The second technique for sensing ac power loss uses two optoelectronic isolators between the detector and the ac power line (Fig 4a). This technique produces a positive output pulse at each zero crossing on the ac line, or at 8.3-msec intervals (Fig 4b). The problem with Fig 4a's circuit is that the interrupt signal occupies the  $\mu P$ 's time while the rest of the system is resampling the detector's output. To solve this problem, you can add a missing-pulse detector similar to the one shown in Fig 4c.

A third detector that relies on direct ac-line connection uses General Instrument's MID 400 power-line monitor. When you use this device, you need to add only two resistors to ensure a clean interrupt signal



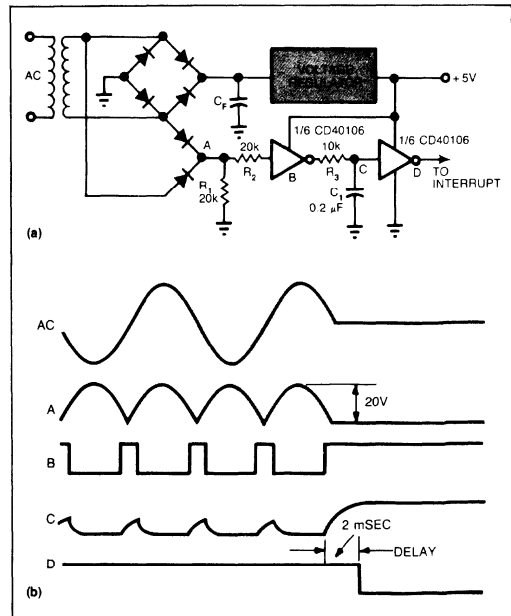
**Fig 5**—To incorporate the MID 400 detector in your sensing subsystem, you need to add only two external resistors that you connect directly to the ac line. You can control the on and off delays at the output by connecting a capacitor across  $R_2$ .

(Fig 5). You can adjust turn-on and turn-off delays by adding a capacitor across  $R_2$ .

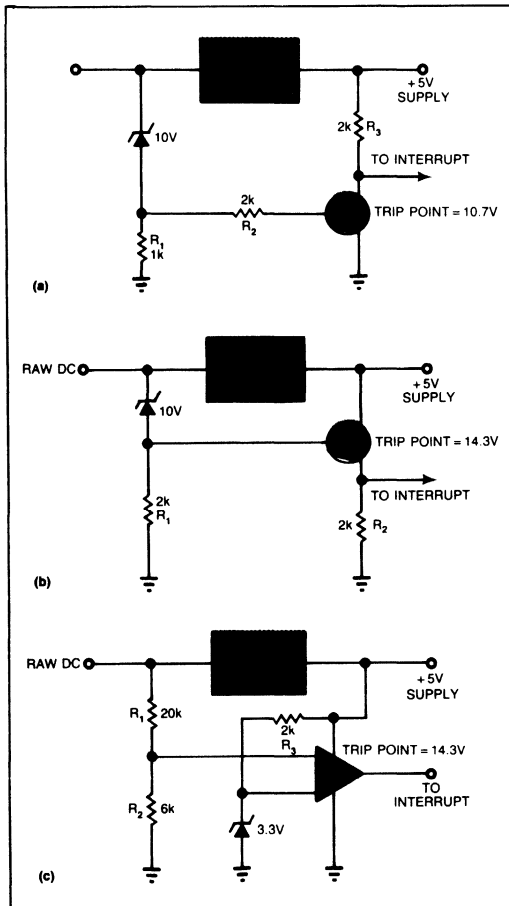
The fourth detector (Fig 6) uses a CMOS Schmitt trigger as a full-wave, low-voltage, missing-pulse detector. To avoid latch-up, and possible damage to the CMOS circuits, you must make sure that the input voltage to the CMOS Schmitt trigger does not exceed the 5V supply voltage. You can meet this requirement by inserting a resistor between the Schmitt trigger and the bridge's output. To obtain narrow pulse widths from the first gate, keep the ac input voltage as high as possible.  $R_3$  and  $C_1$  determine the output's delay, which must be longer than the first gate's pulse width.

#### Sensing dc power loss

If you've decided to sense dc loss instead of ac loss, you don't have to worry about capacitor delays or missing pulses. Consider the sensor in Fig 7a, for instance. The sensor generates a negative interrupt pulse when it senses dc loss; it uses a zener diode to set the trigger point. On one hand, you should set the



**Fig 6**—When you use two Schmitt triggers to detect ac loss (a), the delay produced by  $R_3$  and  $C_1$  must be longer than the first gate's output pulse width. The timing diagram (b) shows the circuit waveforms.



**Fig 7—Using zener diodes** you can configure a power-supply detector circuit to produce either a negative (a) or a positive (b) interrupt pulse when the trigger point is reached. You can configure the op amp shown in c to produce either a positive or a negative output pulse polarity.

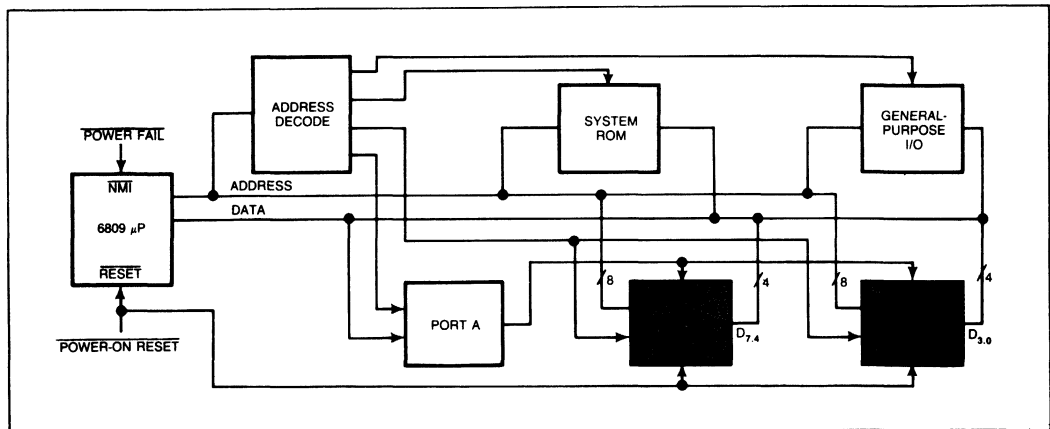
trigger point as high as possible (to allow the circuit to sense the power loss as early as possible). On the other hand, you must still set the trigger point low enough to fall below the lower boundary of the supply's upper unregulated limit (to prevent false triggering). Remember that the diode's voltage rating should equal the desired trip-point voltage minus the 0.7V base-emitter drop.

In the dc detector circuit shown in Fig 7b, when the unregulated dc voltage drops, a pnp transistor turns on and produces a positive pulse. Here, the zener diode's rating is equal to the trip-point voltage minus 5V, plus 0.7V for the base-emitter drop.

The circuit in Fig 7c trips when the dc level at R<sub>1</sub>'s and R<sub>2</sub>'s junction drops to the zener's voltage rating. You can provide either a positive or a negative interrupt signal, depending on the operational amplifier's input configuration.

To ensure that the regulator operates long enough to perform a reliable transfer to nonvolatile memory once a store pulse is sent, you need to use a large filter capacitor. The capacitance depends on the desired trip point, the lowest input voltage to the regulator, and the load. For example, a system with a 10-msec transfer time, a 300-mA load, a 15V trip point, and a minimum regulator input of 7V requires a 375- $\mu$ F capacitor; you can derive the capacitor's value from the equation  $i=Cdv/dt$ .

Once you've chosen a sensing point and a sensing circuit, the next step is to develop a subsystem that uses the power-status signal to generate save and



**Fig 8—This industrial controller's storage architecture** uses a NOVRAAM as both the volatile and nonvolatile system storage elements.



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*Monitoring the ac line in front of the main supply's power transformer gives you the fastest warning of a power loss.*

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restore signals. These signals tell the storage subsystem to transfer data from RAM to nonvolatile memory during power loss and return data to RAM after power has been restored.

The type of system you design will depend largely on the type of nonvolatile storage that you plan to use with that system. For instance, you could use battery-backed RAM, or you could use a NOVRAM like the one used in the industrial controller shown in Fig 8. The industrial-controller design takes advantage of the nonvolatile RAM's ability to transfer data between RAM and EEPROM in a 10-msec single write cycle (see box, "NOVRAM architecture").

The nonvolatile RAM provides both the system storage (RAM portion) and the nonvolatile program storage (EEPROM portion) for power losses. The  $\mu$ P supplies a low-going TTL store signal (100-nsec min duration) to the nonvolatile RAM's store input. During the 10 msec that the nonvolatile RAM requires to complete its data transfer, you must keep the power supply's voltage within the specified operating toler-

ance. Once the system initiates a store cycle, the store cycle can't be terminated.

When the system loses power, the sensor sends a power-failure-detection interrupt to the  $\mu$ P. Once the processor acknowledges the interrupt, it branches to an interrupt routine that writes the current stack pointer and a test byte to the nonvolatile RAM (to signify that a power failure has occurred) and generates a store signal. The power supply holds  $V_{CC}$  above 4.5V for 10 msec after it generates the power-fail signal. During the store operation, the nonvolatile RAM I/O lines maintain high impedance, allowing the  $\mu$ P to complete other tasks. After the system completes a store operation, it must drive the store input high before performing subsequent store operations.

When power is restored, the power-on-reset routine sends a recall signal to the nonvolatile RAM. The routine in the  $\mu$ P then checks the nonvolatile RAM's test byte to see if the previous process had been interrupted by a power failure. If so, the processor saves the current processor state and loads the address

## NOVRAM architecture

A NOVRAM (nonvolatile RAM) is a memory device comprising a static RAM overlaid bit for bit with an EEPROM (electrically erasable programmable ROM). A typical nonvolatile RAM, the Xicor X2212, contains 2k bits organized as a conventional 1k-byte static RAM overlaid with a 1k-byte EEPROM.

The operation of the RAM portion is identical to that of other static RAMs. However, in addition to CS (chip select) and WE (write enable) pins, nonvolatile RAMs also have store and recall pins that control data transfers between the RAM and EEPROM. Because the pulse widths of the control and data inputs are less than 450 nsec, most  $\mu$ P-based systems don't require wait states during the data transfers.

A store operation transfers the entire RAM contents to the EEPROM in a single 10-msec write cycle. After the NOVRAM completes the store operation, the original data will reside in both the RAM and the EEPROM.

The NOVRAM uses a recall operation to transfer data in the EEPROM to the RAM, replacing the RAM's prior content. Instead of moving data on a word-by-word basis, store and recall operations transfer the entire content of the memory simultaneously.

NOVRAMs don't require high-voltage pulses or high-voltage supplies: The devices operate from a single 5V power source and have no battery backup. All inputs and outputs are TTL compatible. The RAM portion's

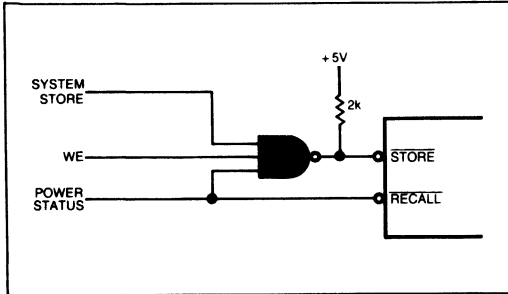
cycle time is 300 nsec, and the common data input/output is 4 bits wide.

### On-chip protection

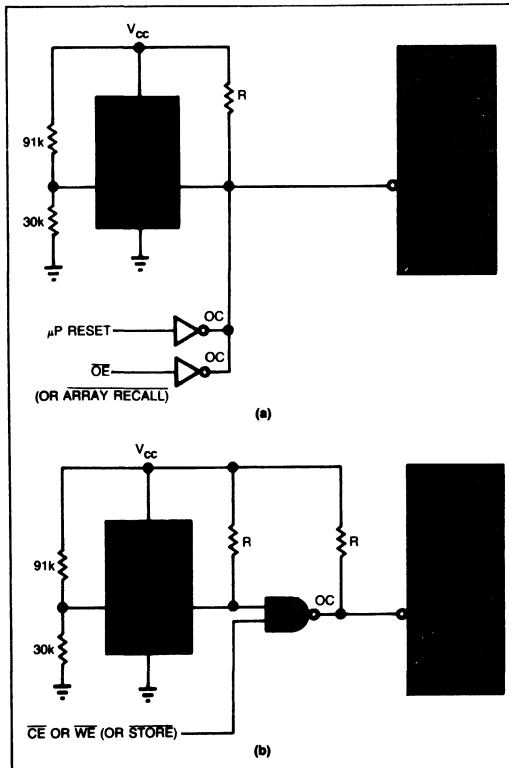
A built-in  $V_{CC}$  sensor protects the NOVRAM from spurious signals often initiated during power-up and power-down. The sensor establishes a threshold supply voltage of 3V. When the supply voltage falls below 3V, store operations to the EEPROM and write operations to the nonvolatile RAM are blocked.

A noise filter built into the EEPROM prevents glitches on the WE line from initiating a write cycle. This filter makes the device ignore pulses of less than 20 nsec so that noise spikes will not be interpreted as write commands.

*An alternative to monitoring ac power at the power transformer is monitoring the unregulated dc power to the regulator.*



**Fig 9**—By NANDing the store, WE, and power-status signals you can protect the NOVRAM from false store commands. In this configuration, all three inputs must be true for a store operation to occur.



**Fig 10**—In a hold-low protection scheme (a), a nonvolatile memory's array-recall pin is pulled to logical zero when the supply voltage falls below 5V. In hold-high protection (b), when power is lost, either the WE or CE pins are held high.

of the saved processor state onto the stack. It then executes a return from interrupt and resumes the previously interrupted process.

### Beware false commands

One of the biggest obstacles you'll face in deriving reliable store and save signals will be to avoid false store commands. Because most  $\mu$ P-based systems don't operate in ideal environments, they often generate false signals during power-ups, power-downs, brown-outs, and power failures. However, these signals are generally nonperiodic in nature, so the system usually recognizes them as by-products of a faulty memory device and disregards them.

Sometimes, however, these signals are periodic and turn out to be unintended write/store commands. After a system reset, for example, the  $\mu$ P's erratic behavior may cause the registers that usually contain the system information to contain false write-store commands instead. Therefore, when the system addresses those registers, those registers issue a false store command.

You can use several system techniques to avoid these errant commands. (For a discussion of on-chip protection features, see box, "NOVRAM architecture.") One technique for protecting the NOVRAM from errant commands takes advantage of the fact that even though most  $\mu$ Ps can issue spurious addresses, they don't usually issue false write commands. By ANDing the system write command with the system store command, you can make sure that the nonvolatile RAM will respond to a store signal only during a write cycle.

Nevertheless, glitches can still appear at the store pin during power up, even if no write command is received at any of the 3-state TTL gate inputs. One way to solve this problem is to use an open-collector NAND gate, one of whose inputs indicates the power supply's status (Fig 9). This method ensures that the store pin's voltage follows the power supply's voltage as the voltage increases.

If you hold one NAND gate's open-collector input low, the output transistor is turned off. Pulling the gate's output voltage to the nonvolatile RAM's power supply through a pullup resistor ensures that the output follows the power supply with no glitches. You can also use the power supply's status signal to hold the recall pin low and the store pin high. This technique gives you better control over the nonvolatile RAM because it uses two conditions to prevent an inadvertent store operation. All you need to do is to connect the status signal directly to the recall pin.

Two additional methods of preventing unintentional nonvolatile data changes during power transitions are hold-low and hold-high protection. When you use hold-low protection (**Fig 10a**), the array recall pin is pulled to logical zero whenever the supply voltage falls below the 5V-10% threshold. The Intersil ICL8211, an 8-pin miniature DIP, provides the voltage reference and gives a zero output whenever the supply falls below its threshold. When the sensed voltage rises above the selected threshold, the device produces a logical one.

(**Fig 10b**) gives an example of hold-high protection. ICL8211 keeps the voltage on the nonvolatile RAM's store pin (or the  $\overline{WE}$  or  $\overline{CE}$  pins) near the power supply's voltage level. This blocks the low pin voltage that's necessary for a write or store operation.

The power-supply output that ICL8211 senses is a sawtooth waveform. ICL8211's output is a logical 1 while the supply output is above 4.5 volts. Below 3V, the nonvolatile RAM's internal protection circuitry prevents inadvertent writes or stores. In the critical unprotected range between 3 and 4.5V, ICL8211 provides a zero output to prevent writes or stores.

An alternative to ICL8211 in these applications is the SGS L487. The SGS L487 is a 500-mA precision 5V voltage regulator that includes an open-collector power-on/power-off reset output pin that protects nonvolatile memory the same way the ICL8211 does.

Other schemes that protect systems from inadvertent store operations employ jumpers, cables, and switches. You transmit the store signal through a jumper or switch that you hold open unless you're changing data in the EEPROM. During normal operation, the only component attached to the store pin is a resistor to the power supply.

**EDN**

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### Author's biography

*Christopher Lopes is an applications engineer at Xicor (Milpitas, CA), where his duties include system-level evaluation, product-application development, and customer technical assistance. A member of the IEEE, Chris holds a BS in electrical and electronic engineering from California State University at Sacramento and is currently enrolled in the MBA program at the University of Santa Clara. He enjoys windsurfing, skiing, and tennis.*

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# Electronics®

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## **THICK OXIDE BEATS THIN FILM IN BUILDING BIG EEPROMS**

## INSIDE TECHNOLOGY

THICK OXIDE BEATS THIN FILM  
IN BUILDING BIG EEPROMS

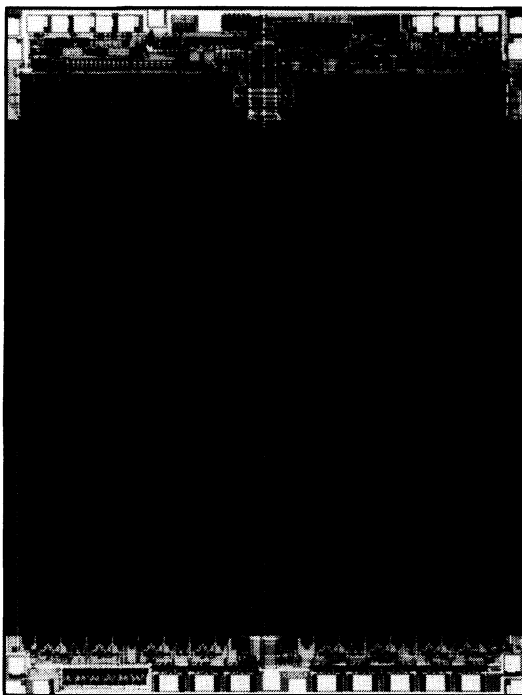
## XICOR USES IT TO SOLVE 3-D SCALING PROBLEMS IN 256-K CHIPS

**B**y abandoning the conventional thin-film route to fabricating high-density electrically erasable programmable read-only memories, Xicor Inc. may have overcome the problems that have kept the parts from climbing above the 64-K density level. The Milpitas, Calif., company employed a conservative 2- $\mu$ m process and standard off-the-shelf 5 $\times$  stepper lithographic equipment to build a 256-K EEPROM.

The key to doing this was the use of a thick oxide and a unique triple-polysilicon floating-gate cell, says William Owen, Xicor's vice president of research and development. The process is inherently more reliable and easier to scale to sub-micron dimensions, he claims, although it was more difficult for the Xicor engineers to master. They were less familiar with it than with the thin-oxide double-poly technology derived from EPROM manufacture.

Conventionally used thin-oxide floating gates are relatively easy to manufacture, but cannot be scaled down easily without introducing significant reliability problems. This unpleasant consequence of the laws of physics is one reason many EEPROM houses are having difficulty moving to densities beyond 64-K to the 256-K level. To do so requires pushing minimum line widths on the oxides down to 1  $\mu$ m using advanced photolithography.

"The problem with scaling EEPROMs lies in the fact that it is necessary to scale in three dimensions—in the vertical as well as horizontal directions," says Owen. "To achieve 256-K densities, not only must thin-oxide EEPROMs be scaled from 2 or 3  $\mu$ m down to 1 to 1.5  $\mu$ m in the horizontal direction, but from 90 to 100 Å down to about 70 to 80 Å in the vertical direction." To achieve similar densities in its 256-K EEPROM, Xicor found it necessary only to scale down from 3 to 2  $\mu$ m



**1. SMALL DIE.** Equivalent in size to many thin-oxide 64-K parts, Xicor's 256-K EEPROM die measures about 64,000 mils<sup>2</sup>.

horizontally and from 600 to 800 Å down to 400 Å vertically.

The thick oxide enabled Xicor's designers to form a basic EEPROM cell with a triple-poly structure that puts the programming portion atop the erase mechanism. This resulted in horizontal cell dimensions smaller than the thin-oxide structure.

Another factor in the smaller size was the use of a proprietary textured thick-oxide surface on the programming elements. The textured surface's electrical potential per unit area is greater than conventionally used smooth surfaces, producing cells that are inherently smaller than comparable thin-oxide cells, but with the same effect. The oxide can be shaved off without affecting cell reliability, making vertical scaling relatively easy.

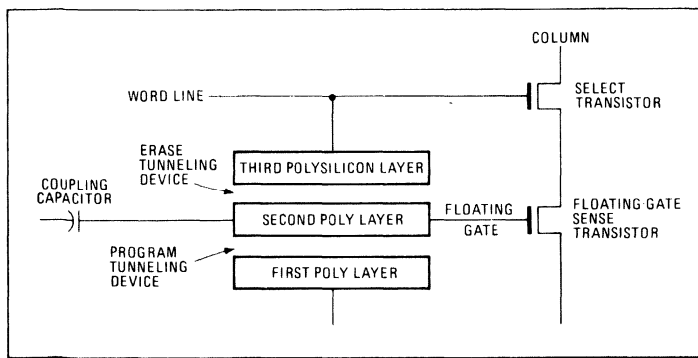
The first 256-K EEPROM fabricated with the 2- $\mu$ m process is the 32-K-by-8-bit n-MOS X28256. It features a chip area of about 64,000 mils<sup>2</sup> (Fig. 1), equal in size to many thin-oxide 64-K parts fabricated using 1.5- $\mu$ m design rules, and half the size of thin-oxide 256-K EE-

PROMs designed with 1- to 1.2- $\mu$ m geometries. Soon to follow will be a CMOS version, the X28C256. Both parts feature 150-ns access times and support 64-byte page-write operations. A write cycle takes 31  $\mu$ s per byte, enabling the entire memory to be written in less than 1 second.

In Xicor's triple-poly cell (Fig. 2), the floating gate sits between the upper and lower poly layers, forming the thick-oxide tunnel structures for erasure and programming. Compared with the 80- to 120- $\mu$ m<sup>2</sup> cells of conventional 1- $\mu$ m thin-oxide designs, the electrically erasable cell in Xicor's 2- $\mu$ m 256-K parts measure only 68  $\mu$ m<sup>2</sup>.

The programming tunnel mechanism occurs between the first and second floating-gate poly layers; the erase tunneling action occurs between the second and third (Fig. 3, left). As in the thin-oxide approach, a selection transistor isolates the selected cell on a column while a capacitor develops, through capacitive coupling, enough voltage across a tunneling device to make electrons tunnel on and off the floating gate. This voltage is sensed by a MOS transistor, whose gate is formed by the second poly layer.

*TECHNOLOGY TO WATCH is a regular feature of Electronics that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*



**2. TRIPLE POLY.** Key to the small die area is a unique triple-poly floating-gate cell. The gate, between the upper and lower poly layers, performs erasure and programming.

Because capacitance increases linearly as oxide thickness decreases, tunnel devices made with very thin oxides—80 to 100 Å thick—rate 5 to 10 times higher than tunnel devices made with 500- to 800-Å-thick oxides. Consequently, cells using thin oxide have to push photolithography requirements to the limit of available equipment and processes in order to make the thin-oxide tunneling devices as small as possible. The coupling capacitor, which must be made from a thicker, nontunneling oxide, ends up relatively large to obtain efficient coupling.

In contrast, thick-oxide tunnel devices inherently have very low capacitance. Therefore they can be made with reasonable feature sizes and still produce a small cell with good coupling-capacitor efficiency. Since the feature sizes used in the tunnel devices are compatible with the lithography requirements of the rest of the cell, they can be readily scaled down as advances in lithography technologies become available for manufacturing.

What makes this structure work is its surface, which Xicor describes as textured with hillocks (Fig. 3, right). Also called asperities, these odd-looking features were at first considered an undesirable side effect of MOS processing, and occur because oxidation progresses faster along some crystal directions than others. Because crystal orientation is random in deposited poly, there are points on the surface of an integrated circuit where oxide growth is enforced. The temperature of the oxide controls the size and shape of the hillocks.

Through the use of carefully designed and controlled fabri-

cation techniques, Xicor exploits this phenomenon to build EEPROM transistors using thicker silicon dioxide layers that can still discharge the floating gate. Because the oxidation is a well controlled step, the properties of the emitters are exceptionally regular. They are shaped so that the electric field increases at the crest of the hills, substantially enhancing the emission of electrons.

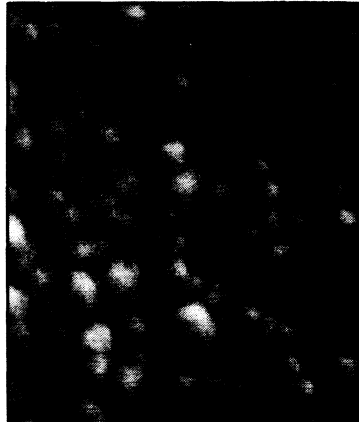
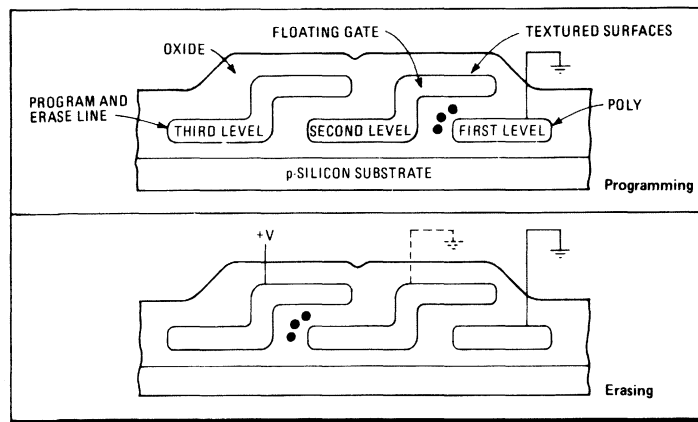
The poly electrodes are separated by oxide layers about 500 to 800 Å thick. Without the hillocks, Xicor says, 100 V would need to be applied to produce effective tunnel current. With the textured surfaces, the voltage required for tunneling is only 10 to 20 V, low enough to be generated easily on chip with an internal charge-pump circuit.

The coupling capacitor's size also contributes to the smaller cell area. To induce tunneling, the floating-gate voltage is raised or lowered through capacitive coupling to a bias-voltage supply. To avoid excessively high bias voltages, efficient coupling to the floating gate must be achieved by making the coupling capacitance much higher than all other floating-gate capacitances combined. These other capacitances include that of the MOS sense transistor, and especially that of the tunnel devices.

To electrically program a cell, electrons must tunnel onto the floating gate. In Xicor's triple-poly enhanced-emission cell, this is accomplished by applying a bias voltage to the coupling capacitor to capacitively pull the floating gate high and develop a voltage across the program tunneling device. When this voltage reaches the tunnel voltage, electrons tunnel from the first poly level's surface through the programming device to the second-level floating gate. When the applied voltages are brought back to normal reading levels, the programmed floating gate carries a negative voltage because of the extra electrons on it. When read, the MOS floating-gate sense transistor is turned off by the negative voltage and a 0 is produced at the EEPROM's output.

To electrically erase a cell, electrons must tunnel off the floating gate. In Xicor's triple-poly cell, this is done by capacitively coupling the second poly level's floating gate low while the third poly level's word line, which forms the other end of the erase tunneling device, is brought high. When the voltage across the erase tunneling device reaches the tunnel voltage,

**3. TUNNELS AND TEXTURE.** In Xicor's cell design, programming by tunneling action occurs between layers 1 and 2 and erasure between layers 2 and 3 (left). The thick-oxide cell approach uses a "textured" floating gate surface to enhance electron emission.



electrons tunnel from the second poly floating gate to the third poly word line. When the applied voltages are brought back to normal reading levels, this erased floating gate has a net positive voltage because of the lack of electrons on its surface. When read, the MOS floating-gate sense transistor is turned on by this positive voltage and a 1 is produced at the EEPROM's output.

Other advantages of the thick-oxide approach, says Owen, include improved data retention and endurance, or the number of data changes a nonvolatile memory can sustain before the first bit fails. Because the floating gates in the Xicor design are completely surrounded by thick thermal oxides, similar to an EPROM, data retention is excellent even at very high temperatures. "In fact, the only way retention can be measured on the thick-oxide devices is by subjecting them to temperatures over 300°C for several weeks," Owen says. "If these measurements are extrapolated, the typical retention for a Xicor EEPROM is more than 2 million years at 125°C." But for the record, the company is much more conservative, guaranteeing data retention of only 100 years at 125°C.

The data-retention advantages of the textured thick-oxide approach are retained—or even improved—as devices are scaled, he says. This is due to the fact that lower programming voltages are needed in order to scale the memory properly, so isolation widths and device channel lengths can be reduced in both the memory array and in the peripheral circuitry. However, for a typical part, which stores data in 3 ms and must retain it for 10 years, the tunneling current under storage and reading conditions must be reduced by at least  $10^{11}$  than under programming conditions because the retention time is  $10^{11}$  times longer than the storage time.

For planar nontextured tunneling structures, this is a difficult design constraint because the slope of the current voltage curve—that is, the relationship between the current and voltage of the tunneling device—is fixed. This means that the maximum allowable read voltage drops with the programming voltage on a volt-for-volt basis, not proportionately.

On the other hand, a textured-surface tunneling structure has a much steeper current-voltage curve; that is, for each increment of change in one voltage, there is an amplified increment of change in the other. In addition, the curve is not fixed, which means the relationship between the current and voltage can be tailored to yield steeper curves if necessary. This means that for a given

maximum read voltage, a textured surface requires a lower programming voltage than a planar thin-oxide structure, leading to better scaling.

With regard to endurance, recent data on Xicor's EEPROMs indicates an expected failure-in-time rate of 0.015% per 1,000 hours, or 150 FIT, in systems requiring 10,000 data changes per byte over a 10-year period, says Owen. "Thus for many applications, the endurance-related fallout is actually similar to or lower than other semiconductor-related failure rates."

To achieve 1-Mb densities, Owen believes that although it will require moving to 1- $\mu$ m geometries horizontally, only a few "tens of angstroms" reduction will be necessary in the vertical direction. "In thin-oxide EEPROMs, this is a reduction of 10% to 15% down to the operational limits of the floating-gate mechanism," he says. By comparison, Xicor's thick-oxide approach requires a reduction on the order of a few percentage points. "Moreover, the scaling is well within the limits of the Xicor cell design," he says. "As a matter of fact, we think we can continue to scale for several generations before we run into any of the problems our competitors are running into with thin-oxide EEPROMs." □

## XICOR: FROM LONG SHOT TO LEADER

**Life is sweet** these days for Raphael Klein, Julius Blank, William Owen III, and Wallace E. Tchon, who all helped found Xicor Inc. in 1978. But they can recall the time when the Milpitas, Calif., company's chance of survival was considered a long shot.

"The problem was that few in the industry thought we had a technological edge except us," says Owen, vice president of research and development. "There was Intel Corp., with its thin-oxide approach to fabricating electrically erasable programmable read-only memories, and there was Xicor, with the thick-oxide approach. Everybody seemed to be going the thin-oxide route." All that is changing now.

First of all, it is becoming clear that the company is at least a generation ahead of its competition with its thick-oxide approach. While everyone else is pushing to 1- $\mu$ m geometries to achieve 256-K products, Xicor is coasting along with a relatively conservative 2  $\mu$ m to achieve the same density.

Second, thin-oxide advocate Intel has entered into a long-term agreement with Xicor for joint development of advanced EEPROMs. The deal also calls for mutual second-sourcing of EEPROMs and related products. As part of the agreement with Intel, Xicor has received \$6.5 million; and may receive an additional



**COMING UP ROSES.** The commitment to thick-oxide EEPROMs finally starts paying off for Xicor Inc.'s Tchon (left), Blank, Klein, and Owen.

\$500,000 as well as a \$10 million lease guarantee.

Third, the company continues to dominate the market it created, 5-V-only EEPROMs. Sales have grown from \$2.8 million in 1982 to \$39 million in 1984. Estimates for 1986 range as high as \$55 million.

Finally, Xicor had profitable operations during all four quarters of 1984 plus Q1 of 1985. It owns about 50% of the market for 5-V EEPROMs and Novrams, static random-access memories backed by nonvolatile EEPROM cells.

Klein, now chief financial officer and chairman of the board, is a graduate physicist from the Israeli Institute of Technology and performed in a variety of technical management positions at Fairchild, Intel, Monolithic Memories, and National Semiconductor before starting Xicor as its first president. He

holds two patents.

Owen, who joined the company to direct its development of advanced memories in 1978, holds an MS in electrical engineering and previously worked at Intel. As a process engineer and senior design manager, he was involved in the development and design of Intel's HMOS memory products.

Strategic planning vice president Tchon, who joined Xicor to aid in the development of its initial memories, is now principally involved in business planning, patent activity, and investor relations. With an MS in physics, Tchon holds 10 patents. Before Xicor, he held engineering positions at Honeywell Information Systems and Intel.

Blank, one of the original eight founders of Fairchild Semiconductor Corp. in 1957, has been a member of the Xicor board of directors since its founding.

# MACHINE DESIGN

A PENTON/IPC PUBLICATION

## TECH BRIEFS

### SOLID-STATE POTENTIOMETER

**RICHARD PALM**  
Applications Engineer  
Xicor Inc.  
Milpitas, CA

**P**otentiometers play a vital role in circuit design, yet they have a

number of problems. Their settings can change when exposed to vibration. They are difficult to use with automatic insertion and soldering equipment. And trimming must be done by hand.

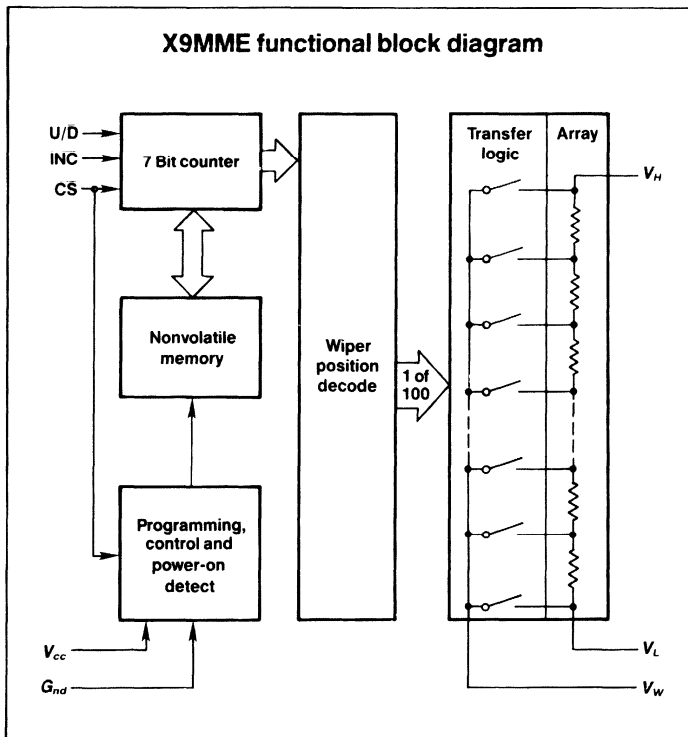
A solid state potentiometer solves these problems. Packaged in an eight-pin minidip, an electrically

erasable ( $E^2$ ) device called the X9MME digitally controls resistance trimming. The device has three-wire TTL control and operates from a standard 5-V power supply. Packaged in the dip is a 99-resistor array. Tap points are between the resistive elements and at the ends of the array. A tap point can be connected to the wiper output  $V_w$ .

Because the resistive elements are all equal, each has  $1/99$  the total resistance of the array. In a voltage divider application, moving the wiper up or down the array produces a linear output on  $V_w$ , with a resolution of 1%.

The tap point on the array is selected with three TTL inputs on the digital portion of the device. These inputs control a seven-bit up/down counter. To move the wiper tap point, the "chip select" line must be activated ( $CS = \text{LOW}$ ), the wiper direction selected ( $U/D, \text{up} = \text{HIGH}, \text{down} = \text{LOW}$ ), and a clock pulse provided to the INC input. Counter output is decoded to select one of 100 tap points.

Mechanical potentiometers essentially have a nonvolatile memory; resistance does not change until the wiper is moved. In the X9MME, seven bits of nonvolatile  $E^2$  memory retain the resistance value. When the device is deselected after a wiper position change, the counter output is stored in memory. If power is re-





## TECH BRIEFS

moved and subsequently restored, the nonvolatile memory contents are transferred to the counter and the last stored wiper position decoded. Wiper position retention is 100 years.

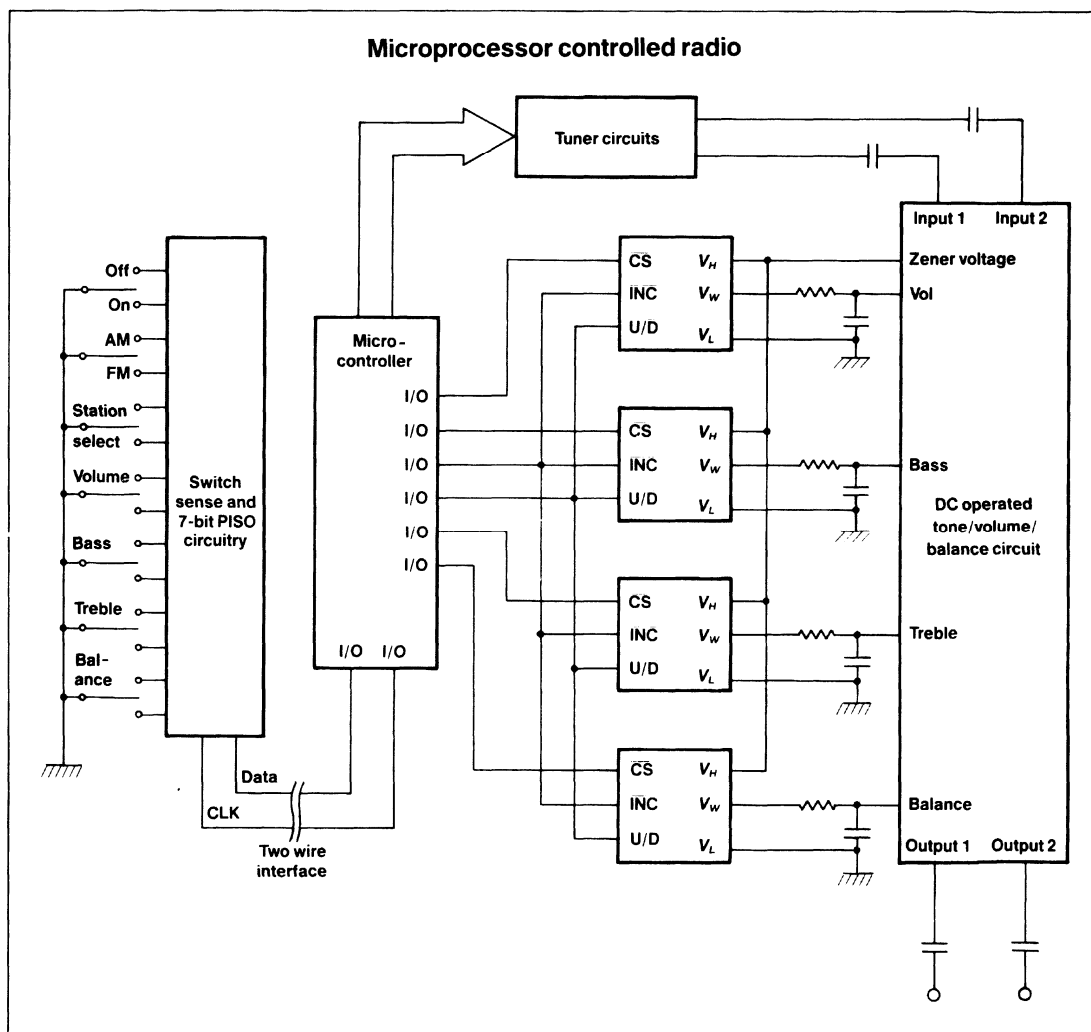
The manufacturing and test cost of equipment produced in high volumes can be reduced when solid state pots are used. Because automatic insertion equipment can be used, the device is soldered and cleaned just like other electronic components. This eliminates special handling and cleaning steps. During board testing, automatic

test equipment (ATE) can check the device and set wiper position. Hand operations are reduced, and the cost of supplemental test equipment is eliminated.

Operator convenience can also be of prime concern in circuit design. If the equipment operator or field technician must access the pot to make adjustments, the design process is complicated. The X9MME, in contrast, can be placed anywhere in the circuit and still be controlled through keyboards or a microprocessor.

As an example of how circuitry

can be simplified, consider a hypothetical car radio system. Control might be by miniature rocker switches mounted on the steering wheel. The switch sense and 7-bit parallel-in-serial-out circuit could be implemented in either discrete TTL circuits or as a standard cell or programmable logic device. The microcontroller interface would be two wires, one for the shift clock and another for the interrupt and data transfer. The microcontroller actuates off/on, AM/FM selection, and tuning. Six port lines control volume, bass, treble and balance. ■





## X88C64:

### Improving Microcontroller Performance with a New E<sup>2</sup>PROM

Richard Palm, Strategic Marketing Manager, Xicor, Inc.

#### INTRODUCTION

Today, the single-chip microcontroller is perhaps one of the most important building blocks in modern systems design, integrating a powerful microprocessor, RAM, program memory and peripherals all on a single-chip. Applications range from stand-alone embedded controllers, such as in appliances, to elements of highly specialized distributed processing systems, such as peripheral controllers.

With the integration of more hardware onto the chip, the complexity of design has shifted from hardware to software. Single-chip microcontrollers which control such systems as automotive engine controllers are based on complex real-time control algorithms. This increase in the complexity of the software has emphasized a major applications problem with single-chip microcontrollers: that is, the software in a single-chip microcontroller is extremely "firm". Once the internal ROM of the microcontroller is masked, the only way to change the software is to make a new mask and physically change the microcontroller chip. The need to alter software in embedded controller systems is driven by several requirements. Some of these are listed below:

1. Software revision to correct bugs.
2. Software revision to improve algorithm.
3. Initial or modified system configuration.
4. Self-modifying code to adapt to systems operating environment.

The "firmness" of the single-chip microcontrollers internal Program ROM is compounded by the long manufacturing cycle of a mask-programmed microcontroller. The time required to make a software change to a running series may be as long as 24 weeks, since it requires code submittal, verification, mask fabrication, wafer production, assembly and test. Couple this with

the fact that during this conversion time large quantities of the old version will be fabricated as the work in process is moved out of the line. One can easily see that the software internal to the microcontroller is very firm indeed.

#### THE PROBLEM OF REPROGRAMMABILITY AND SINGLE CHIP

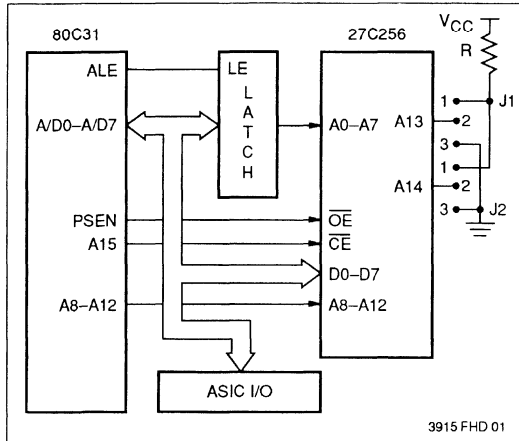
Microcontrollers In a effort to "soften" the internal program memory of the single-chip microcontroller, many manufacturers offer versions of their devices which utilize EPROM instead of mask programmable ROM for the program storage. This enables the customer to program the chip just prior to its mounting on the PC board. This certainly solves many of the above mentioned problems, or at least makes them more manageable. Unfortunately, the EPROM versions of the single-chip microcontrollers are more expensive. They also do not lend themselves to in-circuit reprogramming which is desirable for many applications such as self-alterable code and service reprogramming.

Many designers have developed ingenious methods to overcome these problems. A common technique is to use an external EPROM to store the program code. This provides many of the benefits of the EPROM version of the single-chip microcontroller without the associated cost.

Many single-chip microcontrollers are capable of operating in a mode in which two of the I/O ports are used as an Address and Data multiplexed bus to access external memory. In this case the UVEPROM can be removed, erased and reprogrammed; but this compromises the integrity of the enclosure and requires socketing the EPROM rather than soldering in the component. Figure 1 shows such a typical application, where an 80C31 (ROMless version of the 80C51) is used with a 27C256 EPROM.

## Improving Microcontroller Performance with a New E<sup>2</sup>PROM

**Figure 1. Typical 80C31/UVEPROM Interface Circuit**

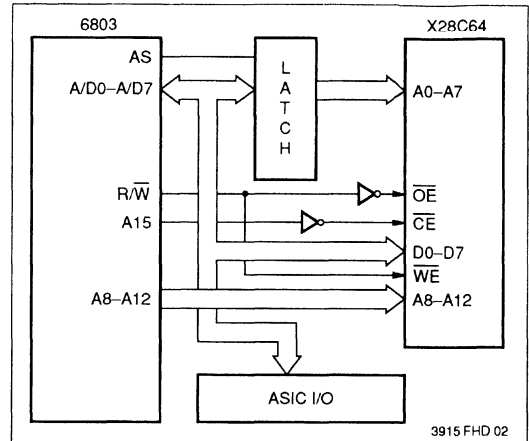


An extension of this approach allows in-situ reprogramming of the program memory; a 5-Volt E<sup>2</sup>PROM is used instead of the EPROM. Since the software can now be altered in a byte-by-byte approach, new software can be downloaded to the microcontroller through its serial interface. For this reason, an 8K X 8 E<sup>2</sup>PROM is sufficient for the program storage, since only one copy of the program needs to be resident at one time. Figure 2 shows a typical 6803 implementation of such a system. Since the 6803 and other members of the 68XX family are based on a Von Neumann architecture, it is possible to write to program memory, which will allow the system to update any bytes desired. A single R/W signal is decoded to provide the WE and OE signals for the X28C64. Since the X28C64 is a second generation E<sup>2</sup>PROM which features Software Data Protection, no hardware write protection is needed to prevent inadvertent write cycles from occurring during Power-up and Power-down.

While this solution provides a high level of in-situ reprogrammability, there are a few disadvantages to this approach. During the relatively long internal write cycle time of the E<sup>2</sup>PROM instructions cannot be read from the same memory device. Therefore, care must be taken when the processor executes a write to the same device from which it is currently executing code.

A technique which can be used with the Von Neumann type microcontrollers is to transfer the write and wait routine, usually only a few bytes long, into the internal RAM of the microcontroller.

**Figure 2. Possible 6803 and Conventional E<sup>2</sup>PROM Circuit**



With the Harvard type architecture this will not work. In this case, or if the internal RAM cannot be spared, a secondary program memory chip needs to be added to the system.

Given all of the above problems and complexity, it can easily be seen that an ideal solution is a single-chip microcontroller with about 8K Bytes of E<sup>2</sup>PROM on board. Attempts at providing on-board E<sup>2</sup>PROM have been made, but adding the complexity of E<sup>2</sup>PROM processing to the microcontroller chip has proven to be uneconomical. This is the reason for the development of the X88C64.

### X88C64: An E<sup>2</sup>PROM for Microcontrollers

The X88C64 is an 8K Byte E<sup>2</sup>PROM which is designed specifically for use as a data and for program memory for single chip microcontrollers. In addition to the normal industry standard features of today's third generation E<sup>2</sup>PROMS, such as 5-volt latched write operation, page mode write operation, toggle bit write completion notification and Software Data Protection, the device incorporates several useful features tailored for the single-chip microcontroller.

The first of these features is the bus interface. Rather than the normal separate address and data bus, the X88C64 features a multiplexed address and data bus designed to interface directly to the microcontroller without a latch for addresses or additional decoding logic.

# Improving Microcontroller Performance with a New E<sup>2</sup>PROM

The X88C64 also features an advanced write lock-out feature, called Block Protect, an extension of the industry standard software data protection. Block Protect provides programmable write protection for individual 1K blocks of the array.

Lastly, and perhaps most significantly, is the dual plane architecture, which allows the device to be read during the write cycle. The internal E2PROM array of the chip is divided into two 4K Byte blocks. A12 selects which of the two arrays is being accessed. The dual plane architecture allows write operations to occur within one 4K Block, while simultaneously reading from the other 4K Block. As long as write operations occur in only one plane the other plane is free for program execution without interruption. By simply duplicating the write instruction in each half of the memory, it is possible to write to any location in the X88C64. An example of this will be shown later. Figure 3 shows the block diagram for the X88C64.

## X88C64 and The 8051 family

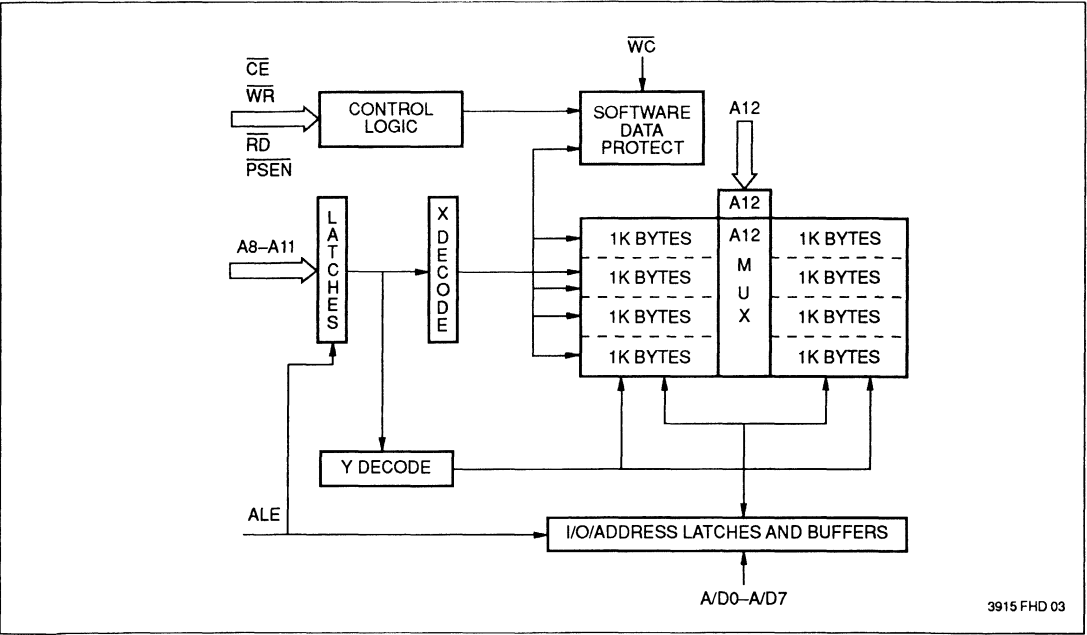
The X88C64 is configured to interface with virtually all of the 8051 family including the 8031 and 8048, and various other derivatives. Figure 4 shows how the

X88C64 and 80C31 are connected. In this case, the nomenclature of the pinout of the X88C64 is exactly the same as the names referenced by the 80C31, and understanding the interconnection scheme is quite straightforward. The 8051 family is based upon a Harvard architecture where the data memory and the program memory are separate memory spaces, accessed by separate control signals.

Program memory can only be read with a  $\overline{\text{PSEN}}$  signal while Data memory can be read or written using the  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  signals. Normally Program memory cannot be written. However, in order to update the program code the X88C64 allows the user to write any byte in the memory and also read any byte as either program instruction or data.

The  $\overline{\text{PSEN}}$  and  $\overline{\text{RD}}$  signals are internally gated together in the X88C64 such that when either one of the two is low, the device will output program code or data. Thus, the separate memory spaces are combined. There are now 8K Bytes of program storage as well as 8K Bytes of data storage which are both the same data. In essence, the 8051's Harvard architecture becomes a pseudo Von Neumann machine for software purposes.

Figure 3. X88C64 Functional Block Diagram



# Improving Microcontroller Performance with a New E<sup>2</sup>PROM

## X88C64 and the X68XX Family

Figure 5 shows the interconnection scheme between the X88C64 and a member of the 68XX family, the 68HC11. Since the 68HC11 use a Von Neumann architecture, the  $\overline{\text{PSEN}}$  signal is not needed and is tied to  $\text{Vcc}$ . Tying  $\overline{\text{PSEN}}$  to  $\text{Vcc}$  alters the manner in which the control inputs are interpreted, so that the device can easily be used in the 68XX type of systems.  $\overline{\text{RD}}$  is tied to the  $\overline{\text{E}}$  output of the 68HC11 and  $\overline{\text{WR}}$  is connected to the R/W output.  $\overline{\text{CE}}$  is tied to  $\text{Vss}$ , since the 68HC11 requires that the program memory reside at the top of the memory map. If power consumption is an issue in the system, an extra inverter can be added to provide a decoded Chip Enable, which places the X88C64 into low power Standby mode when it is not selected.

The 68HC11 processor uses a Von Neumann architecture where the program and data memory share the same memory space; therefore, updating code is the same as writing data in the X88C64.

## Software Data Protection

The X88C64 features industry standard software data protection (SDP). This is enabled via a three byte command sequence. Once enabled, the X88C64 is protected from inadvertent write operations during power-up and power-down conditions.

Although SDP protects data integrity during these unknown bus state conditions, it still allows the system easy access to memory for data changes. To write to the device in the protected state, a three byte command sequence is written to the device followed by the byte or page data to be written. At the end of the write cycle the X88C64 is automatically returned to the protected state.

## Write Lock Out Block Protect

Block Protect provides a second level of write protection for the end user. Block Protect allows the user to individually protect 1K x 8 segments of the array by

Figure 4. 80C31/X88C64 Interface

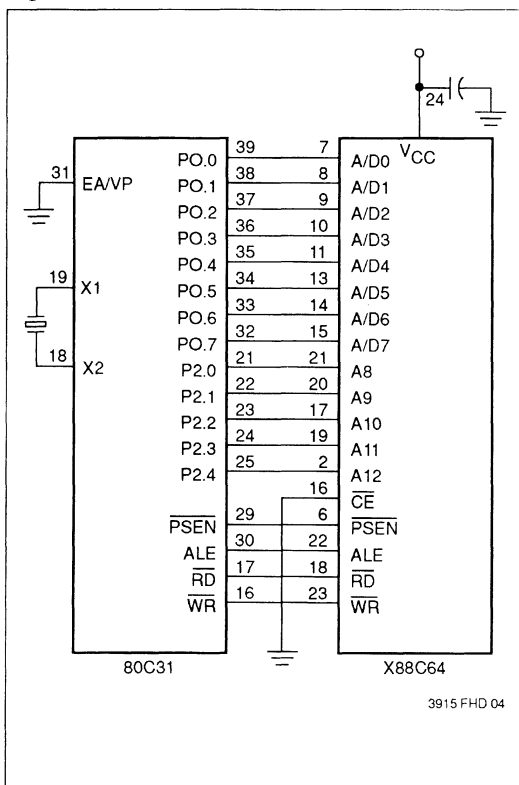
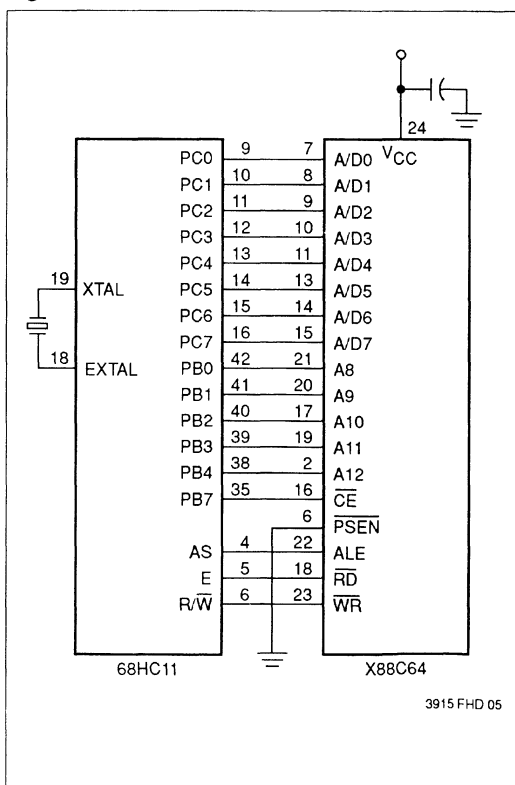


Figure 5. 68HC11/X88C64 Interface



## Improving Microcontroller Performance with a New E<sup>2</sup>PROM

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writing to the block protect register. Access to the register is gained through an extension of the SDP command sequence. Once a block has been protected all attempts to write to that block will be locked out until that block's protection is specifically removed by rewriting the block protect register.

The significance of this feature varies from application to application. In many applications, it is desirable to have some software and/or data which can be altered by the applications software during normal usage, while other sections of the program and/or data can only be changed at service intervals. By using the Block Protect, the X88C64 can initially be configured to allow write operations only in non-protected sections of the chip. When the system is then serviced or re-configured, the proper sequence of byte locations and addresses could be passed to the microcontroller via a serial interface. This sequence will enable the write operation to the protected blocks, perform the write operations desired, and then return these blocks to the protected state. Since the sequence of write operations needed to perform this operation does not reside in the program memory of the microcontroller, there is no possibility of the device inadvertently executing this code.

An additional level of data protection is provided by the  $\overline{WC}$  or write control input. Since the X88C64 is completely protected against any inadvertent write cycles during power-up and power-down by both the Software Data Protection and Block Protect features, the only remaining possibility of data corruption is in the event that the power fails in the middle of the byte write load cycle. At this point in the write operation, the address has already been latched into the device. Even if data is being output onto the A/D0-A/D7 outputs of the microcontroller, a power-failure may cause the microcontroller to go into Reset mode and all of the outputs will be driven high. This low-to-high edge on the  $\overline{WR}$  input will be taken as the end of the byte write load cycle, and thus FF will be written into the location selected for the interrupted write operation, rather than the desired data.

The Write Control input protects against this situation. The write control input can terminate a page or byte load operation at any time during the page load cycle time. External circuitry (inverter in the reset line) can hold this signal low except in the event of a power-fail condition. In this case, the  $\overline{WC}$  signal goes high when system reset goes low, which terminates any page load operation in progress and prevent writing of invalid data.

### APPLICATIONS

The X88C64 provides a single memory solution for microcontroller designs requiring varying degrees of system reprogrammability. This reprogrammability can occur during system operation as well as during normal system service or system reconfiguration. The flexibility of the device allows it to be used to store both reprogrammable software as well as set-up and configuration data. The architecture of the X88C64 provides the most cost-effective solution to nonvolatile reprogrammable program and/or data storage available. Systems can be reprogrammed or reconfigured remotely through the microcontroller's serial interface. In some cases this can be done via phone link, or service module. Algorithms can easily be changed to meet the changing environment in which the system operates. Diagnostic data can be stored in a section of the X88C64 to provide invaluable assistance in error identification and tracking.

The added capabilities of Block Protect allows several levels of reprogrammability to be assigned to various sections of the device. In systems such as digital televisions, the initial screen parameters can be stored in a protected area, which can then only be altered during service. In automotive engine controllers, certain preset emission standard data can be stored in a protected area, while the rest of the data and program can be altered as the operating environment of the engine changes, due to external conditions, age and wear. Security codes which allow special operations to be performed can be stored in a protected area, while other data and programs can be changed freely. In cellular telephones, preset frequencies and security data can be stored in the protected area while phone numbers and other user defined functions can change freely.

### CONCLUSION

The X88C64 is the perfect complement to any single-chip microcontroller design. The device provides 8K Bytes of data and/or program storage with an interface which eliminates the need for any support logic. The advanced features of the device such as the dual plane architecture and Block Protect provide advanced capabilities not previously available and opens the door to alterable nonvolatile program and data store in microcontroller systems.

## **Improving Microcontroller Performance with a New E<sup>2</sup>PROM**

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NOTES



## Recent Trends in Embedded Control Memory

Clifford Zitlaw, Application Manager, Xicor, Inc.

### INTRODUCTION

The proliferation of embedded controllers into new environments has led to a second generation of "application specific" memories. Memory manufacturers have developed devices with architectural and operational characteristics that address specific design requirements. The new devices complement or even replace on-board ROM, RAM, or EEPROM memories found on most microcontrollers.

This paper will briefly describe several memory families suited to specific embedded control environments and then focus on a "controller-specific" EEPROM device recently released by Xicor Inc.

### MEMORY OVERVIEW

**SERIAL MEMORIES:** The majority of controllers sold for embedded applications are ROM based and offer different densities of on-board RAM and EEPROM for data storage. Off-board serial memories often provide a more cost effective solution than designing in a controller with extended on-board data memory. Serial memories based on EEPROM, Ferroelectric, SRAM, or DRAM technology are now available with features tailored to specific environments.

Most serial devices provide an interface to one of the standardized serial busses offered on many microcontrollers. These standard busses provide an effective means of moving data back and forth between the microcontroller and a serial memory. Three of the more popular busses include the MICROWIRE™ bus (National Semiconductor), SPI bus (Motorola), and the IIC bus (Philips).

If a standardized bus is not available, general purpose I/O port lines can be used to communicate with a serial device. This implementation uses software to emulate the bus protocol. While there is added software overhead, this is the only method possible when a controller without a standardized serial port is used.

Portable applications are demanding that components consume less current and operate at lower voltages. Therefore, many manufacturers are offering devices that operate at supply levels of 3.0 volts or below and consume less than 1mA when in active mode.

**EMERGING TECHNOLOGIES:** Two technologies that have recently been introduced may have a place embedded control environments.

Ferroelectrics offer many of the nonvolatile storage features provided by EEPROMs and battery backed SRAMs. While process development is still underway, Ferroelectrics could eventually become a significant technology for non-volatile memory devices.

A new twist on EEPROM technology has led to the development of a device capable of storing analog signals. Each bit in this EEPROM stores an analog level instead of the 1 or 0 stored in traditional memory devices. This new family of devices is well suited to applications where analog data logging is to be performed.

**HIGH SPEED MEMORIES:** High performance products, such as laser printers, are using controllers with processing capabilities unheard of a few years ago. These high performance applications require much more sophisticated memories than those used by traditional microcontrollers. Parallel EPROM devices with cache-like features have emerged to keep up with the requirements of newer high-performance controllers.

**DATA AND PROGRAM STORAGE:** ROM-less controllers operate by accessing off-chip program memory stored in parallel memory devices. External memory requirements include program and often data storage. Recently introduced EEPROM based products address the needs of both program and data storage in low-end controller environments. The X88C64 from Xicor Inc. provides EEPROM program and data storage for microcontrollers in a single package.

### EXTERNAL MEMORY FOR MICROCONTROLLERS

The time and expense required to implement program changes in ROM based microcontrollers often makes external program memory an attractive alternative. EPROM based controllers are available at a substantial price increase but they do not address applications where additional data storage is required. In situations where on-board data memory is inadequate an interface to external memory becomes a design requirement. Therefore, most 8 bit microcontrollers offer the ability to



# Recent Trends in Embedded Control Memory

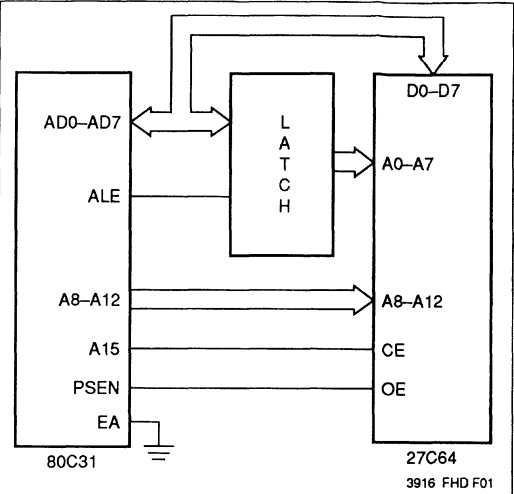
access off-board memory for program and data storage. An external memory interface is implemented by redefining I/O ports as the address, data, and control busses.

Microcontrollers with the ability to access external memory usually have a multiplexed address and data bus to reduce the number of pins required for the external interface. Figure 1 shows how an EPROM can be interfaced to a microcontroller to increase program storage. The implementation shows effectively increases the program and permanent data storage of the circuit but does not change the amount of programmable data memory.

To increase the amount of alterable data storage a second memory device must be added as shown in Figure 2. EEPROMs are often chosen for data storage due to their nonvolatile characteristics. The addition of programmable data storage can be implemented by using a parallel device as shown or with a serial EEPROM.

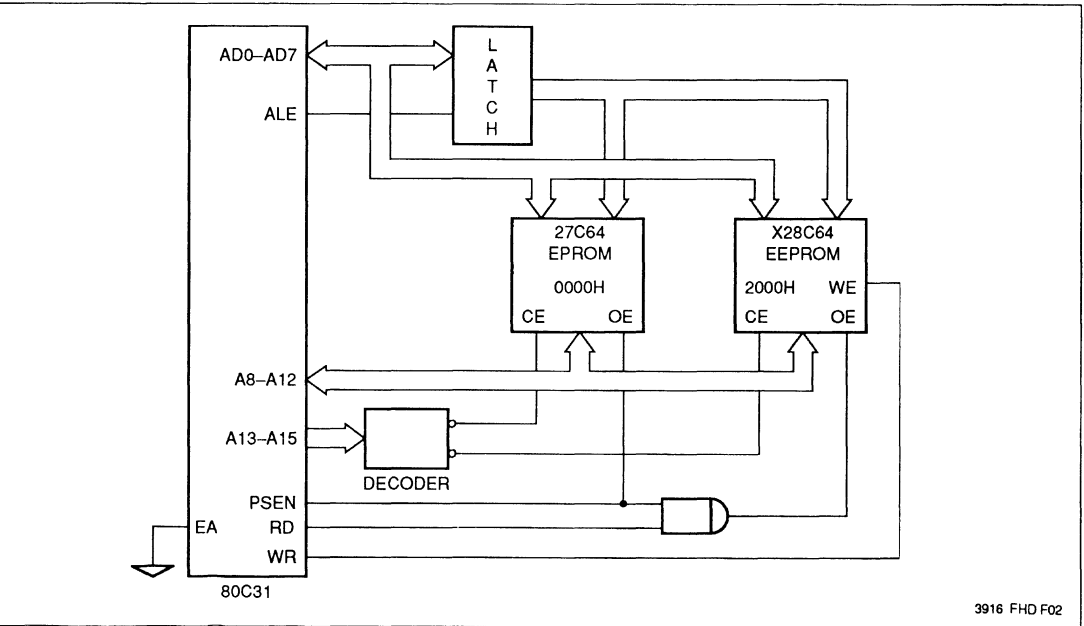
One advantage of using a parallel device is that part of the program code can reside in EEPROM which allows for in-circuit program updates. One of the problems that must be solved when using EEPROMs for program storage is that during a programming cycle, taking up to 10mS, data cannot be read from the device. Because

Figure 1. External Memory Configuration



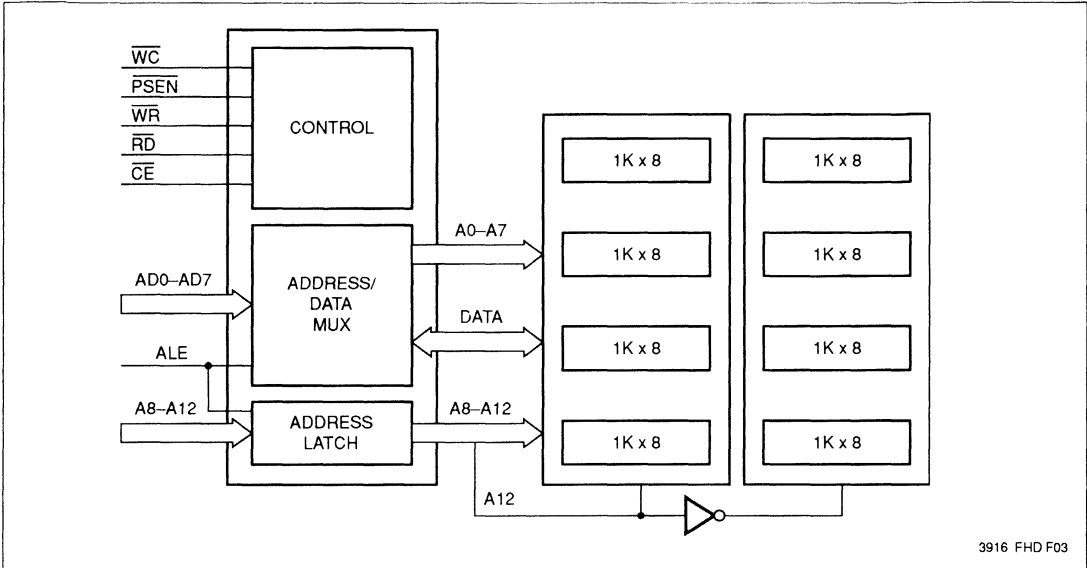
data cannot be read during an EEPROM write cycle processor fetches must take place from a second memory device. The lack of a "read while write" feature makes it awkward or often impossible for a traditional EEPROM to be used as the only external memory device.

Figure 2. Two External Memory Devices



## Recent Trends in Embedded Control Memory

Figure 3. X88C64 Functional Block Diagram



### X88C64 DESCRIPTION

To solve the “read while write” dilemma Xicor developed the X88C64. The X88C64 is the first in a family of devices offered by Xicor that are designed specifically for microcontroller environments. Figure 3 shows the block diagram of the X88C64. The X88C64 provides an architecture consisting of 2 independent 4K by 8 EEPROM memories. Because each half plane is independent of the other a write cycle can take place in one plane while op-code fetches are being performed from the opposite plane. The ability to read while a write is taking place is a unique feature that allows the X88C64 to fill the external program and data requirements in many microcontroller applications.

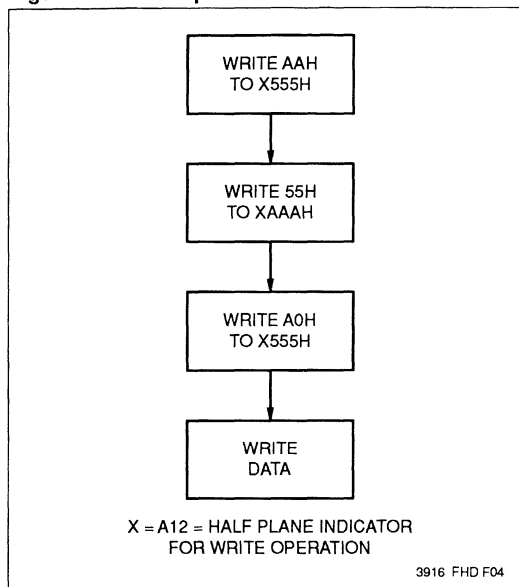
Most microcontrollers provide a multiplexed address and data bus to reduce the number of pins required for an external memory interface. The X88C64 supports this multiplexed bus structure by latching an address when the ALE input makes a high to low transition and transferring data while ALE is low. The multiplexed bus feature eliminates the need for the external address latch required when a traditional byte wide memory is used.

The ability to insure data integrity in an EEPROM has been a design concern for as long as EEPROMs have been available. Inadvertent writes during power up and power down are especially difficult to prevent in microcontroller based environments. The X88C64 provides 2 different software methods of insuring that inadvertent writes do not occur.

The first method required a 3 byte write sequence to occur immediately before new data is written into the X88C64 (Figure 4). This method is similar to the industry standard software data protection (SDP) algorithm used on newer generation EEPROM devices. Each write operation in the 3 step sequence uses a different address/data combination. This unique combination of writes to the device before data is transferred virtually eliminates the possibility of inadvertent write operations. The state of A12 defines where data will be written during the SDP/data transfer sequence. Having A12 define which plane is to be written means that the address sequence used during the 3 step SDP sequence must be modified slightly depending upon which half plane is being altered.

## Recent Trends in Embedded Control Memory

Figure 4. SDP Sequence



A second level of software data protection has been provided with the nonvolatile block protect register (BPR). The BPR is an internal byte of EEPROM memory with each bit controlling the write protect status of one of the eight 1K byte blocks. While a block is protected the data in that segment can no longer be changed. If a protected block needs to be modified its write protect bit in the BPR must first be reset before the block can be written.

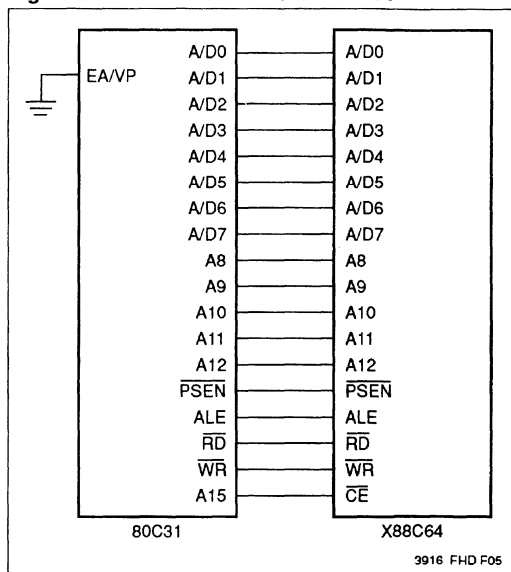
Modifying the BPR is performed with a 6 byte sequence similar to the SDP sequence described earlier. Each bit in the BPR controls the write status in a different 1K byte block. Bit 0 controls the write protect status of addresses 0000H-03FFH, bit 1 controls addresses 0400H-07FFH, etc.

In addition to the software controlled write protect mechanisms on the X88C64 a hardware write control pin (WC) has been provided. Writes to the X88C64 will be inhibited while the WC input is held at a high level. If a write cycle is in progress when the WC pin goes high the write will be allowed to complete and then the X88C64 will enter a protected state.

### X88C64 INTERFACE TO THE 8031

The X88C64 features an interface specifically designed to be compatible with the Intel 8051 family of microcontrollers. The ROM-less version of the 8051, the 8031, is the ideal microcontroller for an X88C64 interface. The interface has been designed so that an X88C64 can be directly connected to the 8031 with no supporting glue logic (figure 5). The pins on the X88C64 are given the same names as the pins they connect to on the 8031.

Figure 5. 8031 and X88C64 Interface



The 8031 memory space is broken into separate program and data areas. Read/Write data memory is accessible with the WR and RD outputs on the 8031. Program memory is read only with access controlled by the 8031's PSEN line. Direct in-circuit program modification is not possible because the 8031 does not provide any way to write to the program memory space. The traditional work-around to allow writes into program space uses glue logic to map a memory device into both data and program space. The X88C64 maps both program and data memory into the same 8K by 8 address

## Recent Trends in Embedded Control Memory

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space to provide write capability to both memory spaces. Because of the dual plane architecture, program execution can continue out of one plane while a write is done in the other plane. This concurrent Read Write (TM) feature makes the X88C64 an ideal choice when in-system program updates are required.

The multiplexed address/data bus interface on the X88C64 is designed to connect directly to the 8031. Data transfer protocols on the AD lines and the ALE polarity match the requirements of an 8031. The X88C64's multiplexed bus eliminates the external address latch required when traditional byte wide memories are used.

If the 8K by 8 EEPROM density of the X88C64 is adequate for external memory requirements the interface to an 8031 requires no glue logic. The CE input is connected to the A15 pin of the 8031 which maps the X88C64 into the memory space between 0000H and 1FFFH. All other pins are connected directly to the pins with the same names on the 8031. This 2 chip solution provides all of the functionality of the 6 chip circuit shown in Figure 2.

The reduced parts count made possible by the 88C64 provides several advantages over the multi-chip external memory configuration. The most obvious advantage is that circuit complexity decreases as the number of devices drop. A second improvement is in the reduced printed circuit board space required to implement similar circuit functions. Manufacturing rework rates should drop as the number of devices on a PCB goes down. System reliability will also be improved because there are fewer components to fail on the PCB. The advantages provided by the X88C64 makes it an attractive alternative to bytewise memories in ROM-less controller applications.

### CONCLUSION

As microcontrollers proliferate into new environments niches will continue to develop for peripheral memory devices to support specific design requirements. Memory manufacturers are becoming increasingly responsive to the applications requirements of the embedded control market. This trend will quite possibly continue until traditional bytewise memories are displaced by devices targeted at specific microcontroller environments.

## **Recent Trends in Embedded Control Memory**

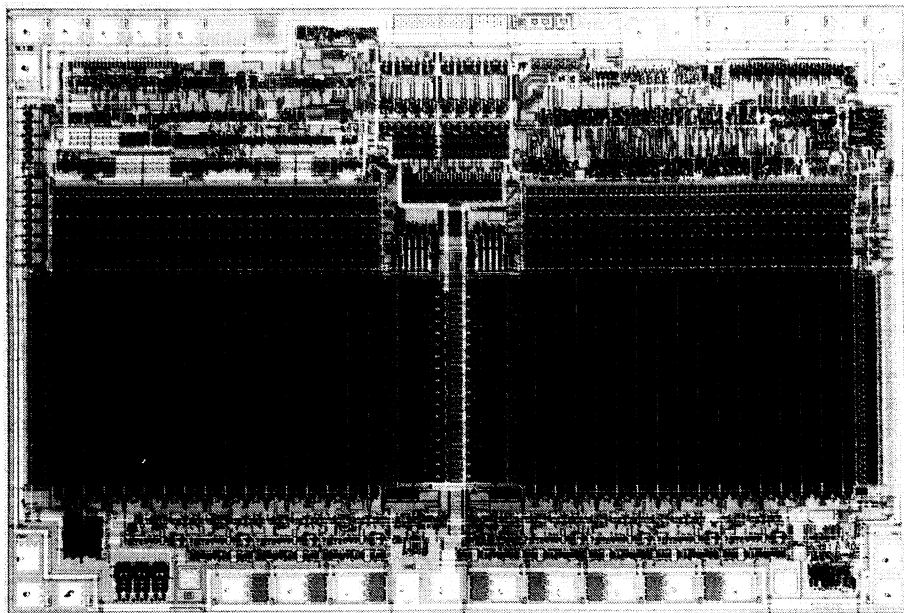
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NOTES



<b>NOVRAM* Data Sheets</b>	<b>1</b>
<b>Serial Products Data Sheets</b>	<b>2</b>
<b>E<sup>2</sup>PROM Data Sheets</b>	<b>3</b>
<b>E<sup>2</sup>POT™ Data Sheets</b>	<b>4</b>
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<b>Memory Subsystems</b>	<b>6</b>
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0114-1

# **X28C64/X28C256 RELIABILITY REPORT**



# INTRODUCTION

The X28C64 and X28C256 are nonvolatile byte-wide E<sup>2</sup>PROMs configured as 8K x 8 and 32K x 8 respectively. Both devices are compliant with the JEDEC approved pinout for byte-wide memories. Both devices operate on a single 5V power supply and feature byte or 64-byte page write, DATA Polling, Toggle Bit and Software Data Protect operations.

The memories are fabricated using Xicor's proprietary textured poly technology. They are designed for applications requiring extended endurance and data retention characteristics greater than 100 years.

Through rigorous environmental and electrical stress testing, the reliability of these devices has been well characterized. This report is a presentation of the data accumulated in testing these devices and supporting information needed to fully utilize the parts.

Figure 1 shows the DIP pin configurations for both the X28C64 and the X28C256; Figure 2 shows the functional block diagram for the X28C256; and Figures 3 and 4 illustrate the physical location of the address bits.

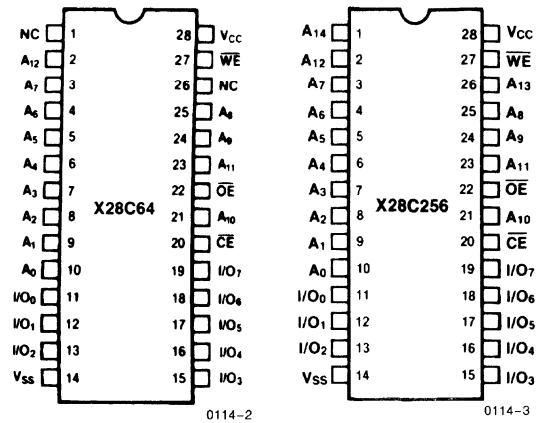


Figure 1: X28C64 and X28C256 DIP pin configurations.

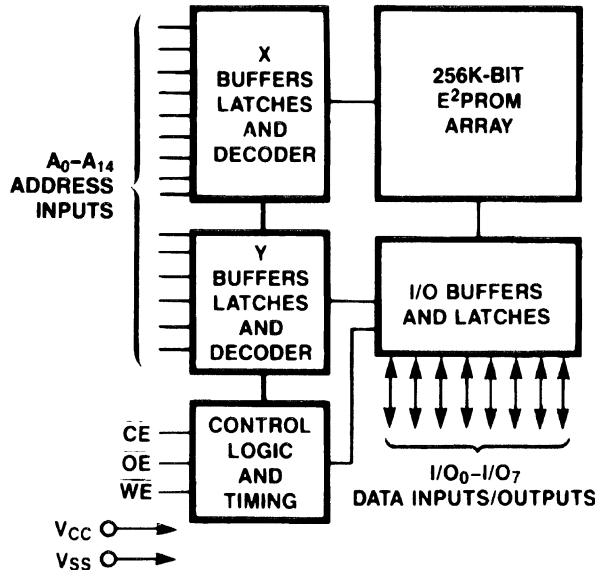


Figure 2: X28C256 functional block diagram.





# RELIABILITY STUDIES AND RESULTS

Before Xicor qualifies a process, it is subjected to accelerated stress testing to characterize potential reliability hazards. The major failure mechanisms that exist are: electromigration in contacts and interconnects, threshold voltage degradation due to hot carriers, corrosion damage due to moisture, and oxide failures due to E<sup>2</sup>PROM operation.

Once these failure mechanisms are characterized and understood, then a product designed using this process must meet further constraints in circuit layout, ESD protection and latch-up protection. These parameters can be varied to further enhance process reliability in the product.

The device is subjected to a series of tests intended to accelerate device degradation and uncover

er flaws in processing or manufacturing. MIL-M-38510 and MIL-STD-883C, Method 5005, Groups A, B, C and D criteria have been the guide for electrical testing, environmental stress testing and package reliability testing.

A summary of product reliability testing and considerations includes the following:

## High Temperature High Voltage Dynamic Lifetest

This test consists of continually reading a device at elevated temperature. V<sub>CC</sub> is set between 5.25V and 6.5V, and the device address is incremented in a binary sequence every 25  $\mu$ s. Its purpose is to uncover latent oxide defects and failures by inducing electrical overstress. The data is shown in Tables I and II.

Lot #	168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.		V <sub>CC</sub>	Device Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In		
1C	0	111	0	111	0	111	0	111	0	111	6.5	222000
2C	1	200[a]	0	199	0	199	0	199	0	199	6.5	398168
3C	0	138	0	80	0	80	0	78			5.25	128888
4C	0	173	0	80	0	80	0	80	0	80	5.25	175624
5C	1	75[b]	0	74	0	74	0	74	0	74	5.25	148168
6C	0	177	0	80	0	80					5.25	96296
7C	1	180[c]	0	100	0	100	0	100	0	100	5.25	213440
8C	0	258	0	160	0	160	0	158	0	158	5.25	334560
Totals	3	1312	0	884	0	884	0	800	0	722		1717144

[a] EOS damage due to latch-up

[b] Oxide defect: 0.6eV

[c] Contact electromigration: 0.9eV

Table I: X28C256 high temperature high voltage dynamic lifetest data.  
(+ 125°C, 5.25V–6.5V)

Lot #	168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.		V <sub>CC</sub>	Device Hours
	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In		
1Q	0	253	0	100	0	100	0	99[a]	0	99	5.25V	224704
2Q	0	342	0	100	0	100	0	100	0	100	5.25V	240656
3Q	0	483	0	100	0	100	0	100	0	100	5.25V	264344
4Q	0	418	0	80	1	80[b]	0	78[a]	0	78[a]	5.25V	214784
5Q	0	288	0	100	0	100					5.25V	131632
Totals	0	1784	0	480	1	480	0	377	0	377		1076120

[a] Unrelated test failure: broken lead

[b] Ionic contamination: 1eV

Table II: X28C64 high temperature high voltage dynamic lifetest data.  
(+ 125°C, 5.25V)

# High Temperature Data Retention Bake

This test induces data retention failures by simulating accelerated storage times. Various aspects of retention as it pertains to reliability are discussed more fully in Xicor publication RR-515: Data Retention in Xicor E<sup>2</sup>PROMs.

The test is also useful in investigating failures caused by mechanical stress (e.g. bond wire lifting). The data for this test is presented in Table III.

# Low Temperature Lifetest

This test is performed at  $-40^{\circ}\text{C}$  and is used to detect hot electron trapping in the gate oxide. These are energetic electrons which exceed the thermal ambient. Data is presented in Table IV.

# Temperature Cycling

This test is designed to promote device failure due to a thermal mismatch between the package and die. The devices are cycled between  $-65^{\circ}\text{C}$  and  $+150^{\circ}\text{C}$  in an air-to-air environment with 10 minute dwell cycles. This data is shown in Table V.

Lot #	Device	48 Hrs.		168 Hrs.		500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.	
		# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In
1	X28C256	0	80	0	80	0	80	0	80	0	80	0	80
2	X28C256	0	61	0	61	0	61	0	61	0	61	0	61
3	X28C64	0	25	0	25	0	25	0	25	1	25[a]	0	24
4	X28C64	0	25	0	25	0	25	0	25	0	25	0	25
5	X28C64	0	25	0	25	0	25	0	25	0	25	0	25
6	X28C64	0	25	0	25	0	25	0	25	0	25	0	25
Totals		0	241	0	241	0	241	0	241	1	241	0	240

[a] Oxide defect: 0.6eV

Table III: X28C64/X28C256 data retention bake results.  
(+ 250°C)

Lot #	Device	500 Hrs.		1000 Hrs.		1500 Hrs.		2000 Hrs.	
		# Fail	# In	# Fail	# In	# Fail	# In	# Fail	# In
A	X28C256	0	33	0	33	0	33	0	33
B	X28C256	0	67	0	67	0	67	0	67
C	X28C64	0	25	0	25	0	25	0	25
D	X28C64	0	25	0	25	0	25	0	25
E	X28C64	0	24	0	24	0	24	0	24
Totals		0	174	0	174	0	174	0	174

Table IV: X28C64/X28C256 low temperature lifetest data.  
(- 40°C, 5.25V)

Lot #	Device	250 Cycles		500 Cycles		1000 Cycles	
		# Fail	# In	# Fail	# In	# Fail	# In
1	X28C256	0	40	0	40	0	40
2	X28C256	0	50	0	50	0	50
3	X28C256	0	50	0	50	0	50
4	X28C64	0	25	0	25	0	25
Totals		0	165	0	165	0	165

Table V: Temperature cycling data.  
(- 65°C to + 150°C)

## Endurance Cycling to End-of-Life

Figure 5 shows device endurance results obtained by changing the data in the entire array to the opposite logic state via mass mode cycling. Device endurance is also characterized by page mode cycling. In this method, each byte or 64-byte page is changed sequentially. This data is presented in Figure 6. Further details on endurance cycling are provided in Xicor publication RR-510: Endurance of Nonvolatile Memories.

Xicor specifications call for a failure rate of less than 1% for 10,000 data changes per bit. Typically, Xicor devices perform far in excess of this.

## Latch-Up Considerations

Latch-up is an inherent fabrication problem in CMOS devices due to the fact that during processing, parasitic bipolar transistors are created in addition to the desired MOS FETs. Design rules to reduce this susceptibility have been developed and are incorporated into Xicor CMOS devices. Further details may be found in Xicor publication RR-516: Latch-up Considerations in Xicor CMOS Processes.

## ESD Evaluation

ESD testing is done in accordance with requirements specified in MIL-STD-883C, Method 3015.6, Notice 7. This document provides guidelines for testing semiconductor devices to human body model discharges.

The X28C64 and X28C256 are compliant to Class 2 (>2000V) sensitivity protection.

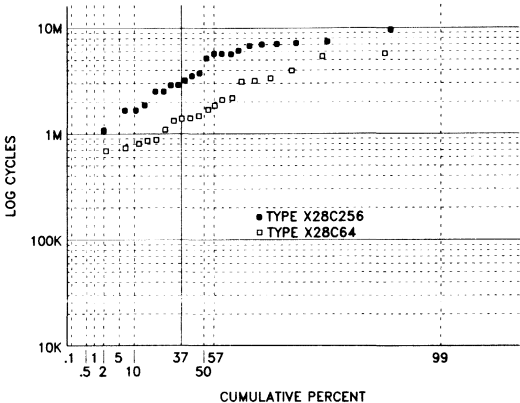
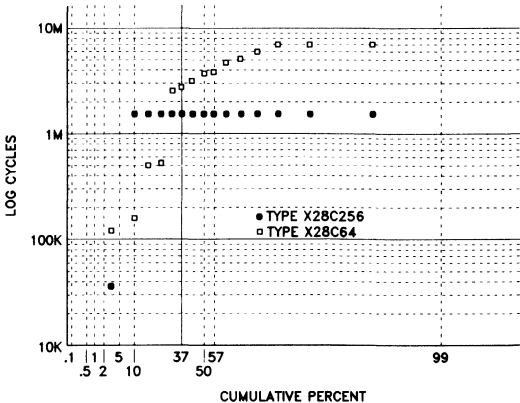


Figure 5: Endurance value distribution plots for X28C64 and X28C256 cycled in mass mode.



**Note:** Page mode cycling stopped at 7 million cycles for the X28C64 and 1.5 million cycles for the X28C256 to free cycling equipment for other tests.

Figure 6: Endurance value distribution plot for X28C64 cycled in page mode.

## Prediction of Failure Rates

Failure rate calculation is easy once the basis for calculation is established. Most semiconductor failures are accelerated to some degree by temperature or voltage, or both. The classic parameter used to accelerate failure rates is temperature. The degree to which any given failure mode is accelerated by temperature is known as the activation energy or as the temperature acceleration factor.

The temperature dependence of a particular failure mechanism can be derived from the Arrhenius model as follows:

$$T_{af} = \text{Exp} \left( \frac{E_a}{k} \times \left( \frac{1}{T_1} - \frac{1}{T_2} \right) \right)$$

where:

$T_{af}$  = Temperature acceleration factor

$E_a$  = Activation energy required to initiate the failure mechanism

$k$  = Boltzmann's constant

$T_1$  = Operating temperature

$T_2$  = Stress temperature

Knowledge of a particular failure mode's activation energy allows one to predict long-term failure rates under normal operating conditions. If the activation energy is not known, it can be determined experimentally.

Typical failure mechanisms and their corresponding activation energies are:

Oxide Breakdown	0.3eV
Electromigration	0.55eV
Oxide Defect	0.6eV
Contact Electromigration <sup>1</sup>	0.9eV
Ionic Contamination	1.0eV

For time dependent dielectric breakdown, voltage acceleration also plays a part.<sup>2</sup> A voltage acceleration factor may be computed using the following model:

$$V_{af} = \text{Exp} \left( \frac{E_s - E_d}{E_{ef}} \right)$$

where:

$V_{af}$  = Voltage acceleration factor

$E_s$  = Stress electric field =  $V_s/T_{ox}$   
(voltage over oxide thickness)

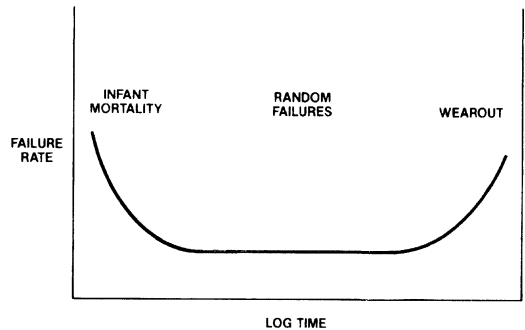
$E_d$  = Operating electric field

$E_{ef}$  = Field constant = 0.062 MV/cm

The voltage acceleration factor is dependent on the electric field and must be calculated for the particular voltage stress and oxide thickness where the failure occurred.

The data presented here is translated into failure rates occurring at normal operating conditions of  $T = 55^\circ\text{C}$  (where  $T$  is the junction temperature), and  $V_{CC} = 5.5\text{V}$ . The power dissipation on-chip raises the junction temperature by  $I_{CC} \times V_{CC} \times \theta_{JA}$ , where  $\theta_{JA}$ , the thermal coefficient, is equal to  $23^\circ\text{C/W}$ . Since the X28C64 and the X28C256 are both CMOS devices, the power dissipation is very low.

Xicor nonvolatile memory failures follow the classic bathtub curve shown in Figure 7.



0114-9

Figure 7: Illustration of bathtub curve of failure rates showing regions in which infant mortality, random failures, and wearout mechanisms dominate the failure rate.

Each region of this failure rate curve has specific failure modes which predominate. For example, the infant mortality region is dominated by failures which arise from processing defects. In production, test flows are designed to eliminate these infant mortality failures by screening, which reduces the incidence of early life failures.

The random failure region, which is the invariant bottom of the curve, is used to find the constant FIT rates calculated in Tables VI and VII. Failure rates are calculated separately for each activation energy, and the total failure rate is obtained by adding the individual numbers. Reliability predictions are then based on an exponential distribution of each failure mode. Since the failures are random in time, they follow the Poisson distribution function, and the failure rate is constant. The consequence of this is that the failure rates for each failure mode are additive, which makes the distribution calculation mathematically tractable. Predicted failure rates are calculated from actual failure rates by making a probability estimation based on the Chi-Square Distribution. By definition, a 60% confidence level means that there is a 60% probability that the failure rate is normally distributed around the calculated number.

End-of-life endurance is found to be dependent on array size, process technology and memory cell design. For reliability purposes, the end-of-life of a device is taken to be the end-of-life of the weakest bit. The mechanism for this failure is known to be oxide trap-up, and can be fitted to an extreme value distribution. Typical end-of-life cycling for the X28C256 is 5,000,000. For the X28C64, the typical end-of-life cycling figure is 2,000,000 cycles. For page mode cycling, the typical figures are greater than 3 million for the X28C64 and greater than 1.5 million for the X28C256. Thus, extremely low failure rates can be expected in typical applications, even at 100,000 or more cycles.

Activation Energy	Number of Failures	Equivalent Hours at 70°C	60% UCL Failure Rate per 1000 Hours at 70°C	Equivalent Hours at 55°C	60% UCL Failure Rate per 1000 Hours at 55°C
0.3eV	0	$4.4 \times 10^6$	0.0200	$7 \times 10^6$	0.0130
0.55eV	0	$1.4 \times 10^7$	0.0065	$3.3 \times 10^7$	0.0028
0.6eV	0	$1.8 \times 10^7$	0.0050	$4.5 \times 10^7$	0.0020
0.9eV	0	$7.3 \times 10^7$	0.0013	$2.9 \times 10^8$	0.0003
1.0eV	1	$1.2 \times 10^8$	0.0017	$5.5 \times 10^8$	0.0004
<b>Totals</b>	1		0.0345		0.0185

Table VI: 60% UCL failure rate predictions for X28C64.

Activation Energy	Number of Failures	Equivalent Hours at 70°C	60% UCL Failure Rate per 1000 Hours at 70°C	Equivalent Hours at 55°C	60% UCL Failure Rate per 1000 Hours at 55°C
0.3eV	0	$7 \times 10^6$	0.0130	$1.1 \times 10^7$	0.0085
0.55eV	0	$2.3 \times 10^7$	0.0040	$5.3 \times 10^7$	0.0018
0.6eV	1	$2.9 \times 10^7$	0.0070	$7.2 \times 10^7$	0.0028
0.9eV	1	$1.2 \times 10^8$	0.0017	$4.7 \times 10^8$	0.0004
1.0eV	0	$1.9 \times 10^8$	0.0005	$8.8 \times 10^8$	0.0002
<b>Totals</b>	2		0.0262		0.0137

Table VII: 60% UCL failure rate predictions for X28C256.



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Failure rate predictions based on this data show a negligible infant mortality rate out in the field (due to extensive pre-shipment screening), and predicted long-term failure rates of 185 FITs for the X28C64 and 137 FITs for the X28C256 at 55°C with a 60% UCL. These numbers are representative of the smaller samples typically available for data analysis and not of the much larger numbers available in production runs.

## Reliability Monitors

To maintain Xicor's quality standards, current production material is systematically sampled and subjected to the same type of stresses and testing used in the qualification procedures. This serves to enlarge the Reliability Department's statistical data base. Failure analysis is performed on material samples and results are published as part of Xicor's ongoing monitor program.

## SUMMARY

The data presented here shows that the X28C64 and X28C256 are both extremely reliable products. Product reliability testing shows low semiconductor failure rates and high end-of-life endurance figures. Inherent data retention in these devices is in excess of 100 years.

These conclusions are based on monitor and device analysis data accumulated over the relatively short lifetimes of these devices. As production continues, more data is obtained through the ongoing reliability monitor system, increasing the number of candidate devices, and improving the ability to make statistical inferences. All FIT rate methods and calculations used here give conservative values.

## REFERENCES

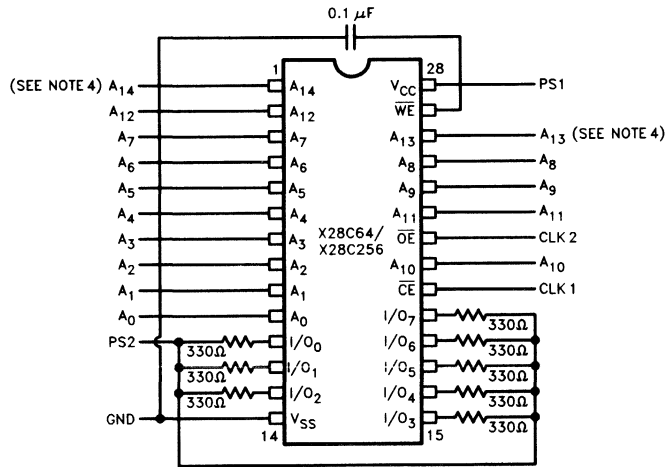
1. D.L. Crothwait, Characteristics of Al-Si Interface Reactions.
2. D.L. Crook, 17th Annual Reliability Physics Symposium (1979): 1-7.
3. Norman B. Fuqua, Reliability Engineering for Electronic Design.

This report is based on data collected through August, 1989.

APPENDIX A

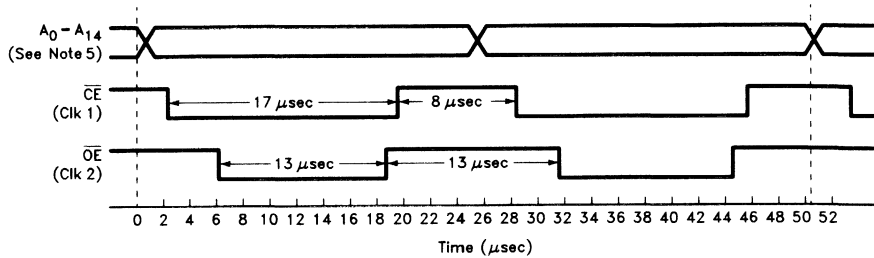
Product	Package Type					
	Plastic		Cerdip		LCC	
	$\theta_{JC}$	$\theta_{JA}$	$\theta_{JC}$	$\theta_{JA}$	$\theta_{JC}$	$\theta_{JA}$
X28C64	35	85	6.3	47	10.4	125
X28C256	4	64	4.3	43.7	8.9	118

Thermal Resistance Table:  $\theta_{JC}$  and  $\theta_{JA}$  expressed in °C per watt.



- Notes: (1)  $\overline{WE}$  must always be hardwired to V<sub>CC</sub> (pin 28) at device as shown.  
(2) All resistors:  
1% metal film  
1/4 W  
(3) I/O pull-up: 330Ω  
(4) Pin 1 (A<sub>14</sub>) and Pin 26 (A<sub>13</sub>) are no connects for X28C64.

X28C64/X28C256 (DIP) Burn-in circuit.

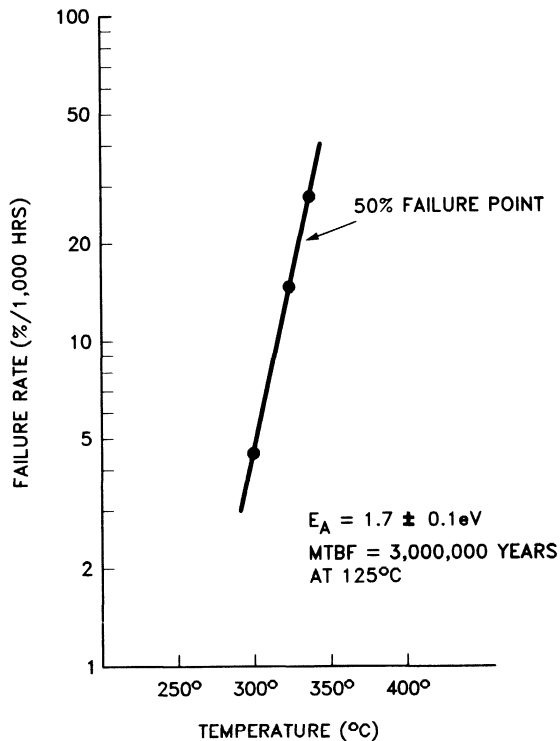


- Notes: (1) A<sub>0</sub>-A<sub>14</sub>: binary sequence every 25 μs.  
(2)  $\overline{WE}$  disabled (tied to V<sub>CC</sub> at device).  
(3) V<sub>IN</sub> Low: ≤ 0.8V V<sub>IN</sub> High: ≥ 2.4V  
(4) V<sub>CC</sub>: 5.5V  
(5) X28C64: address pins A<sub>0</sub>-A<sub>12</sub> are utilized.

X28C64/X28C256 (DIP) Burn-in timing diagram.

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## NOTES



0119-1

# DATA RETENTION IN XICOR E<sup>2</sup>PROM MEMORY ARRAYS

H. A. Richard Wegener

## INTRODUCTION

In Xicor nonvolatile memory devices, data consists of ones and zeroes stored in the memory array in the form of charge retained on a floating gate. During the course of normal operation charges may be added to or lost from the floating gate. The time elapsed between the original transfer of electrons by the act of programming or erasing, and the first erroneous read-out from that memory cell is called retention. The operating conditions during the time period considered may vary widely. Only those conditions permitted by the data sheet need to be considered in its definition. The memory device under consideration may be a single transistor, or it may be a large array of memory cells embedded in peripheral circuitry to function as an E<sup>2</sup>PROM. In either case, the first repeatable malfunction of one single memory cell during read-out defines the end of the retention of that particular device.

The intrinsic retention in Xicor E<sup>2</sup>PROMs is calculated to be many millions of years. However, defects introduced during the manufacture of the memory device may cause the retention to be less than the ideal intrinsic characteristic.

Retention is therefore a reliability problem, and its criterion is its failure rate. Xicor guarantees a failure rate expressed as "5 FITs at 55°C, 60% upper confidence limit". The meaning of this statement, and the reasons leading to it are explained in the paragraphs following this introduction. In most details, they are based on the section on Retention in the forthcoming IEEE Standard on Floating Gate Arrays.

## FLOATING GATE RETENTION: A CAPACITOR DISCHARGE PROBLEM

Charge stored on a floating gate may be thought of as charge residing on one plate of a capacitor, separated from the other plate by the intervening dielectric. Even when all surrounding conductors are grounded, the potential due to the stored charges will cause a very slow discharge through the operation of the Fowler-Nordheim tunneling mechanism. Retention can be modeled and predicted by the expression:

$$t_R = \{C/AB\} * \text{EXP}(B/Vt),$$

where  $t_R$  is the retention time,  $C$  is the capacitance of the floating gate,  $Vt$  is the effective voltage due to the stored charge at which failure occurs, and  $A$  and  $B$  are constants of the Fowler-Nordheim equation.

When measured values for all the variables on the right-hand side of the equation are substituted, retention times well in excess of several million years are obtained. This long term retention is an intrinsic property of Xicor's proprietary floating gate memory technologies, and can be expected as a feature of all Xicor memory cells.

At high temperatures, electrons will also be transferred by Schottky emission, which is dependent on temperature, activation energy, and applied field. This mechanism is described by the Schottky-Richardson equation, which has the form describing the forward current in a Schottky diode. It is this mechanism that gives rise to a temperature dependence of retention, and a measurable activation energy of 1.7eV. With intrinsic retention times exceeding millions of years in the operating temperature range, it is clear that real time retention data cannot be measured. Only under extremely high accelerating temperature conditions can retentions on the order of months be measured. These measurements can then be translated into retention times of approximately 50 billion years at 55°C.

In rare and isolated instances, physical process defects can occur in a memory cell. These defects may give rise to new values for the cell variables and thus result in shorter retention times for the affected cell. Activation energies of 0.6–0.8eV have been measured for such defects.

## Retention in Integrated Circuits

The distinctions between retention in a single memory cell and in an integrated system such as a memory device are threefold: First, there are typically a large number of cells in any memory device. Since a data retention failure is determined by the first cell to fail, data retention in the device is statistically dependent on both the number of cells and their distribution.

Second, being part of a larger system, the cells are exposed to a more varied set of operating conditions. This is due to the diverse needs of the system represented by the chip, and not the simple requirements of a single cell.

Third, the presence of a very large number of cells increases the probability that one of them will contain a defect. In high density E<sup>2</sup>PROMs it can therefore be expected that retention (the failure of the first cell) will have a component, however small, that is determined by the defect density inherent in the technology. Structural defects which give rise to infant failures can be eliminated by production

screens. However, the ultimate retention failure rate is caused by statistical defects inherent in any given oxide process.

## The Reliability Aspects of Retention

The specification of retention is a way of specifying the life expectancy of the data stored in a memory device. The concern for retention is with failures occurring in three phases of the devices' life cycle: a. early in life (infant mortality); b. random failure rate during normal use; and c. the intrinsic failures near the end of life. This can be illustrated by the typical aspects of the classic "bathtub curve", shown in Figure 1.

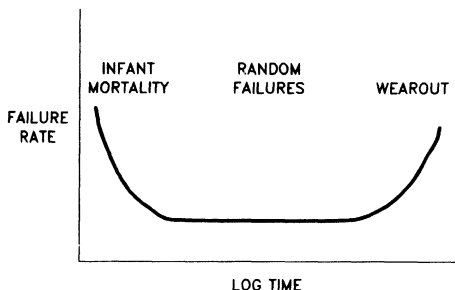


Figure 1: Illustration of bathtub curve of failure rates showing regions in which infant mortality, random failures and wearout mechanisms dominate.

Infant mortality cases are screened out by specific tests before shipment of the product. Some will fail during initial write-erase operations. Some are found by an accelerated voltage stress. Others are caught during a 48 hour storage at 150°C. The last are eliminated by a combination of endurance cycling and retention bake. A constant random failure rate is an indication that infant mortality cases have been eliminated. Since infant mortality failures are screened out during normal testing, they need not be considered a system (end user) reliability problem.

Intrinsic retention failures at the end of device life are determined by the structural design, technology and processing of the memory cell. These failure rates give rise to data retention times many orders of magnitude larger than equipment lifetimes. Successful measurements of intrinsic retention values have required temperatures of 300, 325 and 340°C to determine mean intrinsic retention times of 3000, 90, and 330 hours respectively, and an activation energy of 1.7eV. These translate into retention

times of 1.2 million years at 125°C, 3.6 billion years at 70°C and 50 billion years at 50°C. This was demonstrated in Xicor's **Reliability Report RR-502A**.

The high accelerating conditions make an exact linear extrapolation to normal temperatures difficult with major additional work. Thus, this type of analysis serves mainly to confirm the very large retention times predicted for floating gates obeying Fowler-Nordheim tunneling laws.

This leaves the specification of the random failure rate during normal use as the most practical measure of data integrity. A common measure of the random failure rate is given by the number of failures per 1000 device hours, or the percentage of failures per 1000 hours, both of which can be expressed as FITs ( $[\text{Number of failures} \times 1\text{E9}] / [\text{Number of devices} \times \text{Number of hours tested}]$ ). Since a random failure rate has to be determined under accelerated temperature conditions, the specification must include the temperature to which the accelerated data have been normalized. In addition, a confidence level must be included which (by standard statistical techniques) weights the failure rate estimate according to the number of data points used in deriving it.

## Xicor's Specification of Retention

The Xicor specification for retention is a failure rate of "5 FITs (upper bound at the 60% confidence level) at 55°C". This follows the practice established for (UV erasable) EPROMs, which is a floating gate memory technology with a fifteen year data base.

The value of 5 FITs represents a mean time to failure of 25,000 device years. Another way of expressing this is as a failure rate for a specified retention time. For a 10 year retention, the failure rate is 0.044%.

For comparison, typical (UV erasable) EPROM products have retention failure rates of 20 FITs. The lower failure rate of E<sup>2</sup>EPROMs is due to the fact that their internal high voltage capability acts to cause immediate failures due to defects that would not be affected by the lower voltages in UV erasable EPROMs.

The retention specification as given, includes the failure rate stated as failure units ("FITs"), the temperature at which it is valid, and the statistical confidence level valid for the stated failure rate. For its significance in typical commercial applications and for easy comparison with similar EPROM data, Xicor has chosen 55°C as the reference temperature.

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This is the temperature to which the data taken at accelerated temperatures are normalized. The normalization is performed by the accepted use of the Arrhenius equation, and an activation energy of 0.6eV. Failure rates at other temperatures can also be calculated from the specification given at 55°C, with the help of the same Arrhenius equation and the activation energy of 0.6eV.

The use of a confidence level follows standard reliability practice. When only a few data points (retention failures per year) are recorded, there is a finite chance that they were the result of fluctuations that will make the measured failure rate appear better than the true average. Multiplying the experimental failure rate by the proper factor increases it enough to ensure that it will include 30% of the data that are larger than the average. When this factor has been used, the failure rate is reported at the "60% confidence level (upper bound)". In principle, the choice of a confidence level (expressed as a percentage) is somewhat arbitrary. However, once a given level has been defined, the failure rate stated under its condition can be converted to the value proper for any other level. The 60% level chosen for this specification has the advantages of simplicity and industry acceptance.

## The Determination of Retention Failure Rate

For the measurement of retention failure rates, the acceleration required is somewhat reduced. The activation energy of the mechanism involved in the random failure of floating gate retention has been determined to be near 0.6eV in both (UV erasable) EPROMs and in E<sup>2</sup>PROMs. In order to confirm a failure rate to be equal to or lower than 5 FITs (upper bound at 60% confidence level, at 55°C), at least 75 devices must be stored for 1000 hours (6 weeks) at 250°C. For zero failures at 60% confidence level:  $1/(75 \times 1000) = 13,333$  FITs. When this is divided by 2,724 to extrapolate from 250°C to

55°C the result is 5 FITs. This high temperature necessitates the use of ceramic packages. Plastic packages are limited to a temperature of 150°C. At that temperature, a much larger number of device-hours is necessary to confirm a rate of 5 FITs.

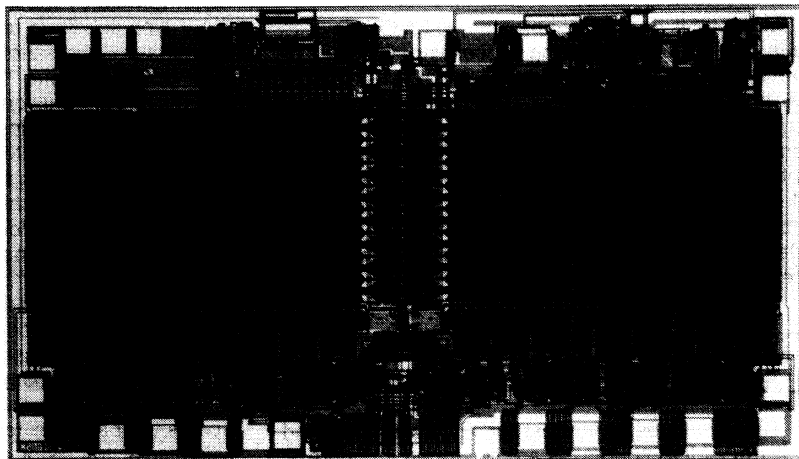
The actual retention failure rate is determined by a test called the "Retention Bake". The devices are stored unpowered at high temperature with a preset (typically checkerboard) data pattern. Devices in plastic packages are stored at 150°C, and ceramic package devices are stored at 250°C. They are then read from time to time. The failures are analyzed, and some are identified as retention failures.

## SUMMARY

The time of retention for data in a Xicor E<sup>2</sup>PROM memory cell is inherently on the order of millions of years. This can be projected theoretically on the basis of a closed form mathematical expression for charge loss that has been verified experimentally. This can also be confirmed by extrapolating experimentally obtained data at high temperatures to normal operating temperatures.

The exact knowledge of this intrinsic retention would be unimportant if every device met its true design and production characteristics. It is the rare presence of defects that introduces the small probability of lower retention times. Retention is therefore a reliability problem, and Xicor has approached it as such.

The failure rates as a function of time have the typical aspects of the bathtub curve. Potential "infant mortality" failures are eliminated by a sequence of screening steps. The "end-of-life" failures are expected to occur a few million years hence. The one characteristic of interest that remains is the "random" failure rate. This failure rate is determined experimentally from Retention Bake data. Based on this experimental data Xicor guarantees retention failure rate of 5 FITs at 55°C at the upper bound of the 60% confidence limit.



0115-1

# **LATCH-UP CONSIDERATIONS IN XICOR CMOS PROCESSES**



# INTRODUCTION

Latch-up is an inherent problem in CMOS devices due to the fact that during processing, MOS FETs are not the only structures fabricated. Parasitic bipolar transistors are also created which act as silicon-controlled rectifiers (SCRs). Since latch-up is inherent in the process, all CMOS devices can be forced into the latched state. The focus in designing CMOS devices is to reduce latch-up susceptibility under normal, and sometimes harsh, operating conditions. Design methods used by Xicor to reduce this susceptibility will be discussed.

# CELL STRUCTURES AND LATCH-UP

The structures of interest for Xicor's 1.8  $\mu\text{m}$  and 1.4  $\mu\text{m}$  CMOS processes are illustrated in Figure 1.

The vertical PNP transistor has its emitter and collector formed by the P+ source/drain diffusion and the P type substrate respectively. Its base is N-well. In the lateral transistor, (the NPN), the base is a P type substrate with the emitter formed by N+ source/drain diffusion and an N-well collector. These two bipolar transistors are cross-coupled with common base-collector regions. Under normal bias conditions, the complementary PNP and NPN transistors remain in the high impedance state, which is referred to as the blocking state. Latch-up can be initiated only when one of the bipolar transistors becomes active. If current flows through any of the parasitic resistors and causes a sufficient voltage drop across the base-emitter junction, one of the parasitic bipolar transistors can be turned on. This forward bias condition of the junction allows collector current to flow. The collector current that flows across the base-emitter resistor of the second parasitic bipolar transistor can cause a sufficient voltage drop to turn on this second transistor.

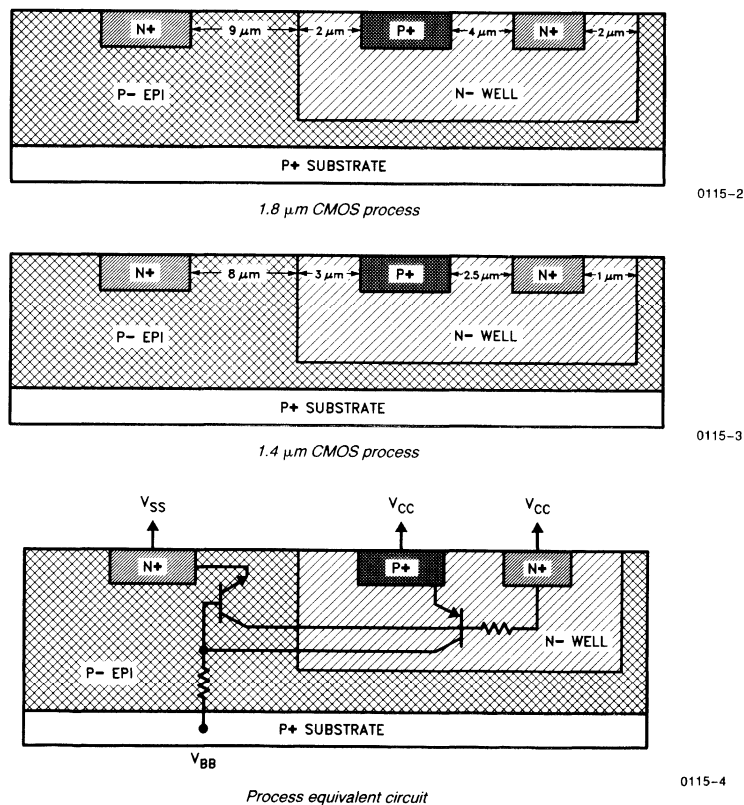


Figure 1: Xicor CMOS processes.

If the current gain of the two transistors and the values of the parasitic resistors are high enough, a regenerative condition is created between the complementary bipolar transistors, where each continues to drive the other. The current in both transistors will increase until either the self limiting condition is reached or the device is destroyed. This high current, low impedance state of the SCR is known as "latch-up".

Latch-up can be destructive to the device when the metal lines are blown or the junctions are melted, or it can be nondestructive. In the second case, the chip can be restored to the blocking state by a power-down and power-up sequence.

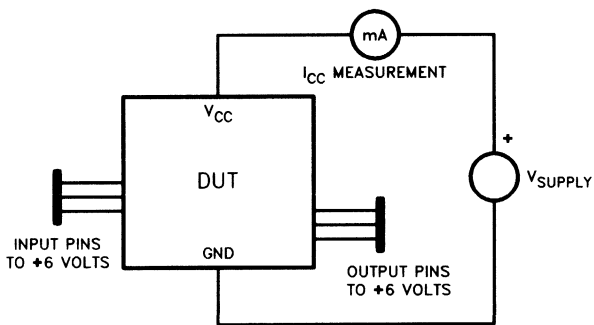
## CAUSES OF LATCH-UP

There are numerous ways in which latch-up can be triggered. The most common ways are during: power-up; supply overvoltage; and pin overvoltage and undervoltage. These conditions are discussed below.

### Power-Up

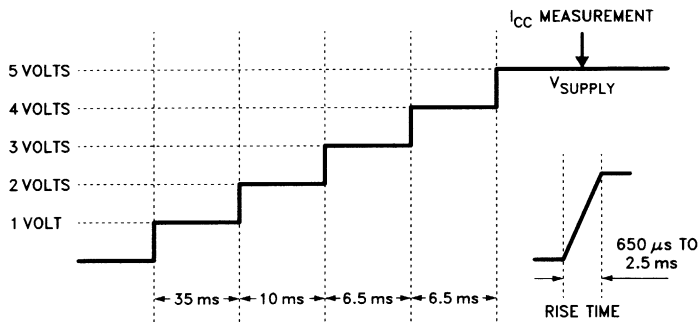
Latch-up can occur when the pins of the device are driven high before the supply voltage has been applied to the circuit. This situation can occur when an unpowered circuit board or device is plugged into a system that is already under power.

Figures 2 and 3 illustrate the test set-ups for both the slow power-up and the fast power-up tests. Results of these tests are presented in Tables I and II.



0115-5

Block diagram



0115-6

Typical timing diagram

Figure 2: Slow power-up test set-up.

Characteristics:  $I_{CC}$  latch-up current due to input and output pins in an overvoltage condition during power-on ramp.

Test conditions: All inputs and data outputs equal to  $V_{CC} + 1V$  minimum.  $V_{CC}$  ramps from 0V to 5V in 1V steps, ramp rate is less than or equal to 0.2V/ms.

Maximum  $I_{CC}$ : 80 mA

Latch-up condition:  $I_{CC} \geq 80$  mA

Temp: +25°C

Product Type	$I_{CC}$ (in $\mu A$ )			
	Process	Typ.	Max.	Min.
X28C64, C256	1.8 $\mu m$	650	750	613
X28C010	1.4 $\mu m$	85	2.3 mA	70

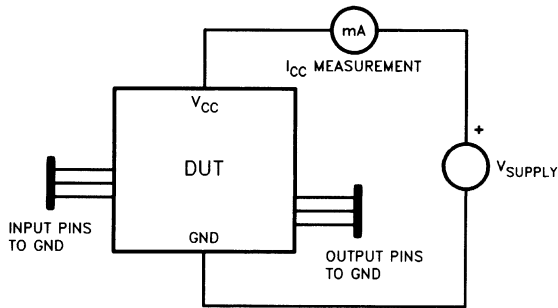
Temp: -55°C

Product Type	$I_{CC}$ (in $\mu A$ )			
	Process	Typ.	Max.	Min.
X28C64, C256	1.8 $\mu m$	860	900	800
X28C010	1.4 $\mu m$	330	2.8 mA	290

Temp: +125°C

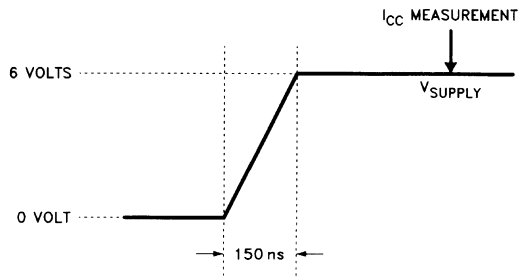
Product Type	$I_{CC}$ (in $\mu A$ )			
	Process	Typ.	Max.	Min.
X28C64, C256	1.8 $\mu m$	530	540	520
X28C010	1.4 $\mu m$	300	2.0 mA	65

Table I: Results of slow power-up test.



Block diagram

0115-7



Typical timing diagram

0115-8

Figure 3: Fast power-up test set-up.

Characteristics:  $I_{CC}$  latch-up current induced by hot socketing.

Test conditions: All inputs and data outputs equal to 0V.  $V_{CC}$  ramps from 0V to 6V in 200 ns or less.

Maximum  $I_{CC}$ : 100 mA

Latch-up condition:  $I_{CC} \geq 100$  mA

Temp: +125°C

Product Type	Process	$I_{CC}$ (in mA)		
		Typ.	Max.	Min.
X28C64, C256	1.8 $\mu$ m	7.0	100[a]	5.8
X28C010	1.4 $\mu$ m	11.0	13.6	9.9

[a] Latch-up induced only for conditions where  $V_{CC} \geq 5$ V

Table II: Results of fast power-up test.

Temp: +25°C

Product Type	Process	$I_{CC}$ (in mA)		
		Typ.	Max.	Min.
X28C64, C256	1.8 $\mu$ m	8.5	9.9	8.0
X28C010	1.4 $\mu$ m	13.0	16.4	11.1

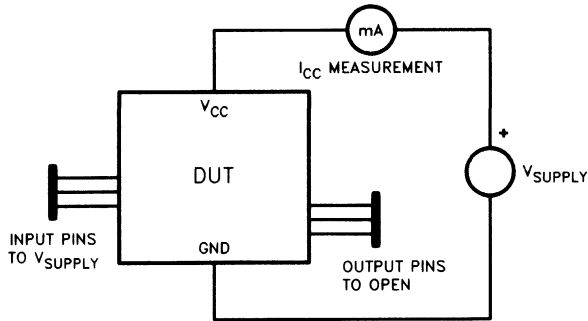
Temp: -55°C

Product Type	Process	$I_{CC}$ (in mA)		
		Typ.	Max.	Min.
X28C64, C256	1.8 $\mu$ m	11.5	13.2	10.5
X28C010	1.4 $\mu$ m	16.0	19.9	14.6

# Supply Overvoltage

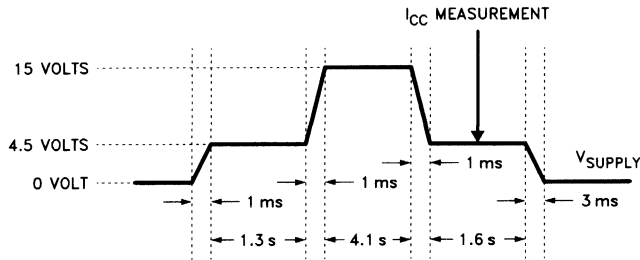
A supply voltage exceeding the absolute maximum rating can cause an internal junction to break down or produce a substrate current that triggers latch-up.

Figure 4 illustrates the test set-up for the supply overvoltage test. The results of this test are presented in Table III.



Block diagram

0115-9



Typical timing diagram

0115-10

Figure 4: Supply overvoltage test set-up.

Characteristics:  $I_{CC}$  latch-up current due to supply overvoltage.

Test conditions: All inputs are tied to supply. All data outputs are open. The unit is powered up to 4.5V, then 15V is applied to the  $V_{CC}$  pin. Measurement is done at 4.5V  $V_{CC}$ , after the 15V pulse.

Maximum  $I_{CC}$ : 100 mA

Latch-up condition:  $I_{CC} \geq 100$  mA

Temp: +25°C

Product Type	$I_{CC}$ (in mA)			
	Process	Typ.	Max.	Min.
X28C64, C256	1.8 $\mu$ m	7.15	8.00	6.25
X28C010	1.4 $\mu$ m	11.5	12.2	10.5

Temp: -55°C

Product Type	$I_{CC}$ (in mA)			
	Process	Typ.	Max.	Min.
X28C64, C256	1.8 $\mu$ m	8.10	9.56	7.02
X28C010	1.4 $\mu$ m	10.1	97.0[a]	151 $\mu$ A

Temp: +125°C

Product Type	$I_{CC}$ (in mA)			
	Process	Typ.	Max.	Min.
X28C64, C256	1.8 $\mu$ m	4.00	100[a]	3.31
X28C010	1.4 $\mu$ m	12.5	96.0[b]	7.08

[a] Latch-up induced for overvoltage  $\geq 14$ V

[b] Latch-up induced for overvoltage  $\geq 13$ V

Table III: Results of supply overvoltage test.

## Pin Overvoltage and Undervoltage

Ringling, or noise glitches on the I/O pins, can create a transient forward bias condition at the I/O junction. If the transistor is part of a susceptible latch loop, latch-up could result.

Figures 5 and 6 illustrate the test set-ups for both the pin overvoltage and the pin undervoltage tests. Results of these tests are presented in Tables IV and V.

Characteristics:  $I_{CC}$  latch-up current due to pin in overvoltage condition.

Test conditions: Untested inputs tied to supply of 4.5V. Untested outputs are open. Triggered voltage of +15V (with max. 100 mA) is applied to pin under test.

Maximum  $I_{CC}$ : 100 mA

Latch-up condition:  $I_{CC} \geq 100$  mA

Temp: +25°C

Product Type	$I_{CC}$ (in mA)			
	Process	Typ.	Max.	Min.
X28C64, C256	1.8 $\mu$ m	7.30	7.70	5.30
X28C010	1.4 $\mu$ m	11.0	13.1	10.0

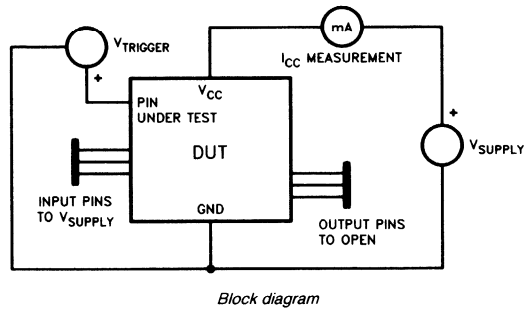
Temp: -55°C

Product Type	$I_{CC}$ (in mA)			
	Process	Typ.	Max.	Min.
X28C64, C256	1.8 $\mu$ m	8.00	8.90	6.60
X28C010	1.4 $\mu$ m	8.00	9.50	7.40

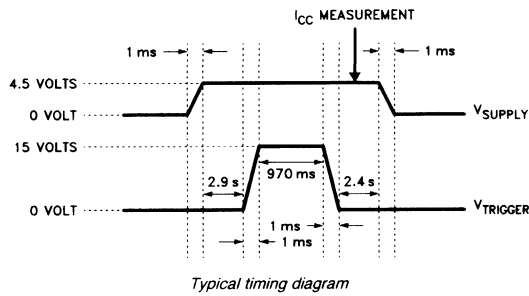
Temp: +125°C

Product Type	$I_{CC}$ (in mA)			
	Process	Typ.	Max.	Min.
X28C64, C256	1.8 $\mu$ m	3.90	3.95	3.60
X28C010	1.4 $\mu$ m	14.5	15.6	11.7

Table IV: Results of pin overvoltage test.

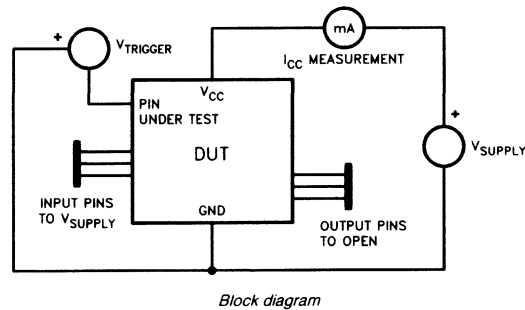


0115-11

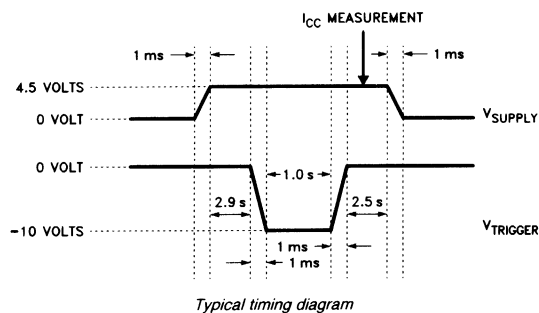


0115-12

Figure 5: Pin overvoltage test set-up.



0115-13



0115-14

Figure 6: Pin undervoltage test set-up.

Characteristics:  $I_{CC}$  latch-up current due to input/output pins in undervoltage condition.

Test conditions: Untested inputs tied to supply of 4.5V. Untested outputs are open. Triggered voltage of -10V (with max. -100 mA) is applied to pin under test.

Maximum  $I_{CC}$ : 100 mA

Latch-up condition:  $I_{CC} \geq 100$  mA

Temp: +25°C

Product Type	$I_{CC}$ (in mA)			
	Process	Typ.	Max.	Min.
X28C64, C256	1.8 $\mu$ m	6.0	6.5	5.1
X28C010	1.4 $\mu$ m	10.5	12.3	10.1

Temp: -55°C

Product Type	$I_{CC}$ (in mA)			
	Process	Typ.	Max.	Min.
X28C64, C256	1.8 $\mu$ m	6.5	7.6	5.3
X28C010	1.4 $\mu$ m	15.0	22.3	11.4

Temp: +125°C

Product Type	$I_{CC}$ (in mA)			
	Process	Typ.	Max.	Min.
X28C64, C256	1.8 $\mu$ m	3.8	4.3	2.9
X28C010	1.4 $\mu$ m	10.0	32.8	9.6

Table V: Results of pin undervoltage test.

## LATCH-UP SUSCEPTIBILITY IN XICOR CMOS PRODUCTS

In order to increase the immunity of its CMOS products against latch-up, Xicor employs several methods in its product design. These include:

- 1) Negative substrate bias: A -3.5V  $V_{BB}$  generator prevents transient forward biasing of the base-emitter junction of the SCR.
- 2) Large spacing between the N+ diffusion area and the N-well during processing eliminates the potential for the parasitic NPN to be active.
- 3) An epitaxial layer on a low resistivity substrate reduces the parasitic resistance, and lowers the gain of the lateral transistor.
- 4) Guard rings around the diffusion area reduce substrate current and substrate resistance.
- 5) All input and output buffers are connected only to N+ diffusions. No connections to P+ diffusions (P-channel source or drain) are made.

## TESTING FOR LATCH-UP

Xicor characterizes the latch-up susceptibility of its 1.8  $\mu$ m and 1.4  $\mu$ m CMOS devices by following specifications defined in MIL-M-38510/750. These test procedures are recommended by the JEDEC JC-40-2 CMOS Logic Standardization Committee. The X28C64 and X28C256 were used to test the 1.8  $\mu$ m process, while the X28C010 was used to test the 1.4  $\mu$ m process.

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## CONCLUSION

Data accumulated from the various stress tests show that Xicor's CMOS products exhibit excellent latch-up immunity. These CMOS devices are carefully designed and fabricated under the design and process rules which were discussed previously. This ensures that Xicor products operate in the blocking state even under harsh operating conditions.

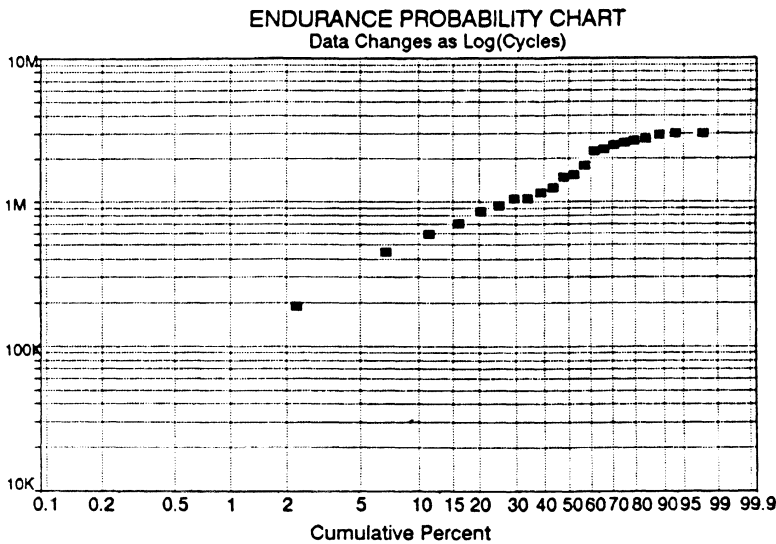
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- This report is based on data collected through June, 1989.



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## NOTES



0122-1

**X24C01  
RELIABILITY  
REPORT**

## INTRODUCTION

The X24C01 is a 1024-bit serial E<sup>2</sup>PROM, internally organized as thirty-two 4-byte pages. Like all Xicor products, the X24C01 employs Xicor's Textured Poly Floating Gate technology, which has been demonstrated to be the optimum technology for full featured nonvolatile memories.

### Reliability Studies and Results

At Xicor, all new products are subjected to a series of tests before the device is qualified. In these tests, the device is stressed at elevated voltages and high and low temperatures. The purpose of these tests is to accelerate standard semiconductor infant mortality failures and any potential defects that may occur as random failures during the device's normal useful lifetime. These data are then used to predict semiconductor failure rates under normal operating conditions.

In addition, Xicor has undertaken studies to determine characteristics unique to nonvolatile memories, such as retention and endurance. This report also includes a group of standard environmental tests to insure reliable operation under all extremes. Explained below are the tests and stresses to which the X24C01 was subjected.

### High Temperature Dynamic Life Test

In the High Temperature Dynamic Life Test, (DLT) the device array is first written with a topological

checkerboard pattern. It is then subjected to a temperature of 125°C at 5.5V in a continuous sequential read mode. All units are tested for retention and functionality at readouts at 48 hours, 168 hours, 500 hours, 1000 hours and 2000 hours.

This test is designed to accelerate early life failures, (first 48 Hours) and to uncover latent defects that would be seen as random failures during the normal useful lifetime. These data, along with the HTHV data are used to predict actual field reliability for the device. The DLT test results are shown in Table 1.

In addition, all units submitted to the tests and stresses that follow, are first subjected to DLT for 168 hours. The test lots are then divided, with some units continuing DLT and the balance split among other tests.

### High Temperature High Voltage (HTHV)

The purpose of this stress is to accelerate failures due to mobile ionic contamination, electrical over-stress and latent gate oxide defects. In this stress, a static bias is established throughout the circuit by applying 5.5V to all pins while V<sub>SS</sub> is held at ground in an ambient temperature of 150°C. The units are stressed for 1000 hours, with readouts occurring at 48 hours, 168 hours 500 hours and 1000 hours. The results of the tests are shown in Table 2.

Lot #	48 Hours		168 Hours		500 Hours		1000 Hours		2000 Hours		Total Device Hours *
	IN	Fail	In	Fail	In	Fail	In	Fail	In	Fail	
1	905	1 <sup>(b)</sup>	904	0	150	0	150	0	150	0	383,280
2	979	0	979	0	143	0	143	0	143	0	379,456
3	1036	1 <sup>(b)</sup>	1035	0	149	0	149	0	149	0	397,168
4	1000	0	1000	0	150	1 <sup>(a)</sup>	149	0	149	0	393,300
5	996	0	996	2 <sup>(c)</sup>	149	0	149	0	149	0	392,488
6	189	0	189	0	49	0	49	0	49	0	112,448
Totals	5105	2	5103	2	790	1	789	0	789	0	2,058,140

**Note:** a. Ionic Contamination  
b. oxide breakdown  
c. Leaky Select Transistor

\* Device-hours excludes the first 48 hours

**Table 1. X24C01 Dynamic Life Test. V<sub>CC</sub> = 5.5V and T<sub>A</sub> = 125°C**

Lot #	168 Hours		500 Hours		1000 Hours		Total Device Hours
	In	Fail	In	Fail	In	Fail	
1	35	0	35	0	35	0	35,000
2	48	0	48	0	48	0	48,000
3	50	0	50	0	50	0	50,000
4	48	0	48	0	48	0	48,000
5	52	0	52	0	52	0	52,000
6	25	0	25	0	25	0	25,000
Totals	258	0	258	0	258	0	258,000

Note: b. oxide breakdown

**Table 2. X24C01 High Temperature High Voltage Test.  $V_{CC} = 5.5V$  and  $T_A = +150^{\circ}C$**

### Failure Rate Calculation

#### Determining The Failure Rate Unit

If there is one failure in 20,000 devices in 1000 hours, the failure rate will be:

$$\frac{1 \text{ failure}}{20,000 \text{ devices} \times 1000 \text{ hours}} = 5 \times 10^{-8}$$

The failure rate of a device is calculated in FIT (Failure unit). One FIT is defined as one failure in  $10^9$  device-hours. Thus, the above failure rate is:

$$\frac{5 \times 10^{-8} \times 10^9 \text{ failures}}{10^9 \text{ device-hours}} = 50 \text{ FITs}$$

As previously mentioned, the results from the DLT and HTHV tests allow one to predict the long-term failure rates for the device under normal operating temperature and voltage conditions.

#### Acceleration Factors

Each failure mechanism accelerated by temperature is associated with an activation energy  $E_a$ . The reaction rate at which a process is accelerated by temperature is given by the Arrhenius equation<sup>4</sup>:

$$R = R_0 \exp \left( -\frac{E_a}{kT} \right)$$

Where:

$E_a$  = Activation Energy

$T$  = Absolute Temperature

$k$  = Boltzmann's Constant =  $8.62 \times 10^{-5} \text{ eV}/^{\circ}K$

For a given activation energy, where  $t_1$  and  $t_2$  are the times to failure at the normal operating temperature of  $T_1$  and the stress temperature  $T_2$ , respectively, then the relationship between the times to failure is :

$$TAF = \frac{t_1}{t_2} = \frac{\exp \left( \frac{-E_a}{kT_2} \right)}{\exp \left( \frac{-E_a}{kT_1} \right)} = \exp \left\{ \frac{E_a}{k} \times \left( \frac{1}{T_1} - \frac{1}{T_2} \right) \right\}$$

Where:

TAF = Temperature Acceleration Factor

$T_1$  = Operating Temperature

$T_2$  = Stress Temperature

Knowledge of a particular failure mode's activation energy allows one to predict long-term failure rates under normal operating conditions.

Typical failure mechanisms and their corresponding activation energies are:

Oxide Breakdown	0.30eV
Metal Electromigration	0.55eV
Oxide Defect	0.6eV
Silicon Electromigration	0.90eV
Ionic Contamination	1.0eV

Ea in eV	Total Device Hours		# of Fails	Equivalent Device Hours		Calculated Failure Rate (FIT)		60% UCL Failure Rate (FIT)	
	@ +125°C	@ +150°C		@ +55°C	@ +70°C	@55°C	@70°C	@55°C	@70°C
0.30	2.058E+6	2.58E+5	0	1.682E+7	1.08E+7	0	0	59.46	92.90
0.55	2.058E+6	2.58E+5	0	8.472E+7	3.60E+7	0	0	11.80	27.74
0.60	2.058E+6	2.58E+5	2	1.183E+8	4.66E+7	16.89	42.93	25.34	64.40
0.90	2.058E+6	2.58E+5	0	9.082E+8	2.24E+8	0	0	1.101	4.459
1.00	2.058E+6	2.58E+5	1	1.816E+9	3.84E+8	0.550	2.605	1.101	5.210
			3			17.45	45.54	98.82	194.7

- Notes: 1. One FIT = 1 failure in  $10^9$  device-hours. To convert to failure rate percent per 1000 hours, divide FITs by 10,000  
2. Failures from 48 hour DLT are excluded, since such failures are considered infant mortalities and are minimized by extensive screening prior to shipment.

**Table 3. Summary of Semiconductor Failure Calculations for the X24C01.**

For time dependent gate oxide breakdown ( $E_a = 0.3\text{eV}$ ), there is also a voltage acceleration factor (VAF) given by Crook's equation<sup>5</sup>, as follows:

$$\text{VAF} = \exp \left( \frac{E_s - E_d}{E_f} \right)$$

where:

$$E_s = \text{stress field} = \frac{V_s}{T_{ox}}$$

$$E_d = \text{operating field} = \frac{V_d}{T_{ox}}$$

$T_{ox}$  = Gate Oxide

$E_f$  = Field Constant = 0.062MV/cm

Table 3 contains the results of these calculations. Also included in the table is the 60% upper confidence level (UCL) calculation. This indicates that with a 60% confidence the actual failure rate will be below that calculated. We also made the conservative assumption of including the Oxide Breakdown, Metal and Silicon Electromigration ( $E_a = 0.30$ ,  $E_a = 0.55\text{eV}$  and  $E_a = 0.90\text{eV}$  respectively) failure rates. These failure mechanisms should be included whether they were observed or not, since they could be anticipated.

#### Data Retention Bake

Data stored in  $E^2$ PROMs are associated with the absence or presence of electrical charge stored on the floating gate. A device is considered to have failed if the charge leaks off the floating gate. A floating gate at equilibrium (+ and - charges are equal) will be read as one or zero depending on the sense amp circuitry.

Therefore, in order to test for leakage, a charge is placed on the floating gate such that when the cell is read it will be opposite to that read at equilibrium. After being written with the specified pattern, the units are baked for 2000 hours at  $150^\circ\text{C}$ , with readouts occurring at 500 hours, 1000 hours and 2000 hours. The results of the tests are shown in Table 4. A retention FIT rate calculation was also performed and is shown in Table 5. It should be noted: based on Xicor studies on data retention of all its memories Xicor specifies 100+ years data retention. For details on data retention in Xicor memories refer to Reliability Report RR-515.

Lot #	48 Hours		168 Hours		500 Hours		1000 Hours		2000 Hours		Total Device Hours *
	IN	Fail	In	Fail	In	Fail	In	Fail	In	Fail	
	34	0	34	0	34	0	34	0	34	0	68,000
1	34	0	34	0	34	0	34	0	34	0	68,000
2	34	0	34	0	34	0	34	0	34	0	68,000
3	34	0	34	0	34	0	34	0	34	0	68,000
4	34	0	34	0	34	0	34	0	34	0	68,000
5	34	0	34	0	34	0	34	0	34	0	68,000
Totals	170	0	170	0	170	0	170	0	170	0	340,000

**Table 4. Data Retention Bake @ 150°C**

Ea in eV	Total Device Hours		# of Fails	Equivalent Device Hours		Calculated Failure Rate (FIT)		60% UCL Failure Rate (FIT)	
	@ +125°C	@ +150°C		@ +55°C	@ +70°C	@55°C	@70°C	@55°C	@70°C
0.60	0	3.40E+5	0	4.077E+7	1.60E+7	0	0	24.53	62.35
Totals			0			0	0	24.53	62.35

**Table 5. Data Retention Failure Rate Calculations**

#### Extended Endurance and Data Retention

Devices must retain correct data after long-term operation. A stress called endurance/retention is designed to examine a device's performance at retaining data after repeated write cycles to all memory locations. In this test, all units are subject to 100,000 write cycles, followed by a static bake at +150°C. After the bake the devices are tested for data retention and functionality. The results of the test are shown in Table 6 below.

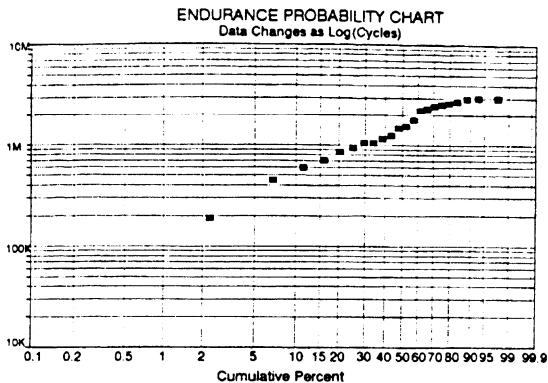
Lot #	100 K Cycle		168 Hours @ 150°C	
	In	Fail	In	Fail
3	50	0	50	0
4	32	0	32	0
5	49	0	49	0
Totals	131	0	131	0

**Table 6. Endurance/Data Retention**

#### End of Life Endurance

Long-term operational life of a device is also measured by how long it can endure repetitive data changes. This is the purpose of endurance testing. In this test the units are subject to continual data changes until the first bit in its array is read incorrectly. There are two major methods of cycling: block or mass mode, where the entire array is changed in one cycle; and page cycling, where each physical row is cycled in one operation, requiring 32 write operations to cycle the entire array one time. The data shown in the endurance probability chart in Figure 1 were collected by page cycling.

This probability chart is a tool developed by Xicor to fit the endurance limit of the weakest bit in the entire array to an extreme value distribution. The ability of Xicor to use this method is a result of the Textured Poly Floating Gate technology employed. This technology has one prevalent failure mechanism, trap-up, which is the diminishing cell program margins due to electrons trapping in the tunneling oxides.



**Figure 1. Typical X24C01 Lot Endurance**

#### Low Temperature Dynamic Life Test

As geometries of semiconductor memories are scaled down, hot electron trapping in the gate oxides has been detected in other technologies. In order to determine if hot electron trapping could impact the reliability of the X24C01, a Low Temperature Dynamic Life test was performed. This test is functionally identical to the DLT test, but with the ambient temperature set at  $-40^{\circ}\text{C}$ . The test results in Table 7 indicate hot electron trapping is not a concern with the X24C01.

Lot #	168 Hours		500 Hours		1000 Hours		Device Hours
	In	Fail	In	Fail	In	Fail	
1	50	0	50	0	50	0	50,000
2	52	0	52	0	52	0	52,000
3	50	0	50	0	50	0	50,000
4	50	0	50	0	50	0	50,000
5	50	0	50	0	50	0	50,000
6	25	0	25	0	25	0	25,000
Totals	277	0	277	0	277	0	277,000

**Table 7. Low Temperature Dynamic Life Test**

#### ENVIRONMENTAL STRESSES

This group of tests is performed on plastic packages to insure that excessive humidity and ambient vapors will not cause failures and also to in-

sure temperature cycling will not have detrimental effects on the combination of materials used.

The three major failure modes for plastic packaged devices under moisture test are:

- Mobile Ions - Ions on the passivation glass are made more mobile by humidity. If enough charge transfer occurs, a device parameter could be altered or a parasitic transistor could be introduced, degrading device performance.
- Chemical Corrosion - Phosphorous is commonly used in the passivation and under metalization layers. Sufficient phosphorous, when combined with water molecules, produces phosphoric acid which may etch away aluminum lines.
- Electrolytic Corrosion - When a voltage potential exists between two adjacent metal lines under enhanced surface conditions, (presence of moisture) an electrolytic corrosion process may be triggered. This condition could result in an open metal line.

#### Autoclave

Autoclave or pressure pot testing subjects a device to a 2 atmosphere steam environment. This test will accelerate mobile ionic drift, chemical corrosion and to some extent electrolytic corrosion. The test results are summarized in Table 8.

Lot #	48 Hours		96 Hours		144 Hours		Device Hours
	In	Fail	In	Fail	In	Fail	
1	52	0	52	0	52	0	7488
2	52	0	52	0	52	0	7488
5	52	0	52	0	52	0	7488
Totals	156	0	156	0	156	0	22464

**Table 8. Steam Autoclave**

#### 85°C/85% Relative Humidity Stress

85/85 testing is performed to determine life expectancy of devices in high temperature and high humidity environments. This test will accelerate all three environmental failure modes. It is an especially good test for detecting electrolytic corrosion.

85/85 tests can be performed in two ways. The first is by supplying voltage to  $V_{CC}$  with all other pins alternately biased at 0V and +55.V. The

second method is to test the device with  $V_{CC}$  at 0V and all other pins alternately biased at 0V and +5.5V. This provides a potential between metal lines and insures maximum humidity at the die surface. Results of these tests are shown in Tables 9 and 10.

Lot #	500 Hours		1000 Hours		Device Hours
	In	Fail	In	Fail	
1	52	0	52	0	52,000
2	52	0	52	0	52,000
5	52	0	52	0	52,000
Totals	156	0	156	0	156,000

**Table 9 . 85/85 (power off)**

Lot #	500 Hours		1000 Hours		2000 Hours		Device Hours
	In	Fail	In	Fail	In	Fail	
1	52	0	52	0	52	0	104,000
2	52	0	52	0	52	0	104,500
5	52	0	52	0	52	0	104,000
Totals	157	1	156	0	156	0	312,500

**Table 10. 85/85 (power on)**

## Temperature Cycling

This test subjects the devices to temperature extremes of  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ . this test is performed to stress the package to detect poor bond wire attachment and to determine if there is a potential problem due to thermal mismatch between the die and the package material that could cause device failures. The results of these tests are tabulated in Table 11

Lot #	250 Cycles		500 Cycles		1000 Cycles		Device Hours
	In	Fail	In	Fail	In	Fail	
1	52	0	52	0	52	0	52,000
2	52	0	52	0	52	0	52,000
3	52	0	52	0	52	0	52,000
4	52	0	52	0	52	0	52,000
5	52	0	52	0	52	0	52,000
6	24	0	24	0	24	0	24,000
Totals	284	0	284	0	284	0	284,000

**Table 11. Temperature Cycling  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$**

## CONCLUSION

The X24C01 has been demonstrated to be a highly reliable semiconductor memory. The semiconductor FIT rate is well below the industry average for a comparable device. Xicor specifies the X24C01 as having an endurance of 100,000 cycles and data retention of 100 + years. The additional environmental data indicates that the combination of process technology and assembly techniques provides a highly reliable device under all environmental conditions.



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## NOTES



## Xicor Endurance Report

RR-520

H. A.R. Wegener

### INTRODUCTION

This report describes endurance relating to Xicor's products employing the Direct Write™ cell. These devices display enhanced endurance cycling characteristics that are attributable to the direct write cell, process enhancements and improved screening techniques.

This report will also review a number of important issues relating to the endurance of Xicor memories: a review of the technology and device operation, methods of measurement and examples of how to calculate the effect of endurance on a system's reliability. Additional information on the endurance of Xicor's earlier products is available in Xicor's reliability reports RR-504 (1984), RR510 (1988) and a reliability brief (Determining System Reliability from E<sup>2</sup>PROM Endurance Data, 1987).

### DEFINITION OF ENDURANCE

Endurance is a characteristic common to all current nonvolatile memory technologies. It describes the number of data changes that a memory device can sustain without a write failure. The endurance of 5 volt only E<sup>2</sup>PROMs is one of the major characteristics of interest to the end user. The easy reprogrammability of these devices leads naturally to applications requiring the E<sup>2</sup>PROMs to reliably sustain a high number of writes.

### ENDURANCE LIMITATIONS OF FLOATING GATE TECHNOLOGIES

All floating gate nonvolatile memories depend upon applying a field across a dielectric in the memory cell. This causes electrons to be injected into the dielectric by Fowler-Nordheim tunneling. These electrons drift across the dielectric and either add charge to, or take charge from, the floating gate in order to change the state of the cell.

Two effects which limit endurance have been identified and studied in detail. The first effect, known as "trap-up", occurs when a small fraction of the electrons tunneling through a dielectric are trapped in the dielectric. After a large number of data changes this trapped charge becomes large enough to inhibit further charge transfer.

The second effect, known as time dependent dielectric breakdown is caused by the stress on the dielectric due

to the electric field applied during tunneling. Which of these two effects dominates depends upon the technology used to make the Fowler-Nordheim tunneling devices.

Two major technologies are used today to manufacture commercial floating gate E<sup>2</sup>PROMs. One, known as the thin oxide technology, depends on tunneling across a thin (~100Å) dielectric lying between two parallel silicon surfaces used for charge transport. The other technology depends on local field enhancement near the surface of a poly silicon film to inject electrons into the conduction band of a relatively thick (~600Å to 1000Å) dielectric. Once injected into the dielectric, the electrons drift across the remaining dielectric under lower drift fields existing in the bulk of the dielectric. The enhanced fields occur at the poly silicon surface of the polysilicon. The bumps along this surface lend the name textured poly floating gate (TPFG) technology.

Electrons are less likely to become trapped while drifting across the thin dielectric than the thicker oxide of the TPFG approach. On the other hand, the entire thin dielectric experiences the field required for tunneling which exists only in a portion of the TPFG oxide, with the result that the thin dielectric approach is more susceptible to dielectric breakdown.

### IMPLICATIONS OF FAILURE MECHANISMS ON PRODUCT RELIABILITY

The implications of the various failure mechanisms on product reliability requires a familiarity with statistical distributions. This is based on the fact that few users are affected by the behavior of a typical bit of the E<sup>2</sup>PROM memory. Rather, what affects the user is the behavior of the worst bit in an array because the failure of the first bit defines the endurance of the memory device.

Studies have shown that TPFG memories have a low failure rate until an endurance level of a few hundred thousand cycles is reached. After this the failure fraction will increase. This is due to the very low extrinsic failure rate for oxide defects in this technology. The increase of failure rate at end of life is due to the intrinsic property of electron trapping. Thin oxide memories exhibit a continuously increasing failure fraction beginning at a low

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# Xicor Endurance Report

endurance level. This is due to the extrinsic oxide failure rate which dominates this technology (reference: N. Mielke, A. Fazio, H. Liou, 25th Interantional Reliability Physics Symposium, 1987)

Therefore, TPGF technology has the advantage of a failure mechanism that is a measurable intrinsic property which can be controlled like any other process parameter. However, with the thin oxide technology the extrinsic property of random oxide breakdown is unpredictable and thus more difficult to measure and control.

## DIRECT WRITE™ CELL

In 1985 Xicor developed the Direct Write cell and began implementing it on all new designs. Figure 1 is a cut away view of the cell structure. Poly 1 acts as both the cell ground isolation transistor and programming cathode; Poly 2 is the floating gate; and Poly 3 acts as both

the select word line transistor and erase tunnel anode. Poly 2 is totally surrounded by an oxide electrically isolating it from all other device structures. Its channel region acts as both the floating gate charge-conditional current path for reading and the data conditional coupling capacitor for writing.

A schematic representation is illustrated in Figure 2. Because the construction of the cell incorporates the poly 1 to 2 programming and poly 2 to 3 erase tunneling elements in a single structure, data storage is a direct, single pass operation, involving the following sequence. First the poly 1 line, common to the entire array, is brought low, cutting off the conduction path from the bit line through the cell to array ground. Next, the bit lines are set up to either 0V for an erase operation or about 16V for a program operation. The poly 3 word line is ramped up to about 22V in about 1ms to drive the nonvolatile charge transport.

Figure 1. Cross Section View of Direct Write Cell

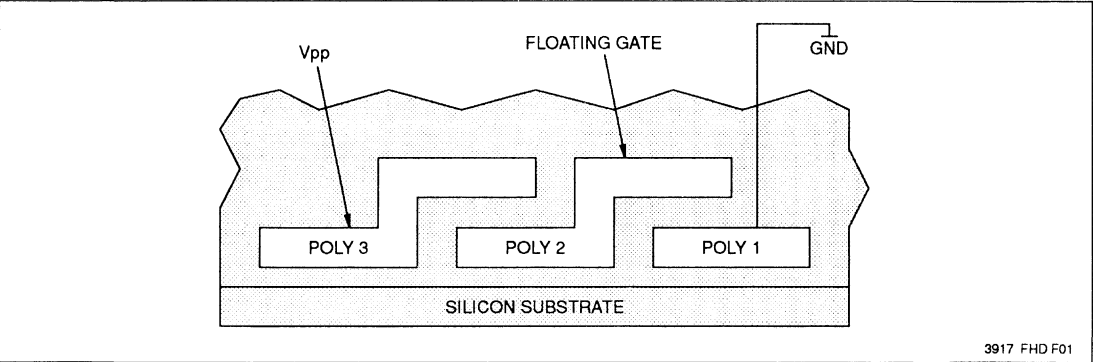
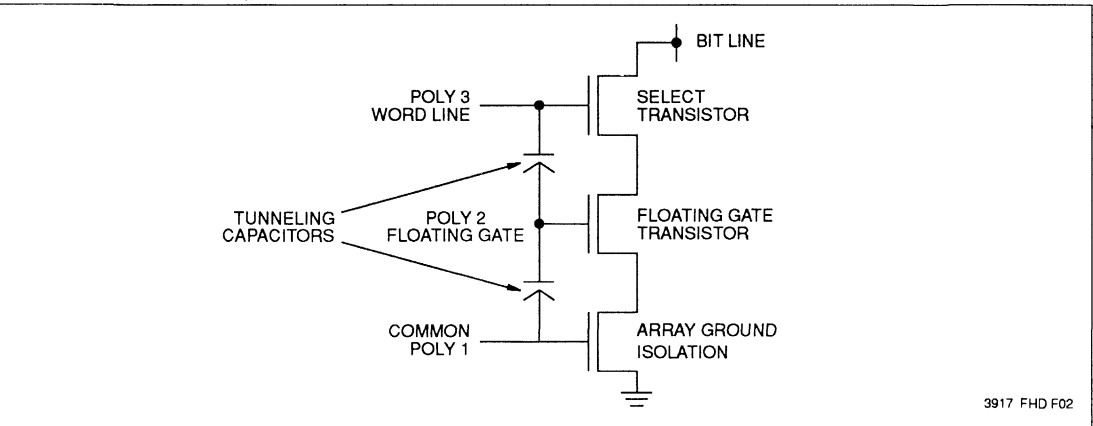


Figure 2. Schematic Representation of the Direct Write Cell



## Xicor Endurance Report

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To erase, the bit line is grounded, whereupon the channel voltage under poly 2 capacitively couples the floating gate towards ground. This develops sufficient voltage across the poly<sup>3</sup>/2 tunneling element to cause electrons to tunnel off of the floating gate.

To program, the bit line is taken high and the channel potential capacitively couples the floating gate positively. This develops sufficient voltage across the poly 2/1 tunneling element to cause electrons to tunnel onto the floating gate.

### EXPECTED XICOR MEMORY ENDURANCE FAILURE MECHANISMS

As discussed in previous sections, with Xicor's textured poly floating gate (TPFG) technology there are two endurance effects which cause failures: the first, and most predominant, is trap-up at end-of-life; the second is oxide defect related.

Trap-up is the result of the accumulation of trapped negative charge in the dielectric that is caused by the repeated passage of current through the dielectric material. This trapped charge creates an opposing potential within the dielectric which suppresses Fowler-Nordheim tunneling. The endurance limit is reached when the trapped charge suppresses tunneling to the extent that insufficient charge is tunneled to change the state on the floating gate.

Because TPFG employs a thick insulating oxide the average electric field across the oxide is 5 to 7 times lower than the field used in a thin oxide device. As a result, oxide defect related failures are greatly reduced. However, defects will occur in the memory array in a random manner. The majority can be screened through electrical testing, leaving a small tail of potential random failures that occur during the expected normal life time of the device.

Based on this, endurance failures for Xicor memories fit a standard bath tub curve distribution similar to those for standard semiconductor failures with the time element of the X axis being replaced by the number of cycles. The front end failures are defect related and screened during electrical testing; the random failure during the useful life of the device is next; this is followed by the end of life based on trap-up.

Therefore, Xicor endurance specifications are based on these two factors, with worst case assumptions. The specification is generally an order of magnitude lower than the typical end of life. The specified endurance level

is then periodically monitored to insure the random oxide failure rate is below the established levels.

### ENDURANCE MEASUREMENTS

Based on the way the direct write cell operates, an endurance cycle is most accurately defined as one "data change.". This means that a change from a "zero to a one" is counted as one cycle and the change from "one to a zero" is counted as one cycle. If a cell containing a "zero" has another "zero" written to it no change of data has occurred and that cell's endurance has not been impacted.

Two endurance measurements are regularly performed. One is the end of life, where devices are cycled until they either all fail or until cycling must be terminated due to time considerations. These tests are conducted utilizing special test modes that permit erasing or programming the entire array in a single cycle.

The second measurement is based on cycling units up to their specified minimum endurance level. This minimum endurance level is specified many times below the average end of life cycles. The method of cycling for this measurement is generally in page mode, to more closely approximate system usage. The cycling is performed by sequencing through the addresses so that all pages in the array are cycled equally. It should be noted that Xicor equates page cycling with byte cycling based on extensive studies indicating cycling an array byte by byte vs page by page is equivalent. Because cycling in byte mode is prohibitive time-wise, cycling is generally performed in page mode for data collection.

Based on the page mode endurance measurements, a failure rate for random failures occurring within the specified endurance limit, can be established in PPB (parts per billion). This number can be used to calculate the expected endurance failure rate for a system.

### SYSTEM FAILURE RATE CALCULATIONS

There are two ways of expressing the impact of endurance on system reliability. First, the probability of a system failure or the percent of systems failing due to endurance is calculated based on the estimated number of cycles for each page over the life of the system. Second, the failure rate in FIT can be determined by including the expected system lifetime in the calculation. Both methods are equivalent evaluators of system reliability.

## Xicor Endurance Report

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### FAILURES IN PARTS PER BILLION CYCLES

This method is based on data collected in cycling the devices as described in the previous section on measurement. Based on the test results, a failure rate in parts per billion page cycles (PPB) is calculated. Summaries for different device type PPBs are available from the factory.

To illustrate how this number can be used to calculate the failure rate due to endurance, a system is defined below and a step by step sequence to calculate the system's endurance failure rate is given.

Assume that the memory is a X28C256 with a random endurance failure rate of 1PPB per page cycle and a specified endurance limit of 10K cycles per byte.

In this application 12 pages are cycled 10,000 times and the balance of pages are cycled 100 times over the lifetime of the system.

The total number page cycles is:  $(12 \times 10,000) + (500 \times 100) = 170,000 \text{ PageCycles}$

The system failure rate is simply 170,000 times 1PPB = 170 PPM or .017%. This means .017% of these systems would be expected to have a failure due to endurance during their expected lifetime.

### FAILURES IN TIME (FIT)

Failures in time is a more traditional method of evaluating reliability. This is the industry standard of expressing the usual semiconductor related failures.

The total system failure calculations in the above example can be easily converted into FIT rates by inserting the time element. Assume the planned system life is ten years or 87,600 hours. FITs are expressed in failures per 10<sup>9</sup> device hours: therefore, the calculation would be:  $(170/10^6) \times (10^9/87,600) = \sim 1.9 \text{ FIT}$

# DETERMINING SYSTEM RELIABILITY FROM E<sup>2</sup>PROM ENDURANCE DATA

By Richard Palm

Xicor has published numerous reliability reports regarding data retention and endurance; however, the relationship of this data to system reliability warrants further analysis and discussion. This paper will discuss two methods for determining the affect of endurance on system reliability. The first method will use actual data collected on the X2816A and the second method will use data collected on the X2864A.

## Definition of Terms

**Endurance** - is the ability of a nonvolatile memory to sustain repeated data changes.

**Endurance Failure (Level)** - is the limit of endurance, expressed in number of write cycles, when the *first bit* of any memory device or memory system is found to be in error after a required data change.

**Write Cycle** - to reduce testing time Xicor uses a test method whereby the entire array of the device under test is written in a single write cycle. Therefore, all references to "write cycle" equate to every bit in the entire array (device or system array) being written.

**Cumulative Failure (Probability)** - the percentage of parts not expected to attain a particular goal; i.e., endurance level.

**Note:** all endurance data used in this report were collected at a cycling frequency of one cycle per 100ms and at +25°C.

## Background

There are three reliability categories for nonvolatile memories: semiconductor, data retention and endurance.

- Semiconductor reliability pertains to several failure modes common to all semiconductor devices such as oxide rupture and micro-cracks.

- Data retention refers to the capability of a non-volatile memory device to retain valid data under worst case conditions.
- Endurance is the ability of a nonvolatile memory device to sustain repeated data changes.

Xicor reliability reports, RR502A and RR504, detail these three categories for Xicor devices. Reliability is easily deduced for semiconductor failures and data retention. The affect of endurance on reliability is not so straightforward.

Because endurance screening is a destructive procedure, Xicor performs endurance life tests on a sample basis. The data collected from these tests are then plotted onto an extreme value distribution graph to determine the endurance distribution for a particular lot of devices.

## Using the Extreme Value Distribution Data

Figure 1 is an extreme value distribution graph for twenty X2816A devices and Table 2 (located on the last page) is the raw data used to generate the straight line shown.

- In this sample lot the lowest ranked device (#1) exceeded 279,000 write cycles before the first bit failure occurred; however, the graph extends to the left to show that only ~ .01% of all devices from this manufacturing lot will fail before 200,000 cycles.
- The maximum of the extreme value distribution occurs at the 37% cumulative probability point (statistically, 37% of all devices will fail to reach this endurance level), indicating that the predicted most probable endurance of devices in this lot is 460,000 cycles.

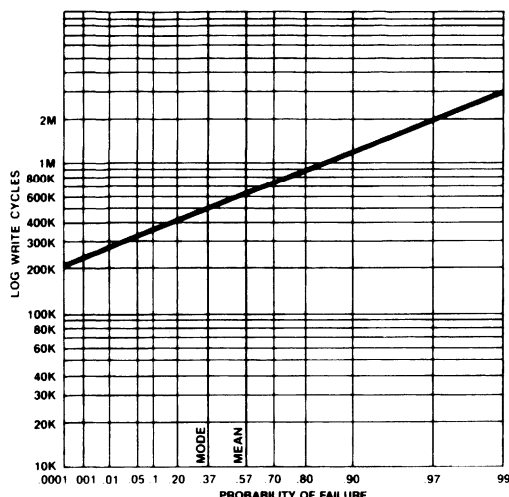


Figure 1: Extreme Value Distribution Graph for One Twenty Piece Lot of X2816As

Reliability data are generally stated in terms of percent failures per 1000 hrs. This can be easily derived from the extreme value graph in a two step procedure.

The system design parameters for this example are chosen as follows: the lifetime of the system is five years; and each X2816A will experience 250,000 write cycles over the lifetime of the system.

- The first step determines the failure rate per 1000 write cycles using the formula  $W = C/E$  where:  
 $W$  = failure rate in %/1000 write cycles  
 $E$  = endurance level chosen for the system (250,000 write cycles) divided by 1000.  
 $C$  = cumulative failure rate at  $E$  (in this case .5%).  
 Therefore  $W = .5\%/250 = .002\%/1000$  write cycles.
- Converting this to percent failures per 1000 hours requires  $H = W \times A$  where:  
 $H$  = failure rate in %/1000 hrs.  
 $W$  = failure rate in %/1000 write cycles  
 $A$  = number of write cycles per hour. (i.e.,  $2.5 \times 10^5$  cycles/5 years)

In our case,  $H = .002 \times 5.7 = .0114\%/1000$  hrs.

In the above example the entire X2816A is being rewritten at the rate of 5.7 times every hour. In some applications this could occur, but generally the frequency is much lower. Using the same graph and arbitrarily choosing the lowest cumulative failure rate depicted at 200,000 write cycles and performing the same calculations, the percent failures per 1000 hrs. drops dramatically.

$W = .01/200 = .00005\%/1000$  write cycles

$H = .00005 \times 4.56 = .00022\%/1000$  hrs.

## Predicting System Endurance Reliability Within Design Constraints

This next example is based on data collected on the X2864A. The system requirements for which the data were collected are defined as follows: the life expectancy of the system is ten years; the number of write cycles is 10,000. Therefore, Xicor cycled five lots of approximately three hundred devices each, for 10,000 write cycles. The data were collected by cycling the devices every 100ms at  $\sim 25^\circ\text{C}$ . Table 1 summarizes the data collected.

LOT #	# OF UNITS	# OF FAILURES	% FAILURES
1	297	4	1.35
2	295	2	0.68
3	295	4	1.36
4	298	6	2.01
5	299	6	2.01
TOTAL	1484	22	1.48

Table 1: Raw Data From Cycling X2864A Devices 10,000 Times

The overall failure rate of devices unable to reach 10,000 write cycles is 1.48%. How does this relate to system reliability?

- The system is defined as having a life expectancy of ten years or  $87.6 \times 10^3$  hours.
- The failure rate in percent per 1000 hours is determined by dividing the percent of parts unable to reach 10,000 write cycles by system's life expectancy in thousands of hours.

Therefore, reliability based on endurance for this system is:

$$1.5\%/87.6 = 0.017\%/1000 \text{ hrs.}$$

Temperature

RR504 describes in detail the affect of temperature on endurance. In general, this report shows that for every 50°C rise in temperature the endurance rate doubles. The data collected for the above examples was taken at + 25°C. Therefore, for systems operating at a more common + 40°C the endurance will improve. Figure 2 illustrates the case for the X2816A.

- The line labeled + 25°C is the same as that in Figure 1.
- The added line is for the predicted increase in endurance at + 40°C.
- The cumulative failure rate at 250,000 write cycles moves from .5% to less than .01% and the endurance reliability increases as follows:  
 $W = .01\%/250 = .00004\%/1000 \text{ write cycles}$   
 $H = .00004\% \times 5.7 = .0002\%/1000 \text{ hrs.}$

The failure rate for the X2864A sample lots can be expected to decrease by a factor of ~ 1.30, for the increase in operating temperature from +25°C to +40°C; yielding a failure rate of .013%/1000 hrs. vs. the unfactored .017%/1000 hrs.

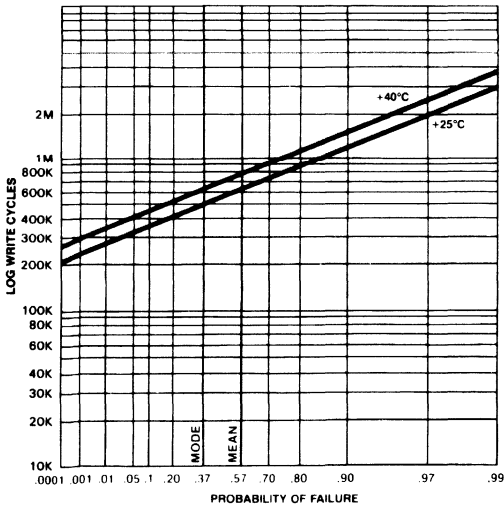


Figure 2: Affect of Ambient Temperature on Endurance

Frequency of Writing

Xicor reliability report RR504 describes device operation and the affects of frequency of writing to a device. Figure 3 is a copy of a graph in RR504, depicting the relationship of write cycle frequency on the endurance of a Xicor nonvolatile memory.

There are two key relationships illustrated by the graph in Figure 3.

- As the frequency of writing decreases the slope of the plotted line, the extreme value, decreases.
- Although the most probable endurance (the 37% cumulative failure point) does not show appreciable change, the decreasing slope is significant in the region most concerned with predicting reliability, the .01% to 5% region (shaded area of Figure 3).

It is in this region that a system's reliability is determined. Arbitrarily choosing the .1% probability of failure point, Figure 3 shows:

- A write cycle frequency of 1 per 100 seconds increases the endurance level by a factor of 2 over a write cycle frequency of 1 per 100 milliseconds.

0018-5

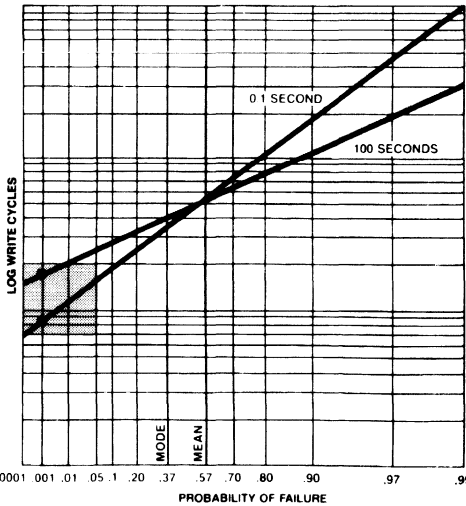


Figure 3: Affect of Write Cycle Frequency on Endurance

0018-3



## Conclusion

This paper has illustrated two methods for determining system reliability based on endurance. In the examples given, the failure rates due to endurance are well below industry standards for semiconductor failures.

Additionally, by factoring in the affects of both temperature and frequency of writing, the endurance failure rates for the X2816A system and X2864A system may be predicted specifically for the user's application.

DEVICE RANK	THOUSANDS OF WRITE CYCLES
1	297
2	315
3	355
4	365
5	400
6	410
7	450
8	450
9	510
10	572
11	620
12	620
13	650
14	680
15	800
16	820
17	940
18	952
19	992
20	1400

Table 2: Ranked Endurance Data for Twenty Pieces of X2816A Devices

0018-4

## RADIATION-INDUCED SOFT ERRORS AND FLOATING GATE MEMORIES

J. M. Caywood & Reliability Engineering Staff

### ABSTRACT

A new failure mechanism which may be induced in floating gate memories by ionizing radiation is discussed. This mechanism, which is designated a "firm error", is modeled in some detail. Calculations which show that the MTBF for alpha particles emitted by ceramic packaging materials is  $>100,000$  years are verified experimentally. The effect of device scaling on this mechanism is also discussed.

### INTRODUCTION

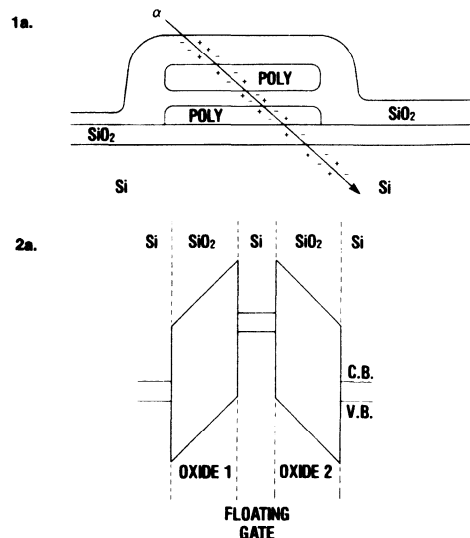
Ionizing radiation incident on floating gate non-volatile memories can give rise to three types of observable effects. The radiation may induce damage in the peripheral circuitry (hard errors); it may cause upset of the sense/readout circuitry (soft errors); or it may cause data loss by transfer of charge from the floating gate. The first of these groups of effects is common to all MOS circuitry and has been investigated extensively over many years.<sup>1</sup> The second group of effects was first observed in dynamic RAMs and has since also been observed in static RAMs and microprocessors.<sup>2-5</sup>

The third effect, on which this paper will concentrate, is qualitatively different than the "soft errors" which are observed in volatile RAMs. In the soft error case, thermalized carriers are collected from relatively long ( $\sim 10\mu\text{m}$ ) distances in the Si substrate which can result in efficient collection of the charges generated by an alpha particle ( $\sim 50\%$ )<sup>4</sup>. In the case to be discussed here, the carriers collected on the floating gate may come from two sources. One source is carriers created by the ionizing radiation in the  $\text{SiO}_2$  which lies between the floating gate and another electrode or the substrate when they are at a different potential. The second source is electrons excited in the floating gate which have enough kinetic energy to surmount the potential barrier between the conduction bands in Si and  $\text{SiO}_2$ . As will be developed in this paper, these effects are relatively inefficient ( $<1\%$ ). Unlike soft errors which are caused by a single ionizing particle, charge transfer to a floating gate is cumulative so that effects of many ionizing events occurring over an extended period of time must be considered.

To differentiate this phenomenon from soft errors which, if they occur in floating gate memories, are dependent upon the design of the readout circuitry and are temporary read errors which can be corrected by re-reading the floating gate, and from hard errors which render all or part of the memory inoperable, we shall call it "firm error". This firm error has the operational characteristics that it causes a read error which cannot be corrected by re-reading the floating gate, but it can be corrected by re-writing the cell or cells in question to provide a completely functional memory.

### MODELING THE CHARGE TRANSFER

Figure 1a shows a typical cross-section through a floating gate memory structure where the + and - signs indicate that electron-hole pairs are created along the track. Figure 1b shows a potential diagram of the same structure. Clearly electron-hole pairs created in the oxides on both sides of the floating gates will drift apart and tend to discharge the gate. Similarly electrons injected from the floating gate into either oxide will discharge the gate. The problem can therefore be broken into that of computing the charge created in the oxide and that of estimating the charge injected from the Si into the oxide.



0019-7  
Figure 1: Cross section and potential diagram of a typical floating gate memory transistor; a) the cross section is cut through in the direction of current flow; b) the potential diagram is shown for the case that the floating gate is programmed and the access gate grounded.

## INJECTION OF CHARGE FROM Si INTO SiO<sub>2</sub>

Emission of excited electrons from Si into SiO<sub>2</sub> is a complex process. Some of the phenomena occurring are illustrated schematically in Figure 2. Hot electrons created by the ionizing particle may be scattered by acoustic or optical phonons, other electrons, or the surface itself. The requirement for electrons to reach the surface with sufficient crystal momentum,  $\kappa$ , normal to the surface to surmount the barrier ( $\kappa_{\perp}^2/2m^* > \phi_B$  where  $\kappa_{\perp}$  is the component of  $\kappa$  normal to the surface,  $m^*$  is the effective mass, and  $\phi_B$  is the barrier height between the conduction bands in Si and SiO<sub>2</sub>).<sup>6</sup> Phonon scattering may be considered to be elastic since the phonon energies are small with respect to the barrier height. However, an electron scattering off another electron may lose up to one-half of its kinetic energy. Hence, electron-electron scattering rapidly thermalizes hot electrons.<sup>7</sup> The escape length of electrons is long for energies near the fermi level but drops rapidly and forms a broad U between 20 Å and 5 Å over the energy range 10 eV to 1000 eV.<sup>8</sup> Escape depths of 25 Å and 12 Å are reported for electrons 5.8 eV and 11 eV above the valence band maximum, respectively.<sup>9,10</sup>

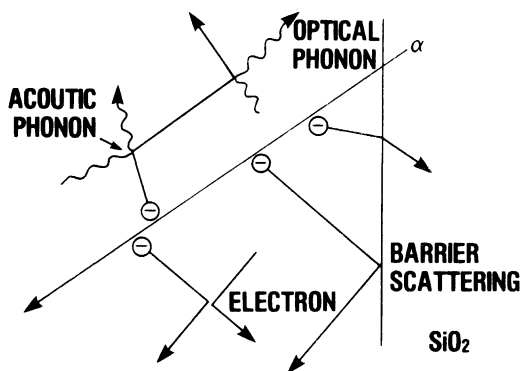


Figure 2: Schematic illustration of scattering process which contributes to small escape depth of electrons from Si.

The ideal situation would be to have electron yield curves as a function of energy for various charged particles of interest incident upon a biased oxidized silicon surface. Unfortunately, we lack such a complete data base, so we shall estimate the yields from data on optically stimulated emission. Figure 3 shows energy distribution curves (EDCs) for three photon energies plotted versus the energy of the states from which the electrons are excited for

photons incident on clean Si.<sup>11</sup> By integrating the EDCs and dividing by the incident photon energy, the yields in terms of electrons emitted per electron volt of incident photon energy are found to be  $6.7 \times 10^{-4}$ ,  $8.9 \times 10^{-4}$ , and  $8.7 \times 10^{-4}$  for photons with energies of 8.6 eV, 10.2 eV, and 11.8 eV, respectively. For lower energy photons, the yields drop precipitously.<sup>6</sup> It is known that the optical absorption length,  $1/\alpha$ , in Si is 80 Å for 12 eV photons.<sup>12</sup> Moreover, the electron escape depth at 11 eV is 12 Å.<sup>10</sup> This implies that one factor limiting the yield is that most of the electrons generated within the bulk of the Si relax via electron-electron scattering. Thus an estimate that a charged particle yields  $10^{-3}$  electrons for every electron-volt of energy lost within 80 Å of the surface is probably an upper bound for emission from silicon into a vacuum.

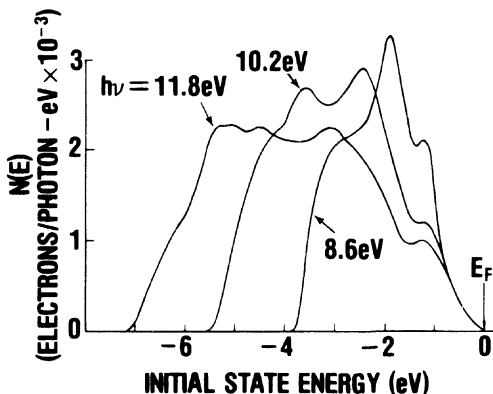


Figure 3: These energy distribution curves give electron yield vs. the energy of the initial state for photons incident on clean Si. (Data from Spicer, ref. 11).

Because the barrier between the conduction band in Si and the conduction band of SiO<sub>2</sub> is  $\sim 0.9$  eV lower than that between the conduction band of silicon and the vacuum level, the yield in the Si/SiO<sub>2</sub> system should be higher than that estimated above.<sup>6,13</sup> The magnitude of the yield increase can be estimated two ways. Callcott measured the effect of applying 0.16 monolayer of Cs to a Si surface. He found that the vacuum barrier was lowered by 1 eV and the photon yield was increased by 2.6 times.<sup>14</sup> Another estimate comes from the observation that for 6 eV photons, Powell reports  $\sim 13$  times higher quantum yield for the Si/SiO<sub>2</sub> system than does Broudy for the Si/vacuum system.<sup>6,13</sup> Since Powell applied a field of  $3 \times 10^6$  V/cm ( $\sim 5\times$  that present in a typical floating gate memory), the barrier between Si and SiO<sub>2</sub> was lowered by 0.45 eV. This implies that

the ratio of the Powell and Broudy results is clearly an overestimate of the yield enhancement. Based on these data, we shall use 10x as a generous estimate of the magnitude of the yield increase between the Si/SiO<sub>2</sub> system and the Si/vacuum system. Our estimate of the yield of electrons emitted over the Si/SiO<sub>2</sub> barrier as a result of an incident ionizing particle is 10<sup>-2</sup> electrons for each eV of energy lost within 80 Å of the Si/SiO<sub>2</sub> interface.

## COLLECTION OF CHARGE GENERATED IN THE SiO<sub>2</sub>

The experimental evidence for collection of charge generated within SiO<sub>2</sub> is much more direct than for charge injected from the Si/SiO<sub>2</sub> interface. Measurements of Srour, Curtis, and Chiu show that the collection efficiency of electron-hole pairs generated by 4-5 keV electrons in SiO<sub>2</sub> varies from very low at low fields to ~20% at 5 x 10<sup>5</sup> V/cm to ~100% at 5 x 10<sup>6</sup> V/cm.<sup>15</sup> From calculations based on these measurements, Ausman and McLean have deduced that one electron pair is created for each 18 eV lost in the SiO<sub>2</sub>.<sup>16</sup> Since typical fields occurring in floating gate memory devices during read or storage operations are 5 x 10<sup>5</sup> V/cm, we shall assume that one pair is created for each 18 eV of energy lost in the oxide and that 20% of the charges created are collected at the electrodes.

## ENERGY DEPOSITED FROM IONIZING RADIATION

Ionizing radiation can be generally separated into that involving massless particles (X-ray, Gamma-rays, etc.) and those which have mass (mesons, electrons, protons, atomic ions, etc.). The absorption cross-sections of the massless particles are quite small and decrease with increasing energy. For example, the  $\kappa_\alpha$  line of Mo occurring at 20.03 keV has a mass absorption coefficient of ~4cm<sup>2</sup>/g.<sup>17</sup> This means that approximately 1mm of Si is required to absorb 63% of the energy of a Mo X-ray beam. Since the cross-section is proportional to the cube of the wavelength, high energy photons lose even less energy per unit of length traveled through a solid. Because of this, it is expected that large fluences of X-rays would be required to transfer significant charge from the gate of floating gate memory.

For particles with mass, the stopping cross-section varies in a systematic way. This is illustrated in Figure 4 where we have plotted calculated energy loss rates in silicon for particles of differing mass using the Bethe-Bloch formalism.<sup>18</sup> As can be seen, for each mass particle, there is a peak in the curve of stopping power vs. energy which shifts to higher energy and becomes larger as the particle mass increases. Because of the log-log nature of the plot shown in Figure 4, it implies that there will be a high density of carriers created at the end of the particle track. This feature is called the Bragg peak.

Since the charge generation rate is maximum for particles with energies in the neighborhood of the Bragg peak, it is illuminating to calculate the charge transferred from a fairly conventional floating gate for two of the particles shown in Figure 4.

Alpha particles are known to be the chief cause of soft errors in volatile memories so their effect will be calculated. The other particle we will consider is an A1 ion, both for itself, since it may be generated as a result of muon capture by Si, and as a proxy for both the Si recoil ions which may be generated in various nuclear reactions and Mg which may also result from muon capture.<sup>19,20</sup>

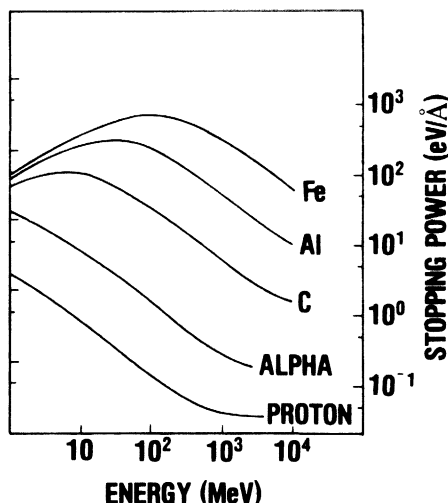


Figure 4: Energy loss rates vs. particle energy for particles with various masses calculated from Bethe-Bloch theory.

The Bragg peak for  $\alpha$ 's in Si occurs for particle energies in the neighborhood of 0.5 MeV. The energy loss rate for  $\alpha$ 's in Si is ~28 eV/Å in this range.<sup>21</sup> The energy loss rate for a compound such

as  $\text{SiO}_2$  can be found from Bragg's rule which postulates the linear additivity of the energy loss cross-sections of the constituents of the compound, viz.

$$\epsilon(\text{X}_m\text{Y}_n) = m \epsilon(\text{x}) + n \epsilon(\text{y})$$

Applying this to  $\text{SiO}_2$  we find that the energy loss rate for alpha particles in  $\text{SiO}_2$  near the Bragg peak is  $\sim 10.6 \text{ eV/\AA}$ .<sup>22</sup> Similar calculations for Al ions give approximate loss rates of  $300 \text{ eV/\AA}$  and  $110 \text{ eV/\AA}$  for Si and  $\text{SiO}_2$ , respectively.

Putting all of this together in the context of Figure 1, we can see that the total charge collected per incident particle should be given by:

$$Q_p = \frac{N_{\text{ox}}(\epsilon)}{18} \int \frac{d_{\text{ox1}}}{\cos\theta} \left( \frac{dE}{dx} \right)_{\text{SiO}_2} dp$$

$$+ Y_{\text{Si-SiO}_2} \frac{\lambda_{\text{esc}}}{\cos\theta} \int \left( \frac{dE}{dx} \right)_{\text{Si}} dp + \left( \frac{dE}{dx} \right)_{\text{Si}} | dp$$

$$+ \frac{\eta_{\text{ox}}(\epsilon)}{18} \int \frac{d_{\text{ox2}}}{\cos\theta} \left( \frac{dE}{dx} \right)_{\text{SiO}_2} dp$$

where  $\eta_{\text{ox}}$  is the field dependent collection efficiency for pairs generated in the oxide,  $d_{\text{ox1}}$  and  $d_{\text{ox2}}$  are the thicknesses of the first and second oxides,  $\lambda_{\text{esc}}$  is the effect escape depth for electrons generated in the Si,  $\theta$  is the angle of the particle path to the normal,  $Y_{\text{Si-SiO}_2}$  is the yield (for normal incidence), and the integrals over path are needed because  $dE/dx$  is a function of energy and hence position.

## SAMPLE CALCULATION

As one example, let's calculate the probability of a floating gate device similar to those in current production being upset by alpha particles emanating from the packaging material. We will assume that the floating gate poly measures  $5\mu \times 14\mu \times 0.4\mu$ , that the transistor gate size is  $5\mu \times 5\mu$ , that the gate oxide and interpoly oxides are both  $1000 \text{ \AA}$  thick and that the field oxide is  $1\mu\text{m}$  thick. We also assume that there is  $2\mu$  of  $\text{SiO}_2$  deposited after the access gate is defined.

Figure 5 shows the alpha particle spectrum measured by Meieran et al.<sup>23</sup> The alpha spectrum is a result of the decay change of thorium and uranium which are present in the alumina which is used for hermetic packaging as trace impurities. For simplicity of calculation, we shall approximate this spectrum as two superimposed step functions. The high energy step begins at  $8.6 \text{ MeV}$  and the lower energy step at  $7 \text{ MeV}$ , the high and low energy steps have the relative weights of 3 to 7. Since it is known that the total emission rate of alumina ranges from 0.1 to

$1.0 \alpha/\text{cm}^2 \cdot \text{hr.}$ , the integral over the approximation will be taken to be  $1 \alpha/\text{cm}^2 \cdot \text{hr.}$

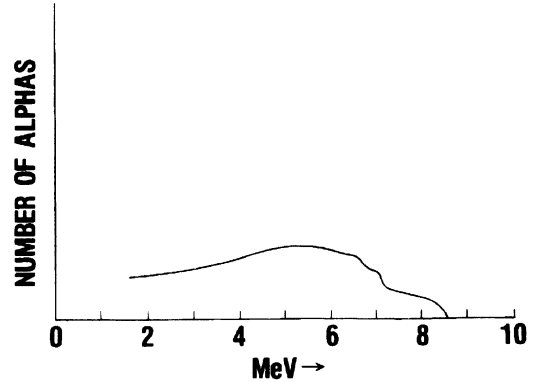


Figure 5: Spectrum of alpha particle emission rate vs. particle energy from an alumina lid. (Data from Meieran et al. ref. 23).

The maximum charge transfer which can occur as a result of a single particle is caused by a particle coming in at such an angle that the complete path length is within the gate oxide. (This requires that  $\theta > 88.85^\circ$ . However,  $\theta < 89.43^\circ$  because for larger angles, the path length of the overglass is so long that no particles get through. Moreover, at  $\theta = 89^\circ$ , the particle energy must be greater than  $6.8 \text{ MeV}$  to penetrate the glass.) If such a particle were to hit a cell so that  $5\mu$  of path length lay within the cell it could lose  $\sim 1.4 \text{ MeV}$ . This implies a transfer of 15,550 electrons. The gate which is under consideration requires  $\sim 450,000$  electrons to charge the state (assuming internal 2 V margin) or about 30 of these pathological alphas. Because the number of pathological alphas needed is  $> 1$ , we can turn to a calculation of the average energy loss/particle.

We make the simplifying assumptions that the fraction of particles lost in the overglass from each of the two step functions contributing to the energy spectrum is given by the ratio of the path length in the overglass to the range of the highest energy particle in the step function, and that the energy loss rate in the effective charge collection region is that for  $1 \text{ MeV}$ . The first assumption causes an underestimation in the particles stopped in the overglass, and the second overestimates the energy contributed to charge generation. Under these assumptions the charge transferred from the floating gate by  $N_0$  alpha particles is given by:

$$Q_t = 2N_0 \sum_i r_i \sum_j \lambda_j \left( \frac{dE}{dx} \right)_j C_j \int_0^{\theta_{\text{max}}} \frac{\sin\theta}{\cos\theta} [1 - \beta_j/\cos\theta] d\theta$$

where  $r_i$  are the relative contribution of the two components in the spectrum;  $\ell_j$  is the effective path length for charge generation;  $C_j$  is the conversion factor from energy loss to collected charges;  $\beta_i$  is the fraction lost in the overglass; and  $\theta_{\max}$  is taken to be the angle whose tangent is the gate length divided by the sum of the gate electrode and gate oxide thicknesses.

From this, one can find that the average alpha particle causes 580 electrons to be transferred from the floating gate. This means that about 750 alpha particles must hit the gate to change its state.

The problem becomes that of finding the probability that at least one cell has been hit 750 times, given that the average cell has been hit  $n$  times. Fortunately, the numbers are large enough that we can invoke the law of large numbers and approximate the distribution as normal with variance  $\sqrt{n}$ . If the array contains  $m$  cells then the probability that at least one cell is hit  $n_{\text{crit}}$  times is given by:

$$Q = \frac{m}{\sqrt{2\pi}} \int_z^{\infty} e^{-t^2/2} dt < \frac{m}{z} \sqrt{2\pi} e^{-z^2/2}$$

$$\text{when } z = (n_{\text{crit}} - n) / \sqrt{n}$$

as long as  $Q < 1$ .<sup>24</sup>

If  $n = 500$ , then  $Q < 1.84 \times 10^{-13}$  for a 16K chip and  $Q < 5.1 \times 10^{-12}$  for a 64K chip. For the chip size and alpha flux assumed, the expected period for the average alpha count per cell to reach 500 is  $7 \times 10^9$  hours. Given the approximations we have made, this probably understates the actual time by about an order of magnitude.

Turning briefly to carriers created by Al ions, we note that very few ions have energies in excess of 3 MeV.<sup>19</sup> Since this energy is below the Bragg peak for Al in Si, the ions stop fairly quickly. Nonetheless, the maximum energy loss rate is  $\sim 120$  eV/Å in SiO<sub>2</sub>. Since the maximum energy of the Al ions is  $\sim 3$  MeV, the maximum charge which would be collected from this ion is about 30,000 electrons which is still small enough that we can use normal statistics. Because of the small cross section for creation of these energetic ions, we can neglect this mode of charge generation for devices operating in normal terrestrial environments.

## SCALING

The effect of scaling on the firm error rate on floating gate devices is interesting because it is very different from that which occurs in volatile memories. If we assume that both lateral and vertical dimensions are scaled by a factor  $\lambda$ , then the storage capacitance decreases as  $\lambda$ . However, since the charge collection is dominated by generation in the oxide, it decreases like  $\lambda^3$ . If the voltage margin decreases like  $\lambda$ , the expected time for upset increases as  $\lambda$ , if the voltage margin is held constant, the expected time for upset increases like  $\lambda^2$ . Thus, scaling should decrease the firm error rate.

## EXPERIMENTAL RESULTS

To verify the theoretical results presented here, floating gate nonvolatile memories have been exposed to two types of radiation: gamma rays, representing massless particles, and alpha particles, representing massed particles. Table I gives the results. The devices tested contained a checkerboard pattern to look for firm error sensitivity for either bias of the floating gate.

As can be seen, no firm errors could be observed. The gamma radiation caused the devices to fail to meet the output leakage specification after 12,000 RAD. Measurement of the threshold of the output transistors showed that the thresholds had dropped from  $\sim 0.7V$  to  $\sim 0V$ .

The alpha particle fluence to which these devices were exposed was approximately that which would be seen after 200,000 years in a dirty package ( $1 \alpha/\text{cm}^2 \cdot \text{hr}$ ) or 2,000,000 years in a clean ( $0.1 \alpha/\text{cm}^2 \cdot \text{hr}$ ). These results are in good agreement with the predictions.

TABLE I

Radiation Type	Energy/quantum	Integrated Surface Flux	#Units Tested	#Firm Errors	Part Type
Gamma Radiation	58.6 keV	12,000 RAD	10	0	X2212
Alpha Radiation	5.3 MeV	$2.6 \times 10^9 \alpha/\text{cm}^2$	5	0	X2816

## SUMMARY

The question of "firm" errors in floating gate non-volatile memories has been treated. A firm error is defined as a change of data occurring as the result of transfer of charge from the floating gate by ionizing radiation. The rate of charge transport by various forms of ionizing radiation is discussed. The case of alpha particles is worked out in some detail as an example. Experimental results of exposure of units to gamma and alpha radiation are shown which support the theoretical predictions. The units in test survived exposure to 12,000 RADs and  $2.6 \times 10^9 \alpha/\text{cm}^2$  without firm errors. The alpha fluence is equivalent to that emitted by a typical ceramic package in about a million years.

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## THE PREDICTION OF TEXTURED POLY FLOATING GATE MEMORY ENDURANCE

By H.A. Richard Wegener &  
Daniel C. Guterman

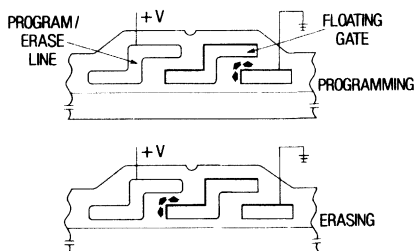
### BACKGROUND

The Textured Poly Floating Gate (TPFG) memory is one of the three major nonvolatile semiconductor memories currently in use. Details of its device theory and its use have appeared in previous publications.<sup>1-4</sup> Its nonvolatile memory cell employs three layers of polysilicon as shown in Figure 1. The most important feature of this cell is its ability to transfer electrons to and from the floating gate through oxide thicknesses of the order of 55 nm to 75 nm, in contrast to other nonvolatile memory technologies that must have dielectrics as thin as 10 nm surrounding their floating gate. The thick dielectric in the TPFG memory cell has proven its advantage in manufacturability and reliability. This advantage is made possible by the presence of a textured surface, whose curved features generate a field enhancement that permits Fowler-Nordheim emission at reasonable voltages. These features have the shape of bumps on the poly surface. The modeling of emission from these surfaces formed the major part of a recent paper.<sup>5</sup> Its results were that these bumps can be approximated by spherical caps on the tip of truncated cones, so that the fields can be found using Laplace's equation in spherical coordinates. From S.E.Ms and T.E.Ms these bumps were known to have a range of sizes. It was found that a simple two-parameter Extreme Value distribution of the cap radii was a sufficient description to get a good fit of model and experimental data over five orders of magnitude of constant current, and eight orders of magnitude of fluence.<sup>5</sup>

### ENDURANCE

Endurance is a characteristic common to all current nonvolatile semiconductor memory technologies. It describes the number of program-erase cycles that a memory device can sustain without

### FLOATING GATE STRUCTURE



0021-1

Figure 1: The nonvolatile part of a NOVDRAM\* cell is shown schematically with the permanently grounded poly 1 at right, the floating gate formed by poly 2 in the middle, and poly 3, also serving as the program/erase line, at the left. To program, poly 2 is coupled capacitively to a positive potential; this results in strong coupling of the floating gate to poly 3, and a high potential between poly 1 and 2. To erase, poly 2 is coupled capacitively to ground; this results in a high potential between the floating gate and poly 3.

failure. In other nonvolatile technologies, the failure modes may involve dielectric breakdown or loss of retention. In TPFG memories, failure is particularly graceful: The addressed bit cannot respond sufficiently to a data change. This is due to the fact that in this technology, the end of endurance is caused by trap-up. Trap-up is the result of the accumulation of trapped negative charge in the dielectric that is caused by the repeated passage of current. The endurance limit is reached when the potential due to this trapped charge grows so large that it suppresses the Fowler-Nordheim tunneling to the extent that insufficient charge is transferred to change the state of the floating gate. The modeling of endurance then simply involves the modeling of the build-up of the negative charge as a function of the number of pulses of Fowler-Nordheim current through the dielectric.

### DESCRIPTION OF ENDURANCE MODEL

A first step is the derivation of the voltage  $V_Q$ , which is the voltage due to the trapped charge that opposed the voltage necessary for tunneling  $V_{TU}$ . The spherical cap model permits the use of Poisson's equation in spherical coordinates. As shown in reference (5),  $V_Q$  is calculated for a charge density defined by a spherical shell with a centroid radius  $R_d$ . An educated guess approximates  $R_d$  with one half of the anode radius  $R_a$ . The

\*NOVDRAM is Xicor's nonvolatile static RAM device.



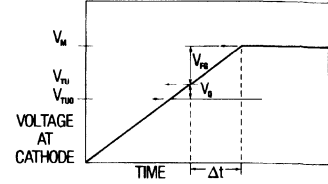
generation of charge density, following the results of previous workers<sup>6,7</sup> is made proportional to fluence (the time integral of current density  $\int J dt$ ) by the trapping ratio  $b$ . This results in

$$V_Q = [\int J dt] (b/K) (R_c^2/R_a) \quad (1)$$

where  $K$  is the dielectric permittivity, and  $R_c$  the radius of the (emitting) cathode surface.

Inspection of Figure 2 will help in understanding what happens during a single (erase) pulse. The ordinate shows the voltage on the program/erase electrode, the abscissa the time during a pulse. The voltage changes linearly with time as shown, at a ramp rate  $r = dV/dt$ . This ramp rate is proportional to the current put out by the charge pump on the chip. As the voltage between floating gate and program/erase electrode increases, a voltage  $V_{TU}$  is reached where Fowler-Nordheim tunneling is initiated. The tunneling current is exactly  $r \times C_{FG}$ , where  $C_{FG}$  is the capacitance of the floating gate. Since the pump current is constant,  $V_{TU}$  will be clamped at a value that keeps the tunnel current constant, but the voltage due to the charge transferred to the floating gate,  $V_{FG}$ , will rise until the ramp is limited at a maximum voltage  $V_M$ . At this point, the tunnel current will fall off rapidly, since any charge transferred will reduce the potential between floating gate and program/erase electrode. In the following analysis, the charge transferred after  $V_M$  is reached will be set to zero. The time,  $\Delta t$ , during which constant current flows through the dielectric is defined by the tunnel voltage  $V_{TU}$  at the beginning, and  $V_M$  at the end. During this time, electrons will be trapped in the dielectric, in proportion to the fluence  $J \times \Delta t$ .

The next pulse will therefore encounter an increased opposing potential  $\Delta V_Q$ , because of the trapped charge generated during the preceding pulse. The ramp voltage at which tunneling starts is now increased by this voltage, the net charge transferred to the floating gate is decreased, and the time  $\Delta t$  during which constant current flows is also decreased. During endurance cycling, the polarities of the pulses are alternated, so that an erase is followed by a program pulse. The (program) ramp following an erase pulse now encounters a potential due to charge transferred during the preceding pulse. This potential adds to that of the new ramp, so that the tunnel voltage is reached sooner, and constant current flows longer until  $V_M$  is reached. In fact, if the structure is symmetrical for both program and erase conditions, the time during which constant current flows is exactly twice that for a single ramp starting with zero charge on the floating gate.



0021-2

Figure 2: The voltage at the floating gate as a function of time is shown for one particular erase pulse. The voltage (due to displacement) changes linearly with time until the tunnel voltage  $V_{TU}$  is reached. Tunneling at constant current clamps the voltage at that value, resulting in a voltage  $\Delta V_{FG}$  due to charge transfer. The trapped charge due to previous erase cycles gives rise to an opposing potential  $V_Q$ .

## MATHEMATICAL MODEL OF SINGLE CELL ENDURANCE

For the purpose of analysis, the floating gate is considered a mosaic of pieces, each containing one emitting bump of cathode radius  $R_{ci}$ . All quantities with subscript  $i$  refer to one such representative piece. Setting the tunnel voltage at  $V_{TU0}$  when no charge exists in the dielectric:

$$V_M - V_{TU0i} = V_{Qi} + V_{FGi} \quad (2)$$

$$\Delta t_i = V_{FGi}/r = (V_M - V_{TU0i} - V_{Qi})/r \quad (3)$$

From Eq(1), the trapped charge in the dielectric after an erase and a program pulse is

$$\Delta Q_i = 2 (b/K) (R_{ci}^2/R_{ai}) J_{FNI} \Delta t_i \quad (4)$$

This can be expressed as the rate of charge trapping per program/erase cycle  $n$ :

$$dV_{Qi}/dn = \alpha_i (V_M - V_{TU0i} - V_{Qi}), \text{ where} \quad (5)$$

$$\alpha_i = 2 (b/K) (R_{ci}^2/R_{ai}) J_{FNI}/r \quad (6)$$

Integrating Eq(5), and setting  $V_{Qi}$  equal to zero at  $n = 0$ , results in

$$\ln [(V_M - V_{TU0i})/(V_M - V_{TU0i} - V_{Qi})] = \alpha_i n \quad (7)$$

Substituting Eq(2) into Eq(7) and solving for  $V_{FGi}$

$$V_{FGi} = (V_M - V_{TU0i}) \exp (-\alpha_i n) \quad (8)$$

The transition from the individual bump mosaic pieces to the full floating gate comes from the argument that the floating gate voltage is really the sum of the charge contributions  $Q_i$  from small amounts of current  $I_i$  emitted by all bumps, divided by the floating gate capacitance  $C_{FG}$ :

$$V_{FG} = \Sigma Q_i / C_{FG} = [\Sigma I_i \Delta t_i] / C_{FG} \quad (9)$$

$$I_i = 4\pi R_{ci}^2 (s/4) J_{FNI} \quad (10)$$

the Fowler-Nordheim  $J_{FNi}$  current is

$$J_{FNi} = A E_{ci}^2 \exp(-B/E_{ci}), \quad (11)$$

the field at the emitting bump is

$$E_{ci} = (-V_{TUi} + V_{Qi})/R_{ci}[1 - (R_{ci}/R_{ai})] \quad (12)$$

the cathode radius

$$R_{ci} = R_M - BB [\ln - \ln(i - 0.5)/G] \quad (13)$$

Summing all bumps  $i$  from 1 to the total number of bumps  $G$  results in the complete expression for the dependence of the floating gate voltage due to tunneled electrons  $V_{FG}$ , on the number of endurance cycles  $n$ :

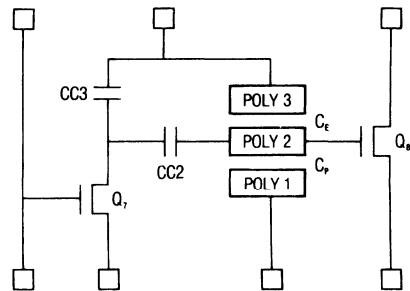
$$V_{FG} = (1/r C_{FG}) \sum 4\pi R_{ci}^2 (s/4) J_{FNi} \times (V_M - V_{TUi}) \exp(-\alpha_i n) \quad (14)$$

The quantities after  $J_{FNi}$  are the result of replacing  $\Delta t_i$  in Eq(9) by Eqs(3) and (8). It now remains to define the end of endurance. Clearly, it arrives when the floating gate voltage is insufficient to establish the required logic level. The end of single cell endurance ( $n = N_c$ ) occurs when the floating gate voltage reaches a defined value ( $V_{FG} = V_{FGM}$ ) that is the boundary of that level.

## SINGLE CELL ENDURANCE DATA

The test pattern used to characterize endurance is the nonvolatile part of a Xicor NOVRAM cell shown in Figure 3. The dimensions of the test cell are identical to those in a NOVRAM memory array. The advantage of this cell is that all voltages can be applied directly to this cell. Cycling is achieved by applying a ramp between ground and  $V_M$ .  $V_{FG}$  is read out by applying the same control voltage sweep simultaneously to ground,  $V_M$  and P/E control. This couples to the floating gate and when a voltage equal and opposite to  $V_{FG}$  is reached, the (floating) gate on the sense transistor will indicate zero charge. Upon increasing the control voltage sufficiently the floating gate potential is increased by the threshold voltage of the transistor, turning on the sense line. This value of the control gate is then recorded, generating the plot shown in Figure 4. The ordinate shows the value of the control voltage necessary to turn on the sense transistor. Since  $V_{FG}$  is positive in the erase state, a negative control voltage must be applied. Therefore, the lower branch of the window plot represents the erase state. When  $V_{FG}$  approaches the threshold voltage of the transistor, its reaction becomes indeterminate, and the limit of the endurance of the cell is reached. ( $n = N_c$  when  $V_{FG} = V_T$ ). This situation is

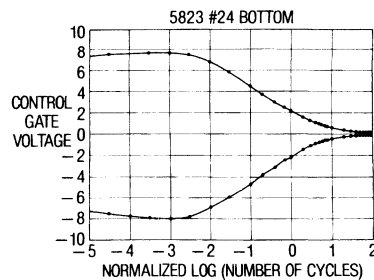
indicated when the applied control voltage is exactly zero. Inspection of Figure 4 shows that the end of the endurance for that particular cell occurred at a number of cycles normalized to a value of 100. The same factor of normalization was applied to all data quoted here in order to prevent possible confusion with results from individual products, or with published specifications.



0021-3

Figure 3: This shows the circuit schematic of the nonvolatile part of a NOVRAM cell. Two transistors are shown in addition to the elements in Figure 1. Transistor  $Q_7$  controls the access to the junction used for capacitive steering of write and erase operations, and transistor  $Q_8$  senses the voltage on the floating gate.  $V_{FG}$  can be measured by turning  $Q_7$  on hard, and finding the control voltage that must be supplied simultaneously to poly 1, poly 3, and capacitor  $CC_2$ , in order to cause a specified current to pass through  $Q_8$ .

## NOVRAM CELL ENDURANCE DATA



0021-4

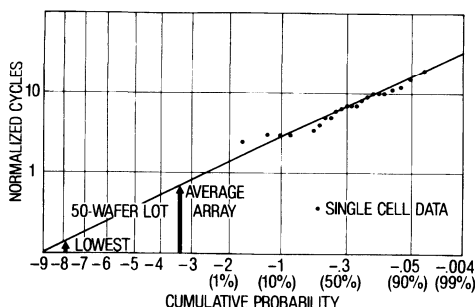
Figure 4: This is a plot of the charge transferred to the floating gate of a single NOVRAM cell as a function of the logarithm of the number of program/erase cycles. The actual floating gate voltage is the negative value of the control voltage minus the threshold voltage of  $Q_8$ .

## RELATIONSHIP OF SINGLE CELL DATA TO LOT ENDURANCE

The number of program-erase cycles at a control voltage of zero was determined for a number of single cell structures from the same wafer lot. The results were plotted on log normal probability paper.

The results can be seen on Figure 5. Careful reading of the abscissa will establish its relationship with the usual chart. In effect, the scale has been extended on the low probability side of the distribution, and for simplicity of notation, the cumulative probabilities have been marked as their base ten logarithms. In a few selected locations near the right hand side, the equivalent percentage values were given in brackets. The single cell data points are on either side of the 50% line of the chart. The slope of the best fit straight line defines the dispersion of the distribution.

#### RELATIONSHIP OF SINGLE CELL DATA TO LOT ENDURANCE



0021-5

Figure 5: This shows the Log Normal probability plot of individual single cell endurance data. The right half of the plot is quite standard, as marked by typical cumulative percentages. The left half represents an extension of the standard chart to much lower probabilities, in order to permit predictions for specific members of a much larger population.

In order to relate these results to the endurance of a commercial lot of NOVRAMs, the definition of the endurance of an integrated circuit with an array of memory cells should be recalled. This definition states that the limit of the endurance of a chip is reached when the first cell fails, after having sustained the same number of data changes as every other cell on that chip. If that chip has 1024 memory cells, then the cell with the lowest endurance limit of these 1024 cells defines the endurance of that chip. The cumulative probability for this is  $1/1024$ . Any chip with 1024 cells can be expected to have that endurance. The number of cycles at the cumulative probability of  $1/1024$  therefore represents the average endurance of a chip from a given lot. The lowest endurance on a wafer of chips is caused by the cell with the lowest endurance on that wafer. If there are, say, 850 chips per wafer, then the cumulative probability of this endurance limit is  $1/(1024 \times 850)$ . Looking now at a full 50 wafer lot, the lowest endurance of that lot has a cumulative probability of  $1/(1024 \times 850 \times 50)$ . The plotting of ranked data on probability paper requires "plotting posi-

tions" that result in about half the calculated cumulative probability values<sup>8</sup> for the lowest value used. In order to be consistent with the plotted data points, the cumulative probability for the average chip endurance from the 50 wafer lot is 0.0005, and this is indicated by an arrow of Figure 5. Similarly, the lowest possible chip endurance on that wafer lot is  $1E-8$ .

## COMPARISON OF SINGLE CELL PROJECTION WITH COMMERCIAL LOT DATA

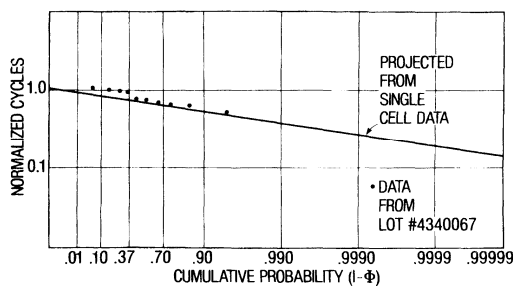
The endurance of individual arrays from a commercial lot can be described by a statistical distribution and its parameters. Since the endurance of an array is determined by the lowest endurance of a fixed number of cells, an Extreme Value distribution describes the distribution of the lowest endurances of all the arrays, and therefore, of the arrays within a lot.<sup>9</sup> This applies regardless of the distribution of the endurances of individual cells within the same array. It is an empirical fact that it is the logarithm of the number of cycles that has the Extreme Value distribution,<sup>10</sup> very similar to the Log Normal distribution frequently found for data from electronic devices. Lot data can be handled simply by the use of Extreme Value probability paper. Available charts are designed for maximum extreme values. For minimum extreme values, such as the lowest endurance of an array, these charts can be used by substituting the complement for the cumulative probability of an observation in order to determine the plotting position. Instead of  $\phi$ ,  $(1 - \phi)$  is used to determine the abscissa. Figure 6 is based on these considerations.

The abscissa is labeled by the complement values, which results in the reversal of the slopes of the straight line describing the distribution. The ordinate is (just as Figure 4) in terms of the logarithm of the normalized endurance. Since the distribution is described by a straight line in this coordinate system, it requires only two points to define its locus. These two points were determined in the previous section: the endurance of the average array, and the minimum endurance of the lot. The difference from Figure 5 (aside from the distribution function) is that the definitions of the cumulative probability values have changed. In terms of an individual cell, the cumulative probability of the endurance of an array is related to  $1/1024$ ; in terms of the array, the cumulative probability is the expected average of individual array units. For the (maximum) Extreme Value distribution this is 0.57; since the shape of the

distribution has not changed, the use of the complement does not apply and the value of the (log of) endurance on Figure 5 at the larger arrow is entered on Figure 6 at  $\phi = 0.57$ . Similarly, the minimum endurance of an array from a 50 wafer lot is now associated with a cumulative probability of  $0.5/(50 \times 850)$  a value increased by a factor of 1024 over the corresponding single cell value (see preceding section). The cumulative probability for the minimum (array) endurance of a lot is therefore  $1.2E-5$ , to be plotted at the 0.99999 position. A straight line drawn through this point and the array average establishes the projected distribution of array endurences. This graphical technique of deriving lot endurences from single cell data will be supplemented by an equivalent mathematical approach in the Appendix.

How good is the fit to actual data? Endurances from a typical monitor of that general time slot in NOVRAM production are shown on Figure 6. The fit is not fortuitous: there are dozens of lot data with almost identical slopes over a range of roughly a factor of 0.5 to 2. Confidence limits (95%) from the single cell data permit a scatter twice as large.

#### ENDURANCE FROM SINGLE CELL VS. COMMERCIAL LOT DATA



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Figure 6: This is a Log Extreme Value probability plot of the endurance of a lot of X2212 NOVRAMs. The points are measured values, the straight line represents endurences predicted from the single cell data shown in Figure 5.

## CONSTANT CURRENT TESTING

The determination of endurance is a very time consuming process. In single cell data taking, typically tens to hundreds of millions of cycles are required. This routinely takes on the order of days to accomplish. For product endurance prediction, about twenty cells are needed, requiring simultaneous testing for any semblance of monitoring effi-

ciency. A much more rapid method of evaluation has been in use for some time. It depends on the observation of the time necessary to reach some predetermined tunnel voltage, when a constant current is forced through the test structure. An empirical factor correlates observed time with observed product endurance. Test times are on the order of ten to ten thousand seconds, depending on conditions used. Inspection of Eq(8) explains the reason for this. The time  $\Delta t$  during which constant current flows is proportional to  $V_{FG}$  (Eq(3)). It is therefore exponentially decreasing with the number of write-erase cycles. Since the data ramp takes the same amount of time, whether current flows through the dielectric or not, the time consumed increases linearly with the number of cycles, while the limiting process decreases exponentially. A constant current test adds the periods of current flow without pauses, reaching the condition for the trap-up limit of endurance in a minimum of time.

## MATHEMATICAL RELATIONSHIP BETWEEN ENDURANCE AND CONSTANT CURRENT DATA

The work described in reference (5) proved that the constant current data can be modeled by bumps whose size have the proper distribution. Since this requires the addition of the contributions of thousands of bumps, the number of different bump radii necessary for a good fit was studied. It was found that at low fluences, a large number was necessary, but after a sufficient amount of charge has passed through the dielectric, the contributions from different bumps had nearly equalized, so that only a few bump radii were a sufficient description. After high fluences, a single bump, representative of the maximum of the distribution of radii, could predict the tunnel voltage necessary to maintain a constant forced current. Since the end of endurance is brought about by high tunnel voltages after large fluences, this condition applies very well and is used in the following analysis. When, in Eq(14),  $R_{ci}$  is replaced by  $R_M$ , the summation sign is replaced by a multiplication by  $G$ . Then the factor to the left of, and including,  $J_{FNI}$  becomes  $1/(r \times C_{FG})$ . But  $I = r \times C_{FG}$ , so that, when  $R_{ci}$  becomes  $R_M$ ,

$$N_C = (1/\alpha_M) \ln[(V_M - V_{TUOM})/V_{FGM}] \quad (15)$$

Substituting  $r \times \Delta t$  (see Eq(3)) for the voltage term in parentheses in Eq(5), multiplying by  $dn$  and integrating results in

$$\int dV_{Qi} = \alpha_i r \int \Delta t_i dn \quad (16)$$

The integral of  $\Delta t$  with respect to the number of cycles is, of course the total time of constant current flow through the dielectric. At the endurance limit,  $V_{Qfi} = V_M - V_{TUO_i} - V_{FGM_i}$ , and the integral of time intervals is equal to the total time of constant current flow to the instant of the end of endurance,  $t_{N_i}$ . Again invoking the asymptotic limit of all  $R_{ci}$ 's becoming  $R_M$ ,

$$t_N = (V_M - V_{TUOM} - V_{FGM})/r \alpha_M \quad (17)$$

Solving Eq(17) for  $\alpha_M$  and substituting in Eq(15) results in the expression for endurance as calculated from constant current data

$$N_C = [r t_N / (V_M - V_{TUOM} - V_{FGM})] \times \ln[(V_M - V_{TUOM})/V_{FGM}] \quad (18)$$

Conversely, the elapsed time at constant current  $t_N$  equivalent to endurance  $N_C$  is obtained by interchanging those two quantities in Eq(18). An estimate of the time advantage is obtained by realizing that in cycling, a minimum time of  $2 \times V_M/r$  is consumed per cycle. Since typically, some time, both analog and digital, is spent in the transition from programming to erasing, this minimum time is doubled.

Therefore the elapsed time to reach the end of endurance by cycling  $t_{CC}$ , is closer to

$$t_{CC} = 4 N_C V_M/r \quad (19)$$

Substituting pertinent values, one can find that  $t_N$  is approximately  $t_{CC}/50$ .

## EXPERIMENTAL CORRELATION OF CONSTANT CURRENT WITH CYCLING DATA

Textured poly capacitor test patterns from the same wafers that had been used to obtain the single cell cycling data displayed in Figure 5 were subjected to forced constant current conditions, and their tunnel voltages were recorded as a function of time. An automated test system exists to perform this test on a routine basis. When tunnel voltage was plotted vs time, the data for ten such structures

resulted in Figure 7. According to Eq(17), when  $V_{Qf} = V_{TU} - V_{TUO} = V_M - V_{TUO} - V_{FGM}$ , then the end of endurance is reached. This condition is indicated by the horizontal line at that voltage. The time  $t_N$  to reach that can be read off the graph and converted into equivalent cycles by Eq(18). These endurences can then be plotted on a graph similar to that used in Figure 6.

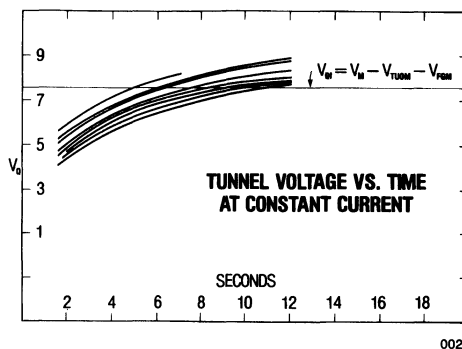
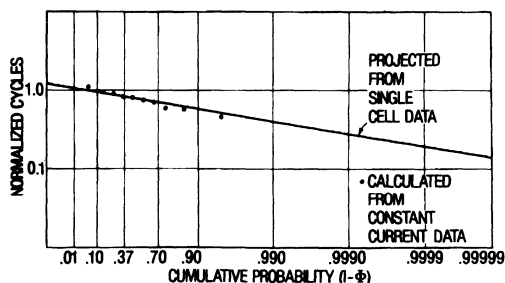


Figure 7: This is a record of tunnel voltage (expressed as trap-up voltage) vs time. The end of endurance is reached when the tunnel voltage reaches a value  $V_{Qf}$ . The time associated with that voltage can be read off this chart.

The area of the constant current structure was eight hundred times that of the single cell capacitors. Since its behavior is dominated by the highest current features, it is set equal to the endurance of the 400th lowest cell. This has been chosen as the average endurance of the lot of constant current devices. The fit in Figure 8 indicates good correlation between the two methods of determining endurance. This means that product endurences can be legitimately predicted from constant current data. Test times on the order of ten seconds are short enough for the E-test stage of wafer evaluation: they clearly permit the prediction of product endurance. But as increasing knowledge leads to an improvement in endurance, this time is expected to increase by several orders of magnitude. Eq(17) indicates a predictable acceleration technique. All that is needed is to increase the level of constant current, measure time to reach the voltage of the endurance limit, and insert that value onto Eq(17). In addition, the value of  $r$  must be adjusted to reflect the new current value, according to  $r = I/C_{FG}$ . Finally, a secondary adjustment must be made to the value of  $V_{TUOM}$  by calculation. Another method would be to increase the area of the constant current device to bring more low endurance features into play.

## ENDURANCE FROM SINGLE CELL VS. CONSTANT CURRENT DATA



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Figure 8: This is again a Log Extreme Value probability plot. The points are those calculated from the times measured via Figure 7. The straight line represents the endurance predicted from the single cell data in Figure 5.

## SUMMARY

We have described a coherent body of understanding and data that permits the prediction of product endurance, and the use of devices for accelerated testing, from first principle device models. This fortunate circumstance arises from the advantageous technological feature of textured poly tunneling, namely that there is one, and only one, mechanism that is prevalent in determining the end of endurance.

This one mechanism is trap-up, the build-up of negative charge in the dielectric in proportion to the fluence of the tunnel current. The model for window closure and for single cell endurance flows naturally from this concept. The predictability of accelerated tests is also the result of this single unifying mechanism. The relationship with product endurance follows from basic statistical considerations.

## ACKNOWLEDGMENTS

The authors would like to express their appreciation for the general support given to this work by Xicor management and staff. In particular, thanks are due to Yupin K. Fong and Kurt B. Raab for their effective help in the software development and for the performance of the measurements of the individual test structures.

## APPENDIX

### Mathematical Formulation for Lot Endurance from Single Cell Data

The approach taken here is simply to translate the graphical operations performed in preceding sections into symbols. Underlying its simplicity are the operations leading to the design of probability papers. They begin by translating the cumulative distribution of a variable into a linear function of that variable. The single cell endurences have the form:

$$\phi_C = 1/2 + (1/2) \{1 - \exp [\text{BELOW}]\} \quad (\text{A1})$$

$$\text{BELOW} = [-(\pi/2) (\ln N_C - \ln \bar{N}_C)^2 / \sigma^2]$$

where  $\phi_C$  is the cumulative probability of single cell endurance  $N_C$ ,  $\bar{N}_C$  is the average cell endurance, and  $\sigma$  its standard deviation. The function form chosen is an approximation<sup>11</sup> to the normal distribution function. It is chosen here because it could be inverted most simply into a form linear in  $N_C$ , since the intent is to make the operations more transparent to the reader. The same operations could be performed by using the exact integral formulation of the cumulative probability of the normal distribution. Expressing Eq(A1) as a linear function of  $\ln N_C$

$$\ln N_C = \ln \bar{N}_C - \sigma \times F_C, \text{ where} \quad (\text{A2})$$

$$F_C = \{(-\pi/2) \ln [\phi_C (1 - \phi_C)]\}^{1/2} \quad (\text{A3})$$

Eq(A2) relates any single cell endurance  $N_C$  to its probability factor  $F_C$  and via Eq(A3), to its cumulative probability  $\phi_C$ . The lowest endurance  $N_{CA}$  expected from an array of cells is defined by

$$\ln N_{CA} = \ln \bar{N}_C - \sigma \times F_{CA}, \text{ where} \quad (\text{A4})$$

$$\phi_{CA} = [1/(\# \text{ cells/array})]$$

An equation like Eq(A4) can be set up for the minimum endurance of a wafer lot  $N_{CM}$ , where  $\phi_{CM} = [1/(\# \text{ cells/wafer lot})]$ . For the lot endurences, an equivalent scheme is set up:

$$\ln N_A = \ln \bar{N}_A - (1/\alpha) \times F_A, \text{ where} \quad (\text{A5})$$

$$F_A = \ln [-\ln (1 - \phi_A)] \quad (\text{A6})$$

Now  $N_A$  is the endurance of an array (or chip),  $\bar{N}_A$  is the modal endurance of the lot, and  $F_A$  is the probability factor derived from the Extreme Value distribution. Incidentally,  $F_A$  is exact and not an

approximation. In analogy to Eq(A4), the average array endurance  $\bar{N}_{AA}$  has the form

$$\ln \bar{N}_{AA} = \ln \bar{N}_A - (1/\alpha) \times F_{AA} \quad (A7)$$

The value of  $\phi_{AA}$  for the average of the distribution must be 0.43, in order that its complement becomes 0.57, the locus of the average of the (maximum) Extreme Value distribution. The minimum endurance of the lot has the same subscript as Eq(A7), except that subscript AM is substituted for AA. The probability factor  $F_{AM}$  is based on  $\phi_{AM} = [1/(\# \text{ arrays/wafer lot})]$ . It will be realized that  $N_{CA} = N_{AA}$ , and  $N_{CM} = N_{AM}$ . Therefore two simultaneous equations can be solved for  $\bar{N}_A$  (the lot average), and  $1/\alpha$  (the lot dispersion), in terms of single cell parameters:

$$1/\alpha = \sigma \times [(F_{CM} - F_{CA})/(F_{AM} - F_{AA})], \quad (A8)$$

and

$$\ln \bar{N}_A = \ln \bar{N}_C - \sigma \times [(F_{CA} \times F_{AM} - F_{AA} \times F_{CM})/(F_{AM} - F_{AA})] \quad (A9)$$

Expressing Eq(A5) in terms of single cell parameters results in

$$\ln N_A = \ln \bar{N}_C - \sigma \times \{ [F_{CA}(F_{AM} - F_A) - F_{CA}(F_{AA} - F_A)] / (F_{AM} - F_{AA}) \} \quad (A10)$$

In this way, the individual endurences expected from a commercial lot  $N_A$  can be predicted from the size of the lot tested, which determines  $F_A$ , the single cell constants  $\bar{N}_C$  and  $\sigma$ , and chip size details of that product, which convert the F's with double subscripts into specific constants.

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# COMPARISON AND TRENDS IN TODAY'S DOMINANT E<sup>2</sup> TECHNOLOGIES

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## ABSTRACT

This paper reviews the three dominant E<sup>2</sup> technologies today, namely the two floating gate approaches of thin tunnel oxide and oxide on textured poly and the dual dielectric approach of MNOS. It evaluates each approach with respect to cell design, operation, manufacturability, compatibility with established process technologies and reliability. It follows with a comparison of the technologies in the areas of development entry cost, scaling and reliability. After a review of the market place, this paper concludes with a projection of the requirements of E<sup>2</sup> technologies to support full function, commodity E<sup>2</sup> memories (E<sup>2</sup>PROM) as well as low cost micro-controllers and ASIC (Application Specific Integrated Circuits).

## INTRODUCTION

Electrically alterable nonvolatile semiconductor memory has been an area of active research for many years, with the promise that it will be the ultimate silicon memory. The first floating gate memory was proposed in 1967<sup>1</sup> and MNOS memories were reported at about the same time.<sup>2</sup> In 1980, the first 16K E<sup>2</sup>PROMs using MNOS<sup>3</sup> as well as floating gate technologies on FLOTOX<sup>4</sup> were reported, while textured poly E<sup>2</sup>PROMs were reported in 1983.<sup>5</sup> However, after all these years of development in the laboratory and volume manufacturing, E<sup>2</sup>PROMs have yet to become a high volume, widely used memory component compared to EPROMs, the closest equivalent memory with lower functionality. There are many reasons given for the limited growth, ranging from the higher cost of E<sup>2</sup>PROM based products to poorly understood reliability of

these components. In this paper, we will focus on the technology factors by comparing the three dominant E<sup>2</sup> technologies to date, and giving our own viewpoint on the development in the market place.

## DESCRIPTION OF TECHNOLOGIES

### FLOTOX (FLOating gate Tunnel OXide)

The cross sectional structure of a FLOTOX cell is shown in Figure 1a. It consists of a floating gate transistor with a thin oxide grown over the drain region. The floating gate is surrounded completely by high quality silicon dioxide, giving its superior retention characteristics. Programming (electrons into floating gate) is achieved by taking the control gate to high voltage while erase (electrons out of floating gate) is achieved by grounding the control gate and taking the drain to high voltage. Because the program and erase coupling conditions are different, they have different design considerations. Electron transfer is through Fowler-Nordheim tunneling mechanism using electric field higher than 10 MV/cm. The IV slope of tunneling is so steep that there is insignificant tunneling under normal read conditions for more than ten years. In order for the cell to properly operate in an array, it has to be isolated by a select transistor. Two cycles are required to load the correct data. All cells in a byte are first programmed, and then selected cells are erased using the drain for data control. The manufacturing process for FLOTOX is an extension of the EPROM technology, which in turn is an extension of the standard single poly silicon gate technology. The critical step in the process is the growth of high quality thin (<12 nm) tunnel oxide. For reliability, the dominant failure mechanism for FLOTOX is the breakdown of the tunnel oxide due to defects under the high field stress of the program/erase cycles, resulting in a leaky oxide.<sup>6</sup>

### Textured Poly Cell

The cross sectional structure of a textured poly cell is shown in Figure 1b. It consists of 3 layers of poly with overlap forming three transistors in series. The floating gate transistor is in the middle formed by poly 2. Again, the floating gate is surrounded by silicon dioxide for high retention. Programming is

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## FLOTOX DEVICE STRUCTURE

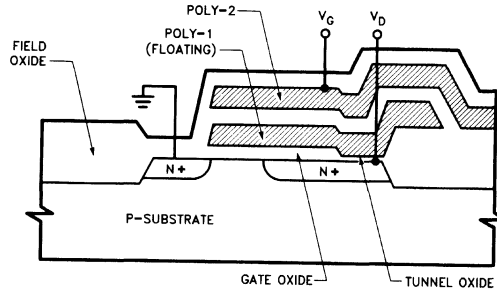
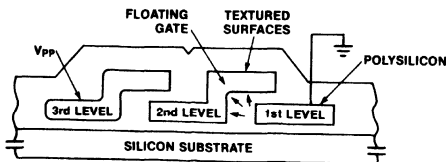


Figure 1a: Cross sectional structure of a FLOTOX memory cell.

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achieved by electrons tunneling from poly 1 to poly 2 and erase is achieved by electrons tunneling from poly 2 to poly 3. The program and erase coupling again is different. The poly 3 is taken to high voltage in both cases, and the element which tunnels is determined by the voltage applied from the drain and coupled to the floating gate through the channel region. The final data state is determined by the data state on the drain: this is a "direct write" cell with no need to clear before write as is required in the FLOTOX cell. This is possible because there are two active tunnel elements. The tunneling process is fundamentally still Fowler-Nordheim tunneling, with enhancement of local electric field due to the geometrical effect of fine texture at the poly surface. The electric field enhancement factor is in the range of 3 to 5, allowing much thicker oxides (60 nm to 100 nm) to be used. No extra transistor is required in an array since the poly 3 transistor serves the function of select transistor, giving a much more compact cell layout. The manufacturing process for textured poly is again an extension of the EPROM process with the addition of an extra layer of poly. The critical process step in this process is the growth of the tunnel oxide on poly. Because thicker oxides are used, oxide breakdown is less of a problem compared to FLOTOX. The dominant failure mechanism in a textured poly cell is electron trapping which results in memory window closure.<sup>7</sup>



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Figure 1b: Cross sectional structure of a textured poly memory cell.

## MNOS (Metal Nitride Oxide Silicon) Cell

The cross sectional structure of a MNOS cell is shown in Figure 1c. It consists of a single transistor with a dielectric stack of silicon nitride on top of a thin layer of oxide (1.5 nm to 2.0 nm) on silicon. Typically, the transistor resides in a well so that the channel potential can be controlled. Unlike the floating gate, charge is stored in discrete traps in the bulk of nitride. Because of the discrete nature of traps, charge transfer has to occur over the large area of the channel region. This is different from floating gate devices where charge transfer can occur over a small area removed from the channel region. On the other hand, any dielectric defect fatal to floating gates will only discharge local traps in MNOS. Programming is achieved by applying high voltage to the top gate whereas erase can be achieved by grounding the top gate and taking the well to high voltage. The program and erase coupling is symmetrical. Because of the very thin oxide, charge is being leaked off continuously due to the internal field, giving an ever diminishing window. In an array, select transistor is required to operate the cell properly. The select transistor may be separate<sup>3</sup> or integrated<sup>8</sup> in which case a more compact cell layout can be realized. Two cycles are again required to load the correct data. Furthermore, the well potential has to be controlled during data change, which makes the array operation more complex. The manufacturing process for MNOS is an extension of single poly silicon gate technology. The memory transistor is fabricated after the first poly periphery transistors are formed to maintain the integrity of the dual dielectric storage element. The

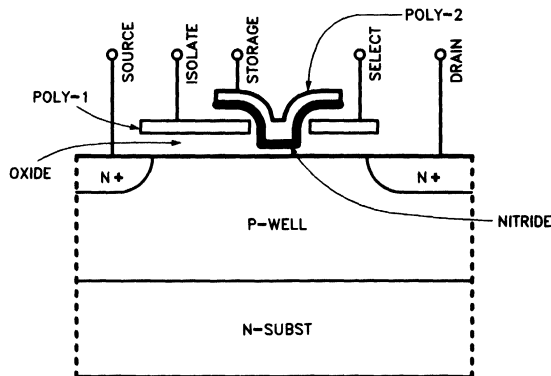


Figure 1c: Cross sectional structure of a MNOS memory cell.<sup>8</sup>

important steps include thin oxide growth, nitride deposition and post nitride temperature cycles. The biggest reliability concern is cell retention and its degradation with cycling.<sup>9</sup>

## COMPARISON

The three different approaches have their technical merit and difficulties. Any one of these technologies can be made to work if they are given sufficient effort and focus. As a result, other considerations ranging from "comfort factors" to compatibility with available technologies tend to determine the choice.

## Development Entry Cost

Entry cost is the amount of extra effort required to bring up a new technology. To an EPROM manufacturer, it is relatively easy to take the FLOTOX approach. The cell concept is simple and the tunnel oxide process is a straight forward variation of a standard high quality oxide furnace cycle. This is why the majority of companies have opted for this approach for their E<sup>2</sup> effort. The textured poly approach, on the other hand, depends on a tunneling process which is not generally understood and is believed to require tighter process control. The cell concept is more complex and the use of three layers of poly imply higher wafer cost. These factors have limited the popularity of developing this approach. Finally, MNOS approach requires the mastering of a number of difficult process steps. The growth and control of the ultra thin oxide, as well as the quality of nitride are critical issues. As a result, despite gaining initial momentum, MNOS has not achieved dominance as an E<sup>2</sup> technology.

## Scaling

There are many factors that determine the size of a memory cell, and generally cell design represents finding the optimum compromise of a number of tradeoffs. Furthermore, as these technologies approach fundamental physical or practical material limits, scaling will become increasingly difficult. For FLOTOX, there is large area requirement for layout of the two transistors plus the tunnel oxide area, dictated by minimum design rules. The select transistor is limited by high voltage. Given the high oxide capacitance of thin tunnel oxide, large poly to poly area is required for the sense transistor. Scaling of the tunnel dielectric is also limited by direct tunneling at 6 nm and yield and reliability issues at 8 nm to 10 nm. Typically, relatively high voltages (15V to 20V) are required to operate the cell. As a result, FLOTOX cell does not scale well.

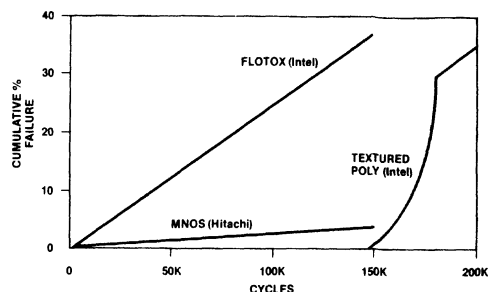
In the case of textured poly, the three poly layers are integrated resulting in a compact layout. Cell size is limited more by lithographic registration of poly layers than by ability to resolve space between poly lines as is the case with FLOTOX. Furthermore, the thick tunnel oxide requires smaller coupling capacitor area to give the required coupling. Given the same performance and reliability requirement, it is estimated that a textured poly cell is about a factor of two smaller compared to a FLOTOX cell for a given generation of technology. Textured poly does require higher operating voltage (>20V) and thus needs a high voltage technology to support it. Finally, scaling of the poly oxide involves more than thinning down the oxide as the field enhancement factor changes with oxide thickness.

The basic MNOS memory cell can be very small and highly scaleable. The select transistors, wheth-

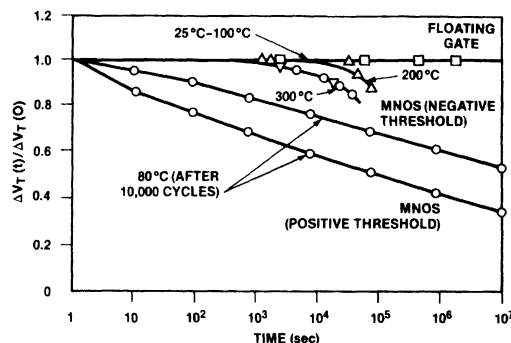
er separated<sup>3</sup> or integrated,<sup>8</sup> will limit scaling. However, in either case, the cell size is better than FLOTOX, and competitive with triple poly for a given generation of technology. One major problem is the requirement of well voltage control. Full byte function is only possible with separate well, giving a large effective cell size. Page function<sup>8</sup> can be used to partially circumvent the well problem but limits endurance. For oxide thicknesses, there is little or no room to scale the ultra thin tunnel oxide, so most of the emphasis has been on scaling the nitride. Charge leakage from the scaled nitride to top gate has been solved by oxidizing the nitride to give a MONOS stack. Low program and erase voltages have been demonstrated at the expense of smaller operating window.

## Reliability

One general problem for E<sup>2</sup>PROM is the limited information on the reliability of the technologies due to sample size or correlation problems. For floating gate technologies, there is no intrinsic problem with data retention, and because the technologies are designed to handle high voltage, there is very low failure rate due to normal 5V operation. Reliability problems occur during program and erase cycles in part because very high voltages are used. For FLOTOX, there is random single bit failure due to oxide defect resulting in a leaky oxide that loses charge over time (see Figure 2). For textured poly, the average electric field across the tunnel oxide is 3 to 5 times lower compared to FLOTOX. As a result, oxide breakdown failure is reduced significantly. On the other hand, there are more electron traps in the oxide, and the impact of electron trapping is magnified by the 3 to 5 times field enhancement factor. Consequently, electron trapping is the dominant failure mechanism, showing up as a failure to program or erase. The failure can be projected real time with margining techniques and since trapping is an intrinsic property, failure probability can be easily projected. In MNOS, charge retention is the dominant reliability issue (see Figure 3). The charge loss process is time dependent, resulting in continuous loss of cell margin and performance. The degradation based on short term data is difficult to predict. The ultra thin oxide is stressed by electric field comparable to FLOTOX and retention is further degraded with program and erase cycles. So far, wide variation in retention and endurance are being reported based on limited sampling.<sup>9</sup>



0022-4  
Figure 2: Endurance of 3 E<sup>2</sup> Technologies: FLOTOX and textured poly processed at Intel (16K arrays), MNOS data from Hitachi (prorated to 16K).



0022-5  
Figure 3: Data Retention: Floating gate, no intrinsic charge retention problem; MNOS, continuous charge loss and window closure tending to become worse after cycling.

## THE MARKET PLACE

Though E<sup>2</sup>PROMs have been available for the last five years, their usage has not grown to the volumes projected. A host of new and established companies have become active in the field, but lack of technology and product feature standardization, together with high cost and reliability concerns have limited the growth in the market place. The major issues for 16K have been 5V only, address/data latch vs no latch, ready/busy vs data polling, 24 pin vs 28 pin, 1 ms vs 10 ms program, self timed vs user timed, with and without V<sub>CC</sub> lockout and 10K vs 1 Million cycles endurance. Byte vs page function and page size are issues at 64K density level. In addition, one can choose oxynitride vs oxide for FLOTOX, textured poly vs FLOTOX for floating gate, and MNOS vs floating gate for E<sup>2</sup>. The reliability claims are difficult to understand and verify due to the link of failure to endurance cycling. Different

methods are used in reliability evaluation, and no standard exists to allow a meaningful comparison. For example, high temperature cycling is worse case for FLOTOX but may be best case for textured poly. Nevertheless, there has been continued growth in the E<sup>2</sup>PROM market, sustained by a wide, diversified application base. The driving force is end-user, in-the-field customization capability offered to microprocessor based products, which is either unavailable, unreliable or not cost effective using other techniques. As a result, standards are now established following 5V-only RAM-like functionality, and the cost and density gap to competing solutions continues to close.

## FUTURE TRENDS

There are two major driving forces in the development of E<sup>2</sup> technologies for the future. One of them is high density memories, requiring small memory cell size for the lowest cost per bit. The second requirement is low density nonvolatile memories in microcontrollers and programmable logic type applications. In the latter case the absolute cell size is not as important as process simplicity and low cost of the overall technology. MNOS based E<sup>2</sup> memories will continue to be used in low density memory as well as military applications requiring high radiation tolerance. However, it has only enjoyed limited popularity for use in high density memory and the trend will continue. A majority of companies have opted for FLOTOX as their first E<sup>2</sup> technology because of the simple device physics and the low entry cost for development. Recently, many Japanese companies have announced 64K E<sup>2</sup>PROMs based on FLOTOX for the smart card market. A number of companies have applied FLOTOX in ASIC and programmable logic array applications. In fact, some have developed single poly versions of FLOTOX for synergy with random logic technology. However, for stand alone high density E<sup>2</sup> memories, FLOTOX will be increasingly limited by defect oxide breakdown problems,<sup>10</sup> giving unacceptable failure rate above the 64K level, unless thicker oxides or new dielectrics can be used in new approaches. Error correction codes can also be used but at the expense of additional die cost.<sup>11</sup> Finally, textured poly inherently gives a smaller memory cell and suffers least from the oxide breakdown problem. Electron trapping is an intrinsic property that can be predicted and easily screened. Consequently, textured poly technology is expected to be most reliable and cost effective for 256K and above densities, while the higher cost of a three layer poly process may limit its use in logic applications.

The nonvolatile memory technology is an ever evolving field. Memories<sup>12,13,14</sup> based on hybrid operation of programming by EPROM and erase by tunneling have gained interest. The erase function is generally limited to the full array and thus it is called FLASH erase. Recent approaches offer cell size and technology complexity comparable to EPROMs, and the functionality of electrical erase. If such technologies are proven to be reliable and manufacturable, they will fill the need of a special market segment and become another major force in the developing nonvolatile memory market.

## SUMMARY

We have reviewed the three dominant E<sup>2</sup> technologies today. MNOS is used in low density memories as well as military applications, but enjoyed only limited popularity for high density memories. FLOTOX has been the most popular approach because of its simplicity and is most suited for low density memories and programmable logic type application. Textured poly gives the smallest memory cell size and is the most cost effective and reliable approach for high density memories.

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## NEW ULTRA-HIGH DENSITY TEXTURED POLY-Si FLOATING GATE E<sup>2</sup>PROM CELL

By D. Guterman, B. Houck, L. Starnes and B. Yeh

This paper describes a new, highly scaled cell structure, the smallest full function E<sup>2</sup>PROM cell reported to date. It utilizes the textured triple-poly-si technology, exploiting the high degrees of structural and functional integration, to achieve a cell size of 31  $\mu^2$ . A top view of the cell, built with 1.2 micron rules is shown in Figure 1, with cell cross-section and equivalent circuit shown in Figures 2 and 3, respectively.

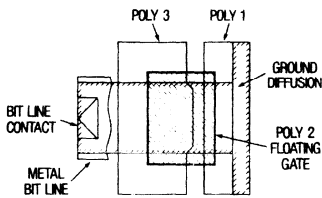


Figure 1: Cell top view.

0023-1

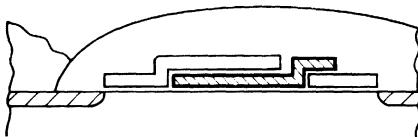


Figure 2: Cell cross-section.

0023-2

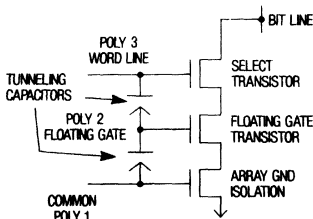


Figure 3: Cell equivalent circuit.

0023-3

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Very small memory cell size is achieved by exploiting the vertical integration of the three poly layers to form a merged gate single transistor cell. This cell is made possible through the dual functions incorporated within various key components; specifically, (1) the poly 3 element, which functions as both word line select transistor and erase tunneling anode (2) the poly 1 electrode which serves the dual role of cell ground isolation transistor and programming cathode during write operation, and (3) the poly 2 floating gate transistor whose channel region establishes both the floating gate charge-conditional current path for reading and the input-data-conditional steering capacitor for writing. Charge transport to and from the floating gate is through Fowler-Nordheim tunneling, established by the geometrically enhanced fields at the textured poly interfaces between poly-si layers. This allows tunneling injection and transport to occur across oxides of thickness greater than 500Å at voltages less than 15V. In comparison to ultrathin (100Å) E<sup>2</sup>PROM technologies, the thicker interpoly oxides result in lower parasitic capacitance of the tunneling element, improved dielectric reliability because of the 3-5 $\times$  lower average fields in the oxide, and an easier path to oxide scaling.

Because of the simultaneous incorporation of the poly 2 to 1 programming and poly 3 to 2 erase tunneling elements, data storage is a direct, single pass operation, involving the following sequence (see Table I). First the poly 1 line, common to the entire array, is brought low, cutting off the conduction path from bit line through the cell to array ground. Next, the bit lines are set up to either 0V for an erased state or about 16V for a programmed state. Finally, the poly 3 word line is ramped up to about 22V in 1 ms to drive the nonvolatile charge transport. To erase, the bit line is grounded, whereupon the channel under poly 2 capacitively steers the floating gate towards ground. This induces sufficient voltage across the poly 3/2 tunneling element to remove electrons from the floating gate. When the bit line is high for programming, the channel potential steers the floating gate positively. This

TABLE I: OPERATING CONDITIONS

Operation	Bit Line	Poly 3	Poly 1
Standby	2V	0	5V
Read	2V	5V	5V
Write			
Erased State	0	~ 22V	Low
Programmed State	~ 16V		

induces sufficient voltage across the poly 2/1 tunneling element to inject electrons onto the floating gate.

Following up on the present 256K product experience, a number of fundamental factors are incorporated into the technology to maintain a high degree of reliability with scaling. Dielectric integrity and excellent charge retentivity is preserved through the use of thick, high quality thermal SiO<sub>2</sub> dielectrics, throughout. Direct write cell operation provides shorter write time by eliminating the unconditional clear before write. As in previous floating gate E<sup>2</sup>PROMs, 5V-only capability via on-chip voltage multiplication is possible because of the efficient Fowler-Nordheim tunneling mechanism.

Small test arrays of the 31  $\mu^2$  cell, shown in the SEM views of Figure 4, have been built and operated successfully for endurances of 1 million writes. Figure 5 shows a representative extended endurance plot, demonstrating erased state cell currents of greater than 40  $\mu$ A and programmed cells having thresholds of greater than 5V, thereby remaining in cutoff.

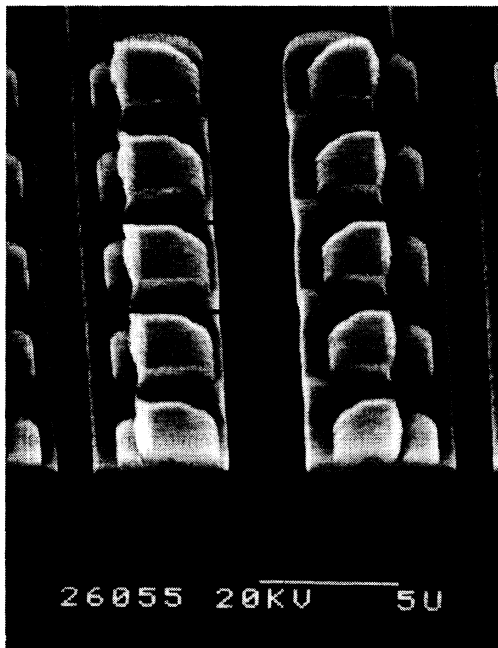


Figure 4a: Cell SEM top view.

0023-4

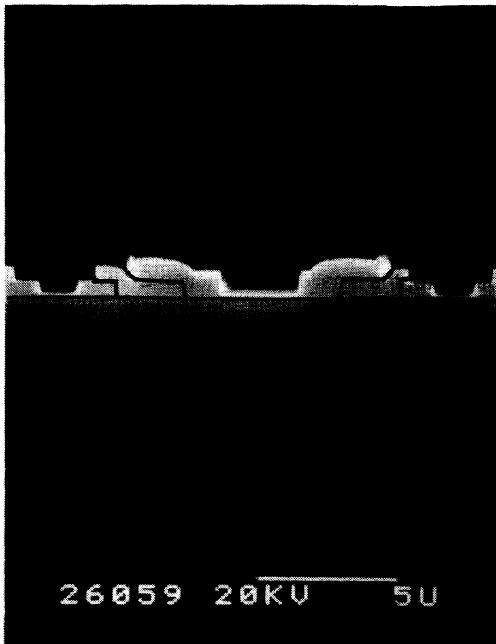


Figure 4b: Cell SEM cross-section.

0023-5

**ENDURANCE DATA**  
**LOT # BD230001S/04 X130/1**

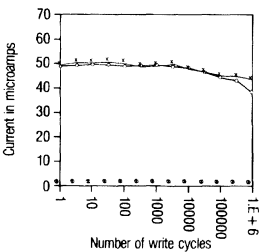


Figure 5: E<sup>2</sup>PROM cell test endurance data.

0023-6

In conclusion, this paper reports the smallest full function E<sup>2</sup>PROM cell described to date. Small size is a result of a cell in which elements serve multiple functions and a technology which is conducive to scaling. This approach will serve as foundation for developing future generation E<sup>2</sup>PROMs beyond today's 256K density.

## RELIABILITY COMPARISON OF FLOTOX AND TEXTURED POLY E<sup>2</sup>PROMs

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Lori J. Purvis & H.A. Richard Wegener—  
Xicor, Inc.

### SUMMARY

FLOTOX and Textured Poly E<sup>2</sup>PROMs share the excellent retention and lifetest performance of the more common EPROM. In particular, retention failures add only about 20 FIT to lifetest failure rates in the 100 FIT range. The lifetest failure rates compare favorably with those of simple static logic products, because these high voltage devices have no oxide breakdown problems during 5V operation. FLOTOX endurance is limited entirely by oxide breakdown, overwhelmingly of the tunnel oxide. Window closing, caused by electron trapping, occurs but does not cause failure in well-designed products.

The Textured Poly approach offers a reliability tradeoff: less oxide breakdown but more window closing. This tradeoff becomes favorable at higher densities. This is because oxide breakdown, being a defect mechanism, worsens with increasing memory size and with scaling of oxide thickness. Window closing is an intrinsic mechanism that does not worsen dramatically with higher density. The two failure mechanisms—oxide breakdown and window closing—should be treated separately in reliability evaluations because they have different dependencies on cycling, temperature and retention bakes.

## RETENTION CHARACTERISTICS

The E<sup>2</sup>PROM retention is at least as good as the EPROM retention, as shown in Table I. The 0.2% failing for the I 2817A represents only 20 FIT added to the failure rate. All retention failures are at most only a few bits out of the memory array. Intrinsic retention limitations simply do not exist on these technologies; most bits have essentially unlimited retention.

Excellent retention is expected with these technologies for two reasons:

- 1) The stored charge on the floating gate is contained by the 3.2eV energy barrier which exists at the Si-SiO<sub>2</sub> interface. This barrier height is quite high, comparable to the barriers preventing dopant atoms from redistributing.
- 2) The oxide layers, even with FLOTOX, are thick enough to prevent carriers from tunneling off the floating gate during low voltage operation.

## LIFETEST PERFORMANCE

TABLE II: LIFETEST COMPARISONS OF INTEL  
E<sup>2</sup>PROM, EPROM AND STATIC LOGIC

Product(s)	Technology	125°C Lifetest Predicted Failure Rate (55°C, in FIT)		
		Breakdown	Retention	Total
2817A	FLOTOX	0	36	70
27256	EPROM	0	22	63
2114B, 8088, etc.	HMOS-II	110	0	120

The failure rates predicted from lifetest in Table II compare favorably with those of EPROMs, which in

TABLE I: RETENTION COMPARISON OF INTEL EPROM AND E<sup>2</sup>PROM, AND XICOR E<sup>2</sup>PROM

Product	Technology	Sample	Temp	% Fail in Retention Bake			
				48 Hrs	168 Hrs	500 Hrs	1000 Hrs
I 2764A	EPROM	1800	250°C	0.9%*	1.1%	2.0%	—
I 2817A	FLOTOX	550	150°C	0.0%	0.0%	0.2%	0.2%*
X2864G	Textured Poly	350	250°C	0.0%*	0.0%	0.0%	0.3%

\*Represents ~ 15 Years at 55°C (E<sub>A</sub> = 0.6eV).



turn compare favorably with those of non-floating gate technologies. E<sup>2</sup>PROMs compare favorably with EPROMs because they are very similar technologies. It is only during endurance cycling that E<sup>2</sup>PROM operation differs significantly from EPROM operation. EPROMs and E<sup>2</sup>PROMs compare favorably with static logic devices because the nonvolatile devices are built on high voltage technologies and are operated during product testing at high voltages. This all but guarantees that there will be no oxide breakdown failures during 5V operation. Static logic devices generally are dominated by oxide breakdown. In addition to the Intel data above, NEC has reported that 65% of field failures from 1976 to 1979 were due to oxide failure.

## ENDURANCE CHARACTERISTICS

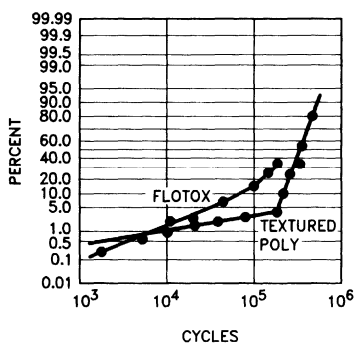


Figure 1: Percent fail vs. number of cycles at room temperature for FLOTOX (2816A, 2817A) and Textured Poly (2864).

FLOTOX endurance, as shown in Figure 1, has a single broad distribution of failures. Textured Poly endurance has a low level defect tail followed by a sharp wearout beyond 150K cycles. The curves imply that the Textured Poly approach offers a trade-off under which a lower defect tail can be had at the expense of some wearout endurance. There are 3 primary failure mechanisms represented in Figure 1:

- 1) Tunnel Oxide Breakdown—the dominant FLOTOX mechanism, also responsible for part of the Textured Poly defect tail.
- 2) Gate Oxide Breakdown—responsible for the remainder of the Textured Poly defect tail.

- 3) Window Closing—the cause of Textured Poly wearout.

These three mechanisms will be discussed in turn.

## ENDURANCE: TUNNEL OXIDE BREAKDOWN

A typical FLOTOX or Textured Poly cell can be cycled over a million times without oxide failure or any degradation in retention characteristics. Occasional defective tunnel oxides will eventually break down under the high electric field ( $\sim 10$  MV/cm) necessary for tunneling. When this occurs, the defective cell will either become stuck to one logic state (if the oxide is truly shorted) or fail to retain charge (if the oxide is only leaky). Generally, the oxide breakdown increases gradually with cycling—a bit becomes leaky slowly, then faster, and eventually it becomes stuck. Tunnel oxide breakdown is responsible for about half of the Textured Poly defect tail. It displays the same characteristics as FLOTOX.

## ENDURANCE: GATE OXIDE BREAKDOWN

Both E<sup>2</sup>PROM types require high voltages to program and erase. This puts high stress on MOS gate oxides both in the cell and in the logic circuitry using high voltage. This high stress causes defective gate oxides to break down. Typical symptoms are a row or column failure or failure of the entire device. This failure mechanism is responsible for the remainder of the Textured Poly defect tail.

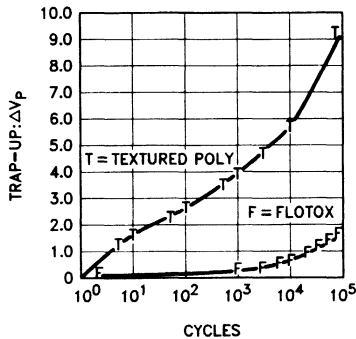
Although more common on Textured Poly than on FLOTOX because of somewhat higher voltages, the overall oxide breakdown failure rate of Textured Poly (tunnel oxide plus gate oxide) is still significantly lower than that of FLOTOX.

## ENDURANCE: WINDOW CLOSING

During endurance cycling, some of the electrons tunneling through the tunnel oxides become trapped there. The resulting negative oxide charge inhibits further tunneling. The effect of this electron trapping

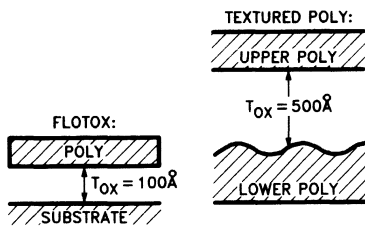
is that with further cycling a cell requires higher and higher voltages to program and erase. This mechanism is responsible for the entire wearout region of the Textured Poly curve but is non-existent in the FLOTOX curve.

In Figure 2 Textured Poly shows a dramatically higher rate of trap-up. As a result, window closing is the dominant wearout mechanism of Textured Poly, whereas it is an issue of FLOTOX only if the circuit design is marginal.



0024-2  
Figure 2: Trap-up vs. cycles for Textured Poly (2864) and FLOTOX (2816A). Trap-up is measured in terms of the increase in programming voltage  $\Delta V_p$  necessary to program the cell.

## TRAP-UP/BREAKDOWN TRADEOFF



0024-3  
Figure 3: FLOTOX and Textured Poly structures.

Trap-up is greater in the Textured Poly approach because:

- 1) The trapping probability for a single electron is proportional to  $N\sigma T_{OX}$ , which for the same trap density  $N$  and cross-section  $\sigma$  is greater for Textured Poly, since  $T_{OX}$  is greater.

- 2) The effect of the trapped charge is multiplied by the same field acceleration factor responsible for the field enhancement used for tunneling.

- 3) There is less field induced detrapping because the average electric field is lower.

Tunnel oxide breakdown is less frequent in the Textured Poly approach because:

- 1) The tunnel oxides are thicker and therefore are less sensitive to microscopic defects.
- 2) The high electric field responsible for tunneling occurs only in the region of oxide near texture points; the bulk of the oxide sees only low field stress.

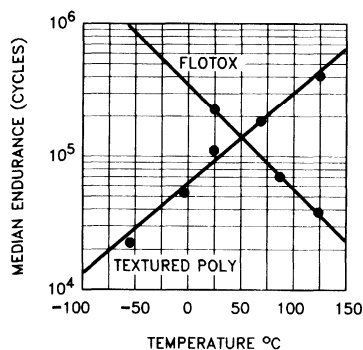
The trap-up/breakdown tradeoff is fundamental to the Textured Poly approach.

## BENEFITS OF THE TRADEOFF

Trap-up is an intrinsic mechanism, determined by trap density, trap cross-section, and initial window size. There is some variation from cell to cell in these parameters, causing some to fail somewhat earlier than others, but the distribution is relatively tight. As a result, trap-up endurance becomes only slightly worse with increasing memory size.

In contrast, oxide breakdown is a defect mechanism, and the failure rate is proportional to the defect density and the memory size. As a result, FLOTOX endurance will always become proportionately worse with increasing memory size unless defect density is continually improved. In addition, scaling FLOTOX implies scaling the tunnel oxide thickness, making the oxide even more sensitive to defects.

For this reason, there is a crossover in reliability between FLOTOX and Textured Poly, with the Textured Poly tradeoff becoming favorable at high densities. Excellent endurance even at high densities is possible with the Textured Poly approach because the defect tail, being only low level, can be screened.



0024-4  
Figure 4: Comparison of median endurance for FLOTOX (2816A) and Textured Poly (2212) as a function of cycling temperature.

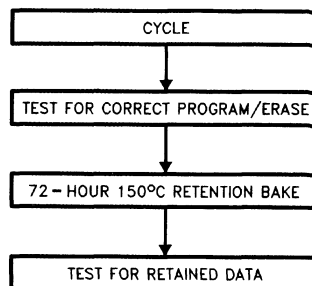
FLOTOX failure, due to tunnel oxide breakdown, is accelerated by cycling temperature ( $E_A \sim 0.18\text{eV}$ ), as shown in Figure 3. Textured Poly failure, due to window closing, is decelerated by cycling temperature ( $E_A \sim -0.11\text{eV}$ ). Whereas it is well known that temperature accelerates oxide breakdown, it also accelerates detrapping of electrons and therefore extends Textured Poly endurance.

A reliability evaluation of these two products performed at 50°C would detect equivalent median endurances, but an evaluation performed at room temperature would favor FLOTOX by about 5× and one at 125°C would favor Textured Poly by about 10×. This temperature acceleration holds true for the median endurance, but the Textured Poly defect tail is due to oxide breakdown and will tend to behave more like the FLOTOX data.

## EFFECT OF BAKES

In many FLOTOX endurance evaluations, less than half of the oxide breakdown failures actually

fail to program correctly. The remainder are cases of oxide degradation and suffer reduced retention instead. As a result, retention bakes must be performed *after* cycling on FLOTOX in order to adequately detect cycling failures:



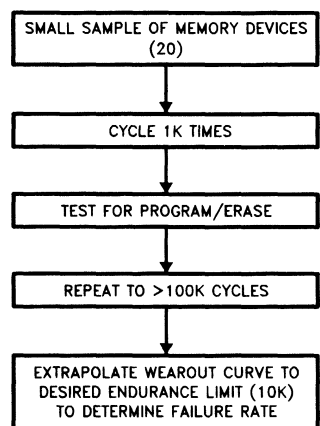
0024-5

In order to take intermediate readouts (after, say, 2K and 5K cycles), the flow of test/bake/test may be repeated at each readout. This worst-case flow for FLOTOX may be best-case for Textured Poly, however, because high temperature retention bakes cause electrons to detrapp significantly, reversing prior window closing and therefore increasing measured endurance.

## SUGGESTED ENDURANCE-EVALUATION METHODOLOGY

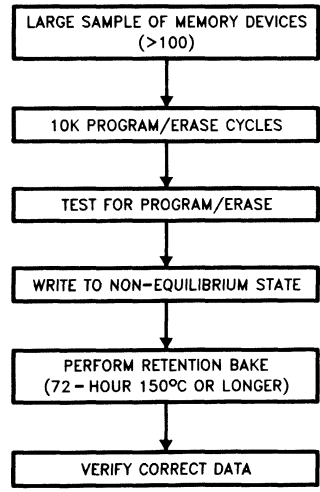
The best way to measure E<sup>2</sup>PROM endurance is to run separate evaluations for the two dominant failure mechanisms: window closing and oxide breakdown.

# Window Closing



0024-6

# Oxide Breakdown



0024-7

These flows will work for either FLOTOX or Textured Poly. Intermediate readouts may be performed in the oxide breakdown flow, but the test/bake/verify sequence should be repeated at each readout.

## ALTERNATIVE EVALUATION METHODOLOGIES

Single-cell endurance data are sometimes presented by manufacturers. This approach will overestimate endurance by orders of magnitude because of the importance of oxide defects and even cell-to-cell variations in trap-up. It might be possible to conclude from single-cell data that a certain FLOTOX cell is "superior" to a certain Textured Poly cell—but a 256K E2PROM constructed with the Textured Poly cell might be several times more reliable.

Worse yet, test pattern data from oxide capacitors are sometimes presented, without backup product data, to "prove" that a certain oxide is "superior" to another. Only product data can reliably be used to compare E2PROM product endurance. Small samples are useful in measuring wearout (median endurance), but large samples are necessary for measuring defect-related tails to the distribution.

## CONCLUSION

The non-endurance-related reliability of FLOTOX and Textured Poly E2PROMs are similar and comparable to EPROMs and simple logic devices. Textured Poly offers a tradeoff between oxide breakdown and window closing which is beneficial at high densities. Reliability evaluations should distinguish between the two dominant E2PROM failure mechanisms: Namely, oxide breakdown and window closing.

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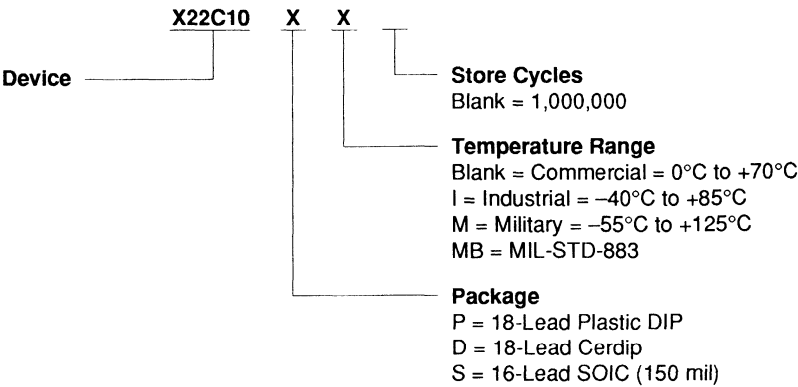
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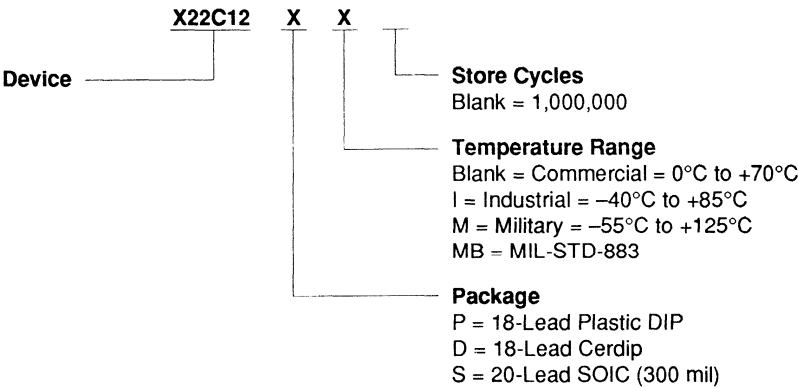
# Ordering Information

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## X22C10: 64 X 4 CMOS NOVRAM



## X22C12: 256 X 4 CMOS NOVRAM

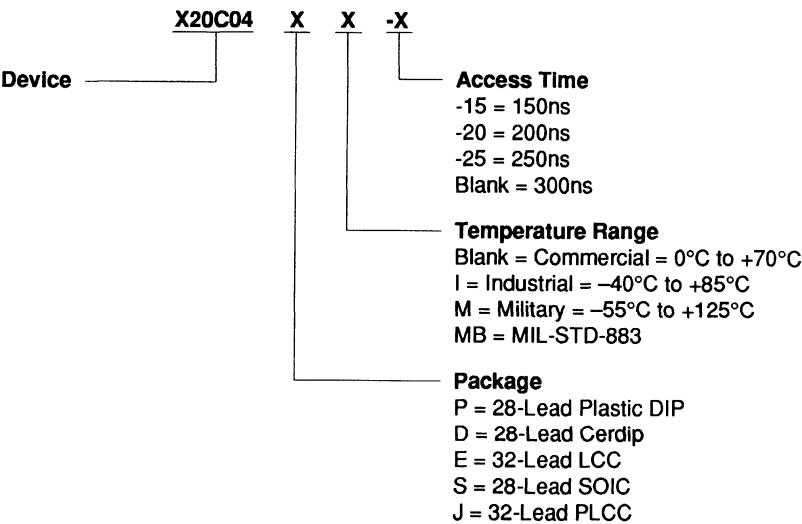




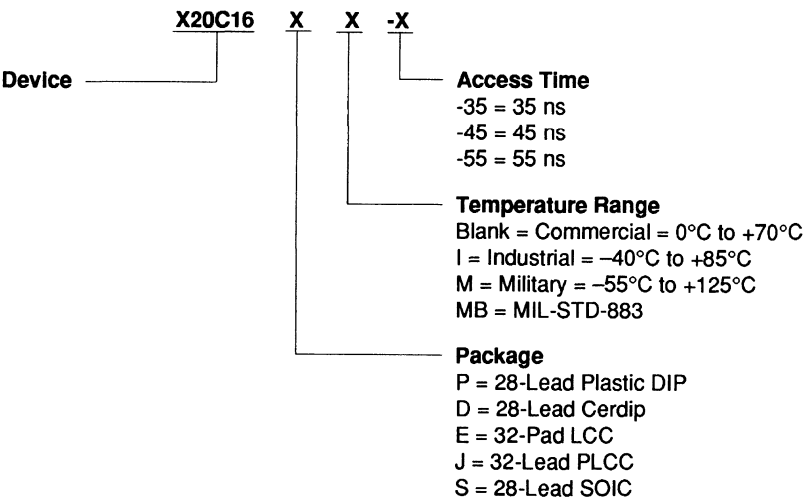
# Ordering Information

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## X20C04: 512 X 8 CMOS NOVRAM



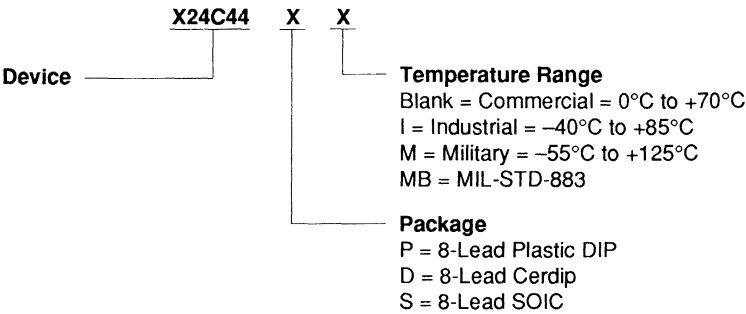
## X20C16: 2K X 8 CMOS NOVRAM



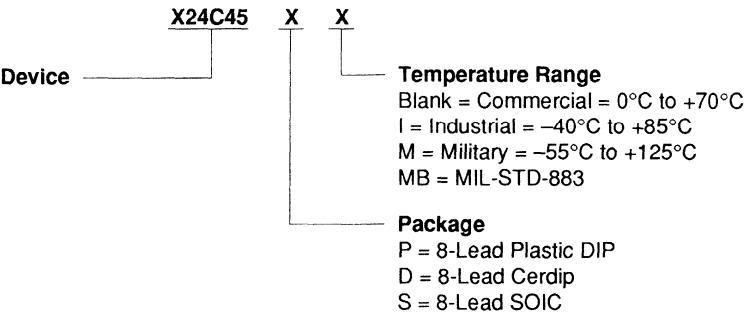
# Ordering Information

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## X24C44: 16 X 16 CMOS Serial NOVRAM



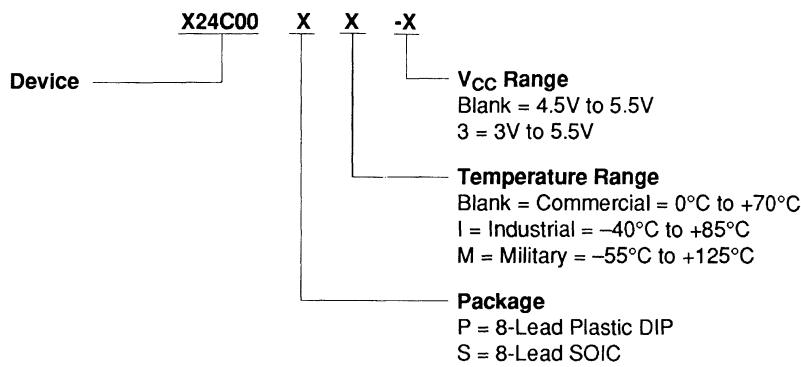
## X24C45: 16 X 16 CMOS Serial NOVRAM With AUTOSTORE



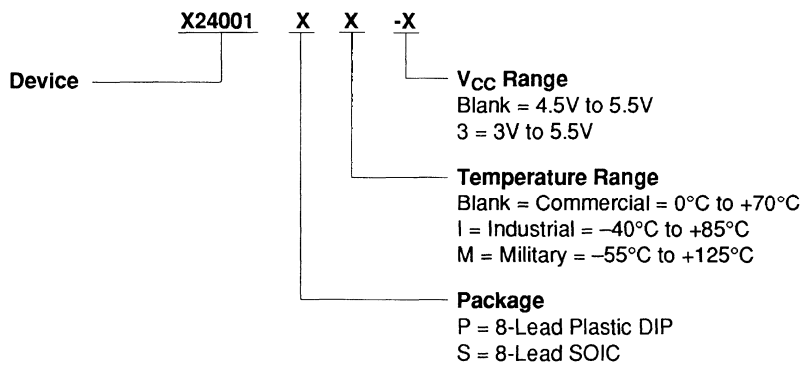
# Ordering Information

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## X24C00: 16 X 8 CMOS Serial E<sup>2</sup>PROM



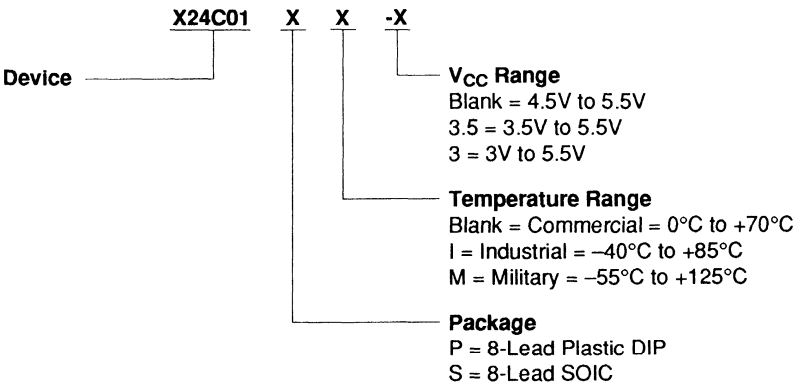
## X24001: 16 X 8 CMOS Serial E<sup>2</sup>PROM



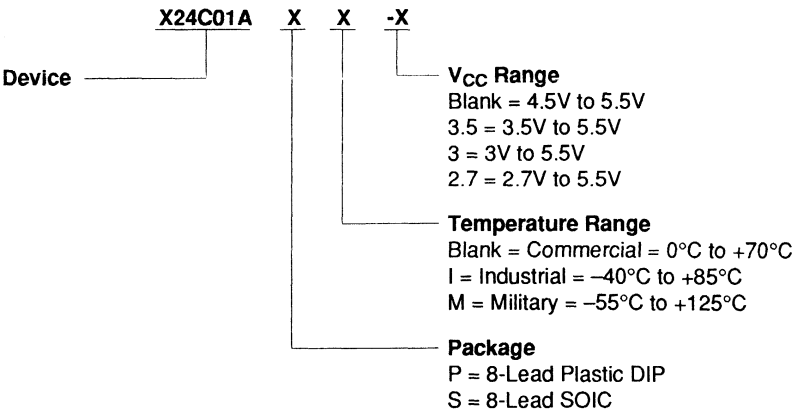
# Ordering Information

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## X24C01: 128 X 8 CMOS Serial E<sup>2</sup>PROM



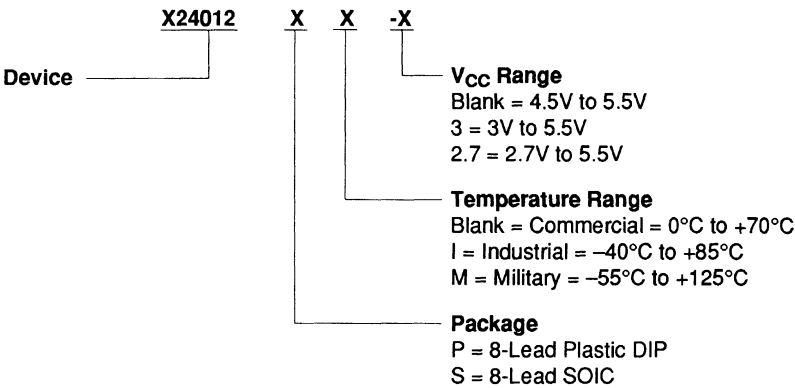
## X24C01A: 128 X 8 CMOS Serial E<sup>2</sup>PROM



# Ordering Information

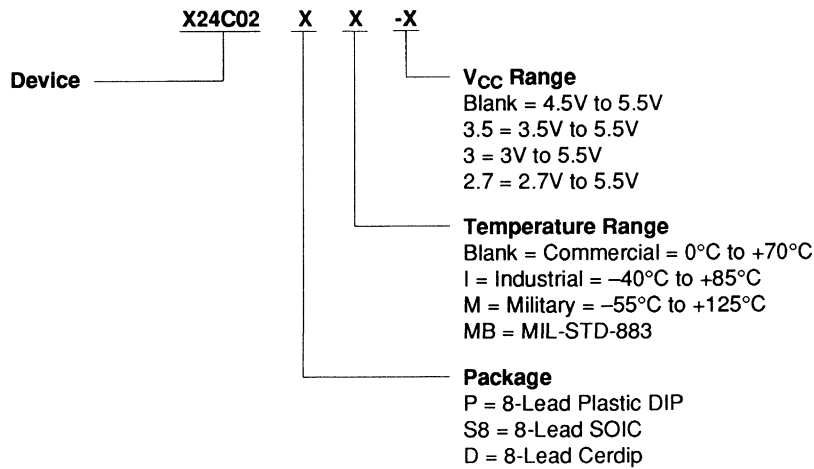
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## X24012: 128 X 8 Serial E<sup>2</sup>PROM

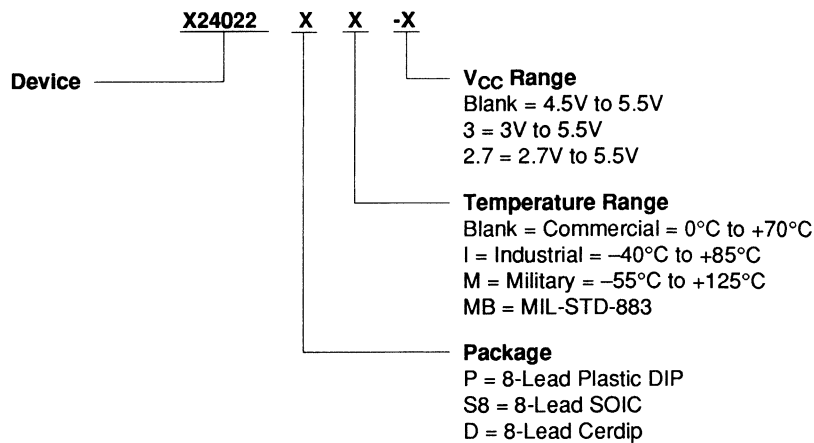


# Ordering Information

## X24C02: 256 X 8 CMOS Serial E<sup>2</sup>PROM



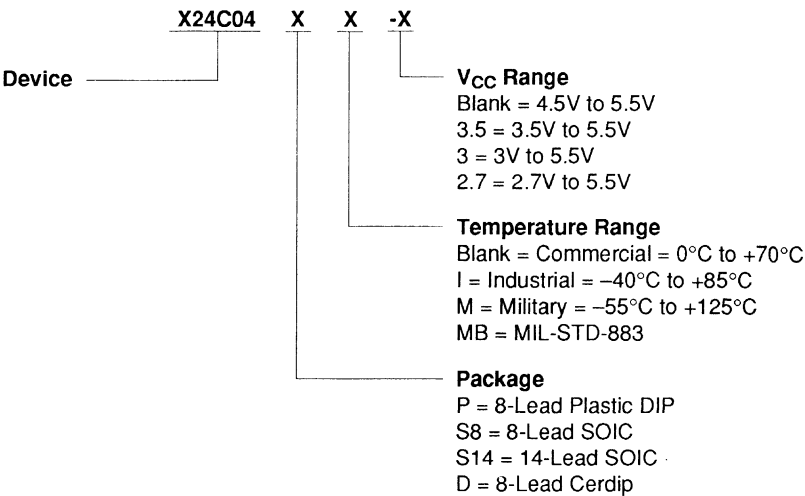
## X24022: 256 X 8 Serial E<sup>2</sup>PROM



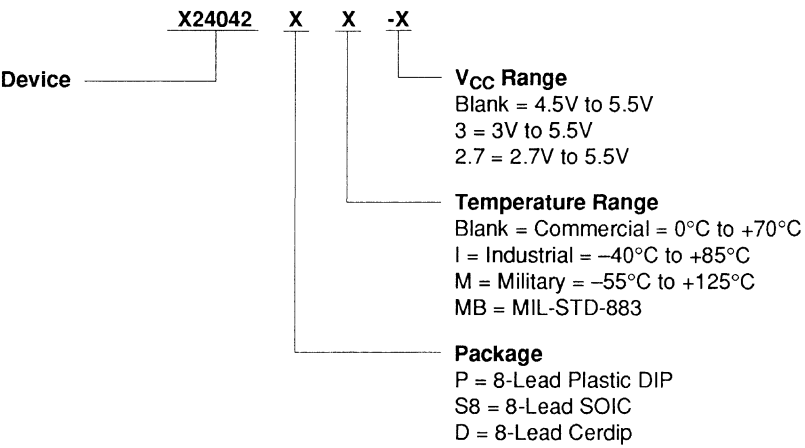
# Ordering Information

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## X24C04: 512 X 8 CMOS Serial E<sup>2</sup>PROM



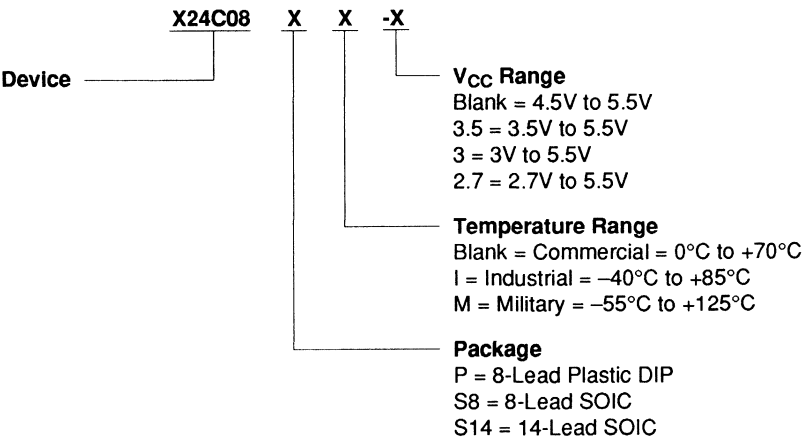
## X24042: 512 X 8 Serial E<sup>2</sup>PROM



# Ordering Information

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## X24C08: 1024 X 8 CMOS Serial E<sup>2</sup>PROM

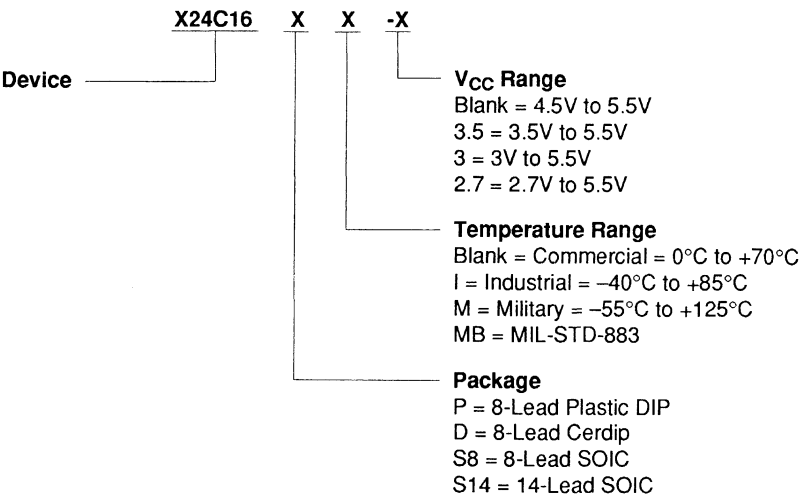




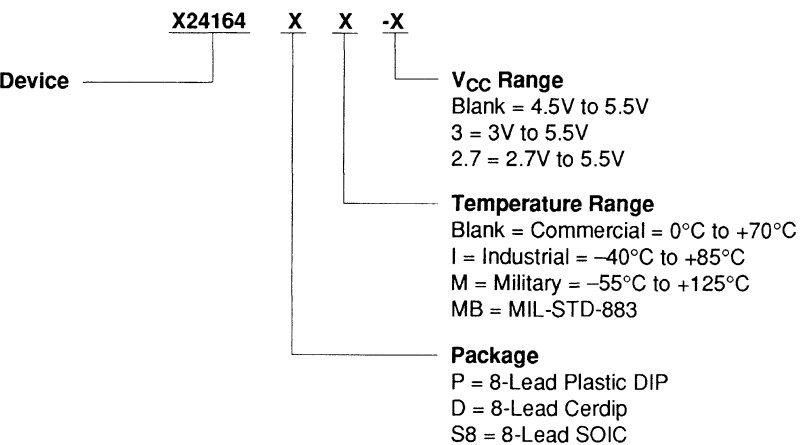
# Ordering Information

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## X24C16: 2K X 8 CMOS Serial E<sup>2</sup>PROM

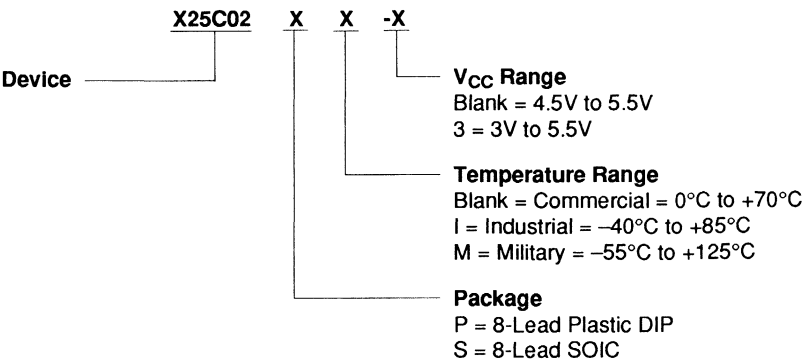


## X24164: 2K X 8 Serial E<sup>2</sup>PROM

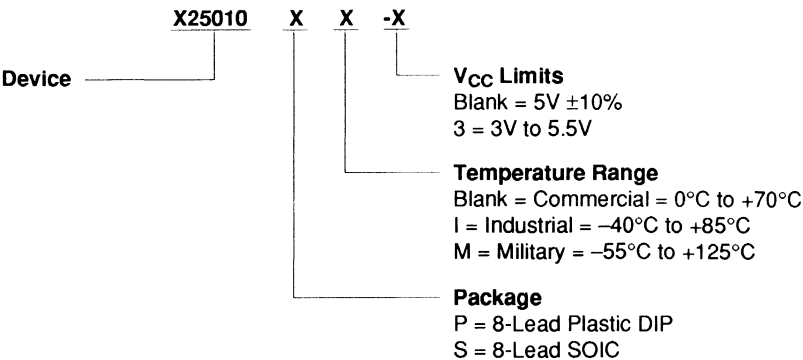


# Ordering Information

## X25C02: 2K SPI CMOS Serial E<sup>2</sup>PROM



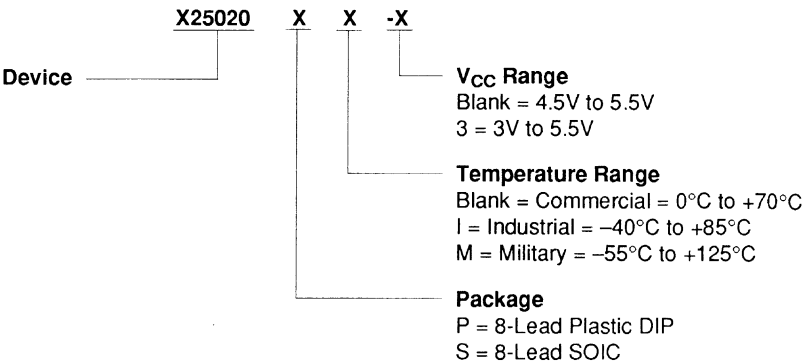
## X25010: 1K SPI CMOS Serial E<sup>2</sup>PROM



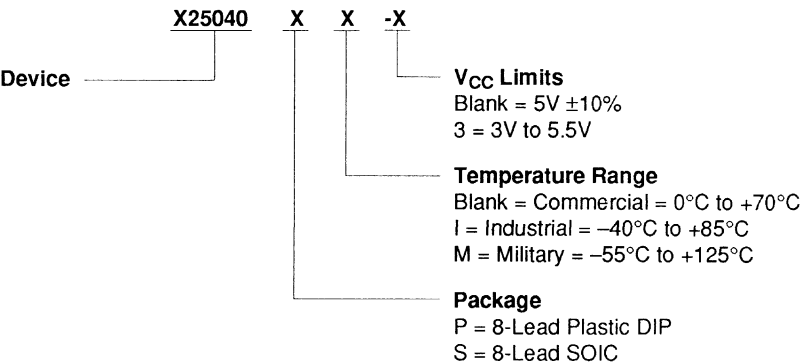
# Ordering Information

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## X25020: 2K SPI CMOS Serial E<sup>2</sup>PROM



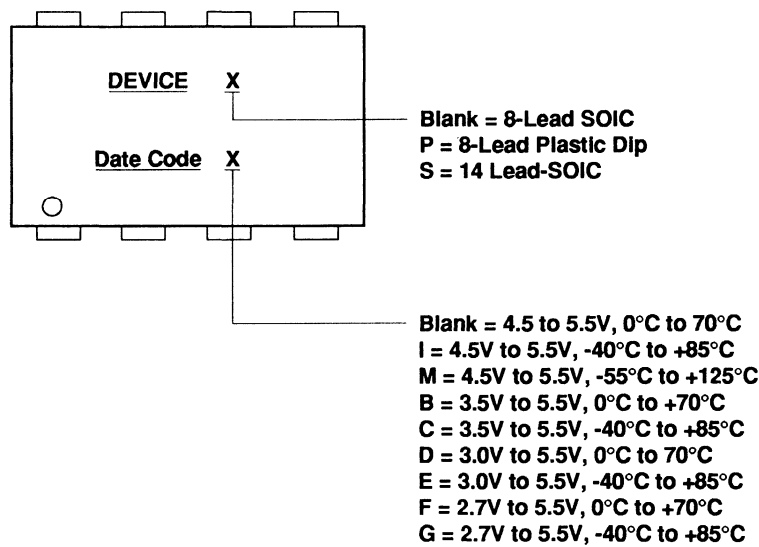
## X25040: 4K SPI CMOS Serial E<sup>2</sup>PROM



# Ordering Information

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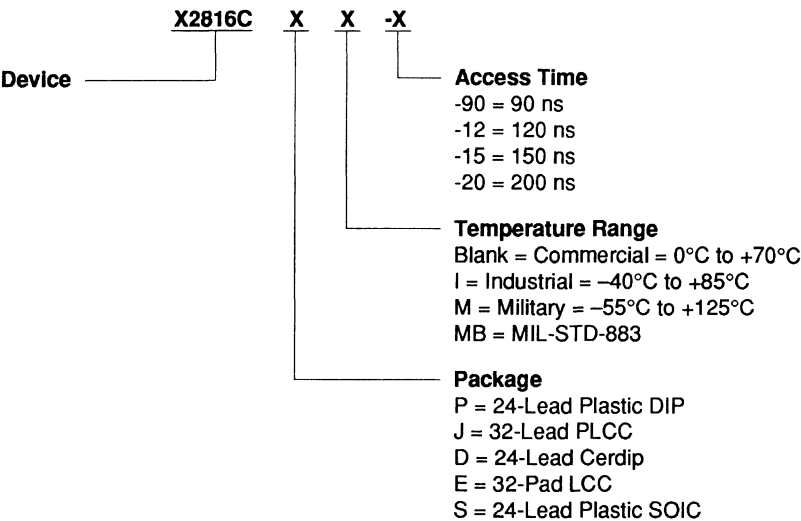
## Serial Part Mark Convention



# Ordering Information

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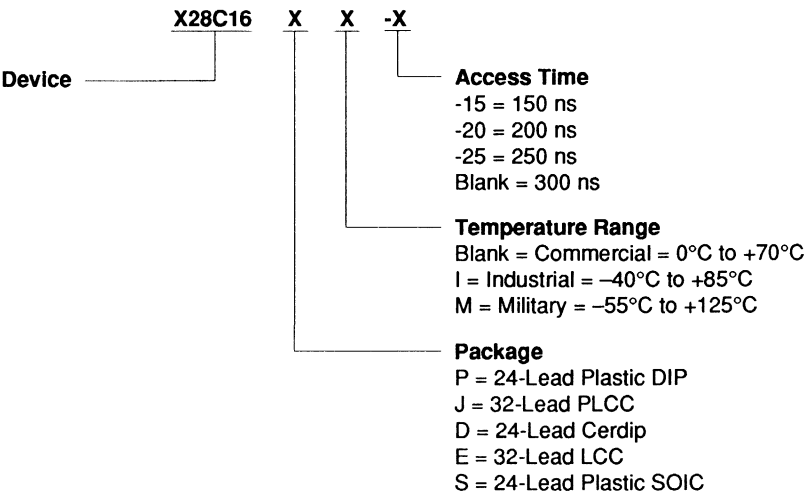
## X2816C: 2K X 8 E<sup>2</sup>PROM



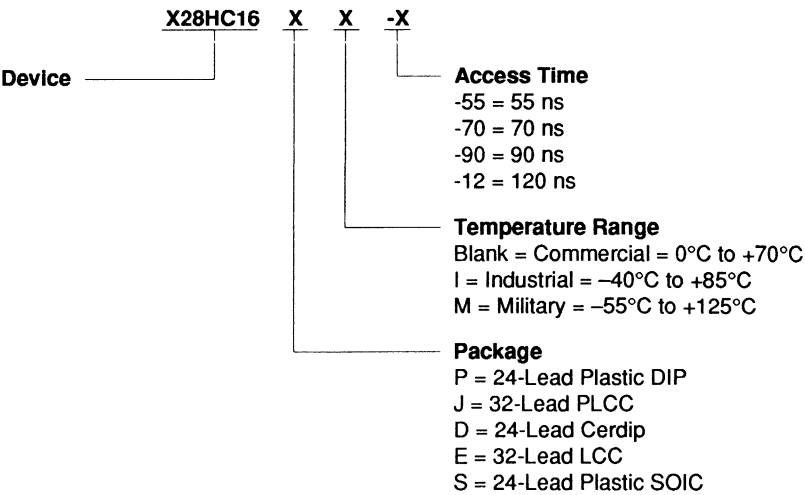
## Ordering Information

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### X28C16: 2K X 8 CMOS E<sup>2</sup>PROM



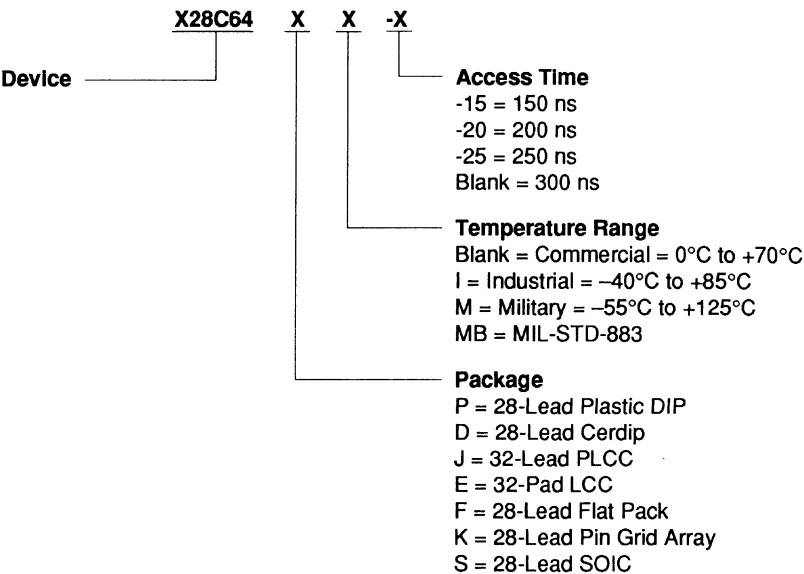
### X28HC16: 2K X 8 High Speed CMOS E<sup>2</sup>PROM



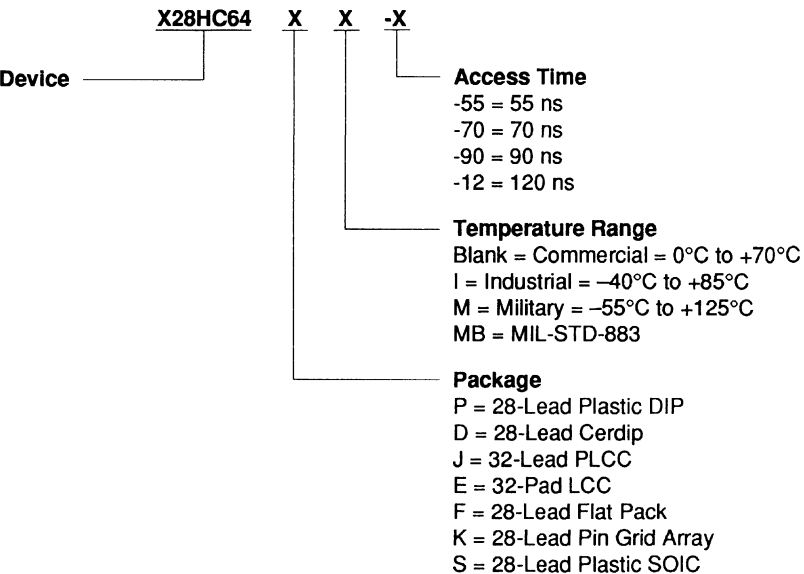
# Ordering Information

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## X28C64: 8K X 8 CMOS E<sup>2</sup>PROM

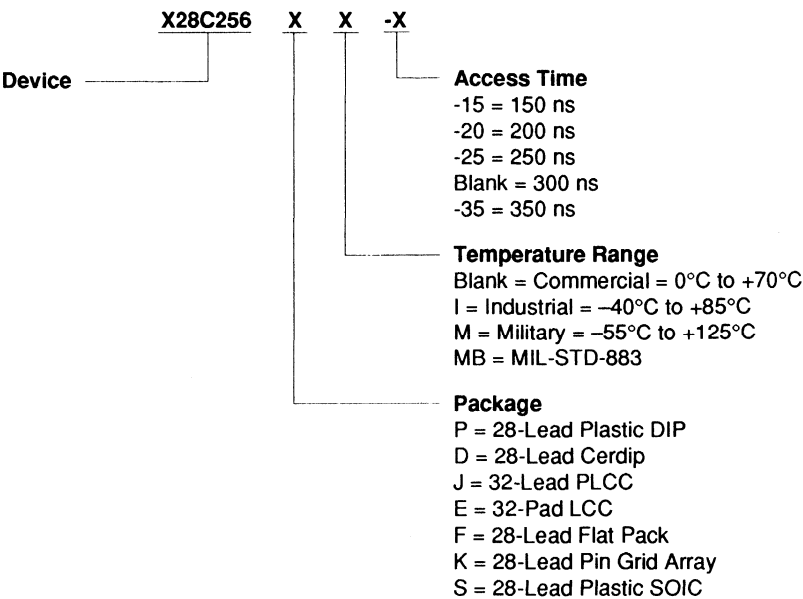


## X28HC64: 8K X 8 CMOS High Speed E<sup>2</sup>PROM

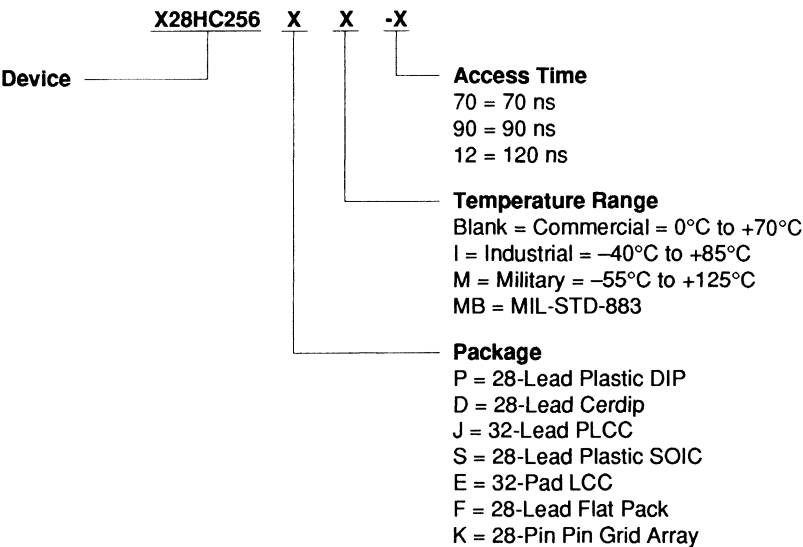


# Ordering Information

## X28C256: 32K X 8 E<sup>2</sup>PROM



## X28HC256: 32K X 8 High Speed E<sup>2</sup>PROM

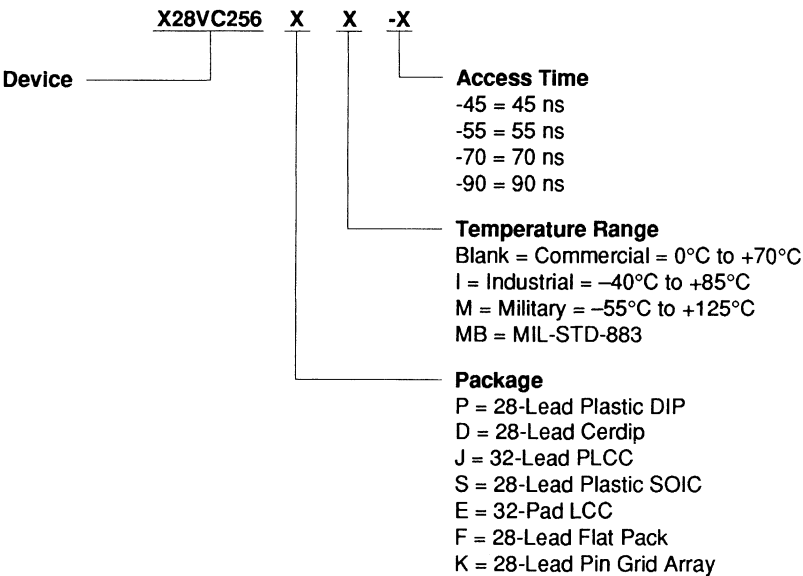




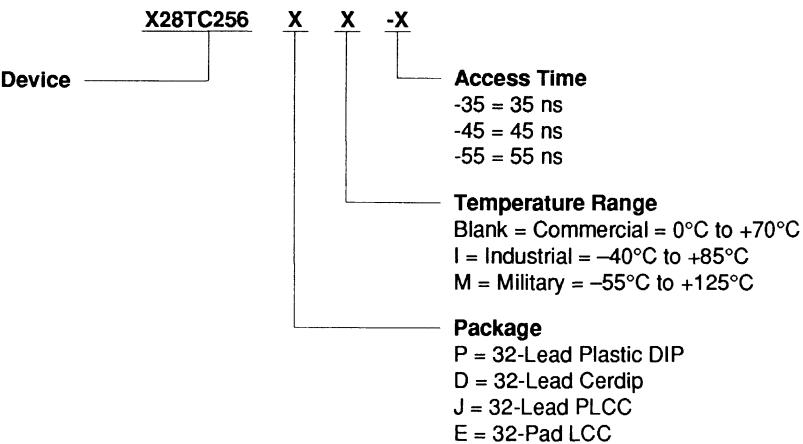
# Ordering Information

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## X28VC256: 32K X 8 Very High Speed E<sup>2</sup>PROM

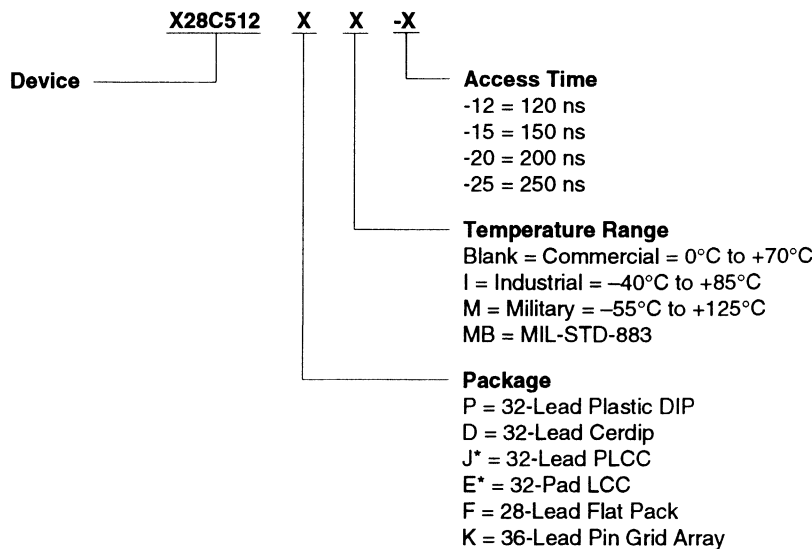


## X28TC256: 32K X 8 Turbo E<sup>2</sup>PROM



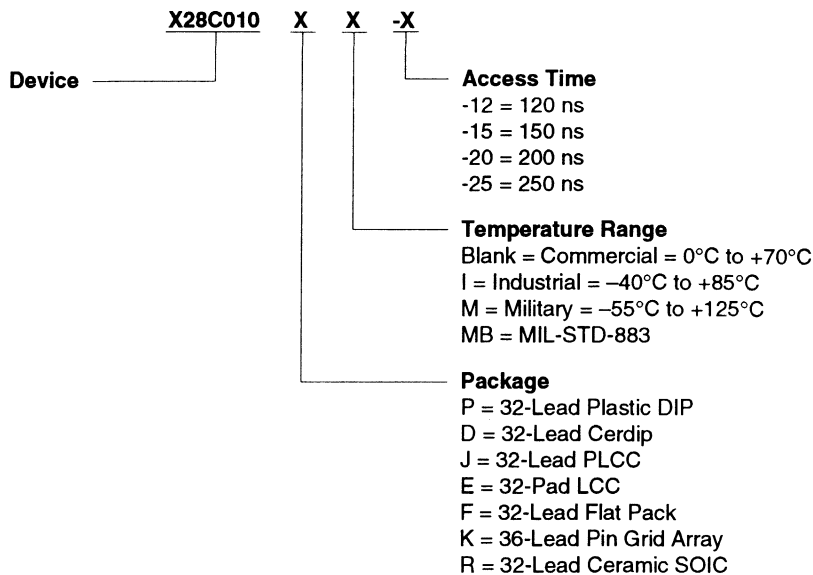
Ordering Information

X28C512 and X28C513\* : 64K X 8 CMOS E<sup>2</sup>PROM



\* The ordering information for the 'C513 is the same as the 'C512, except for the package availability. The 'C513 is only available in the J and E packages.

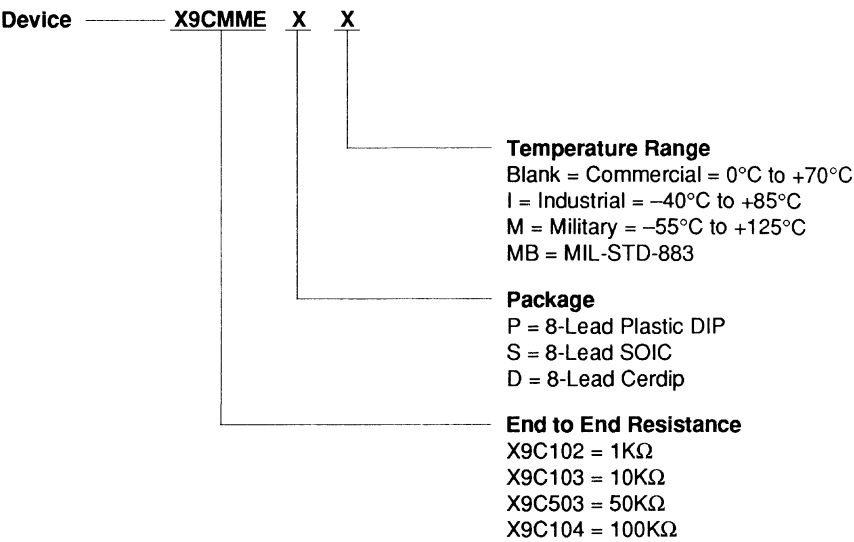
X28C010: 128K X 8 CMOS E<sup>2</sup>PROM



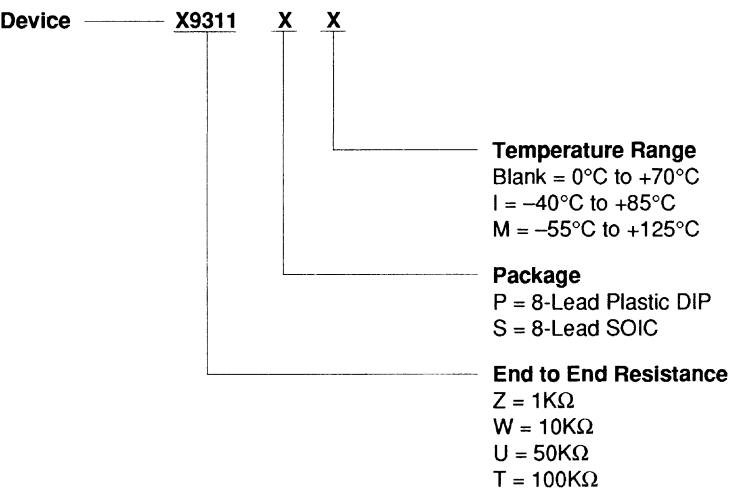
# Ordering Information

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X9CMME: E<sup>2</sup>POT 1K, 10K, 50K, 100K Ohms, Terminal Voltage +5V to -5V



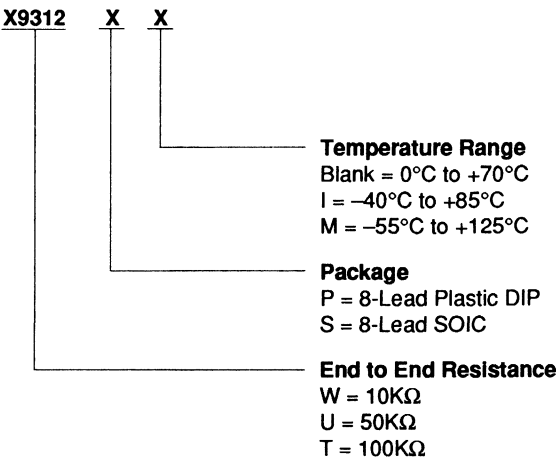
X9311: E<sup>2</sup>POT 1K, 10K, 50K, 100K Ohms, Terminal Voltage 0V to +10V



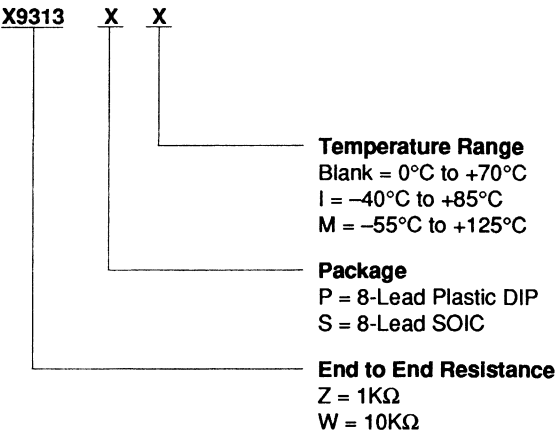
# Ordering Information

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X9312: E<sup>2</sup>POT 10K, 50K, 100K Ohms, Terminal Voltage 0V to +15V



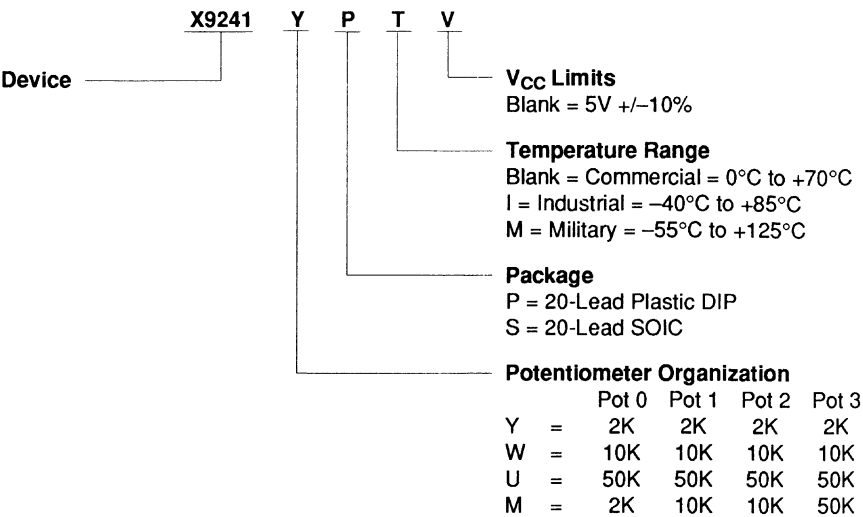
X9313: E<sup>2</sup>POT 1K, 10K Ohms, 31 Resistor Array



# Ordering Information

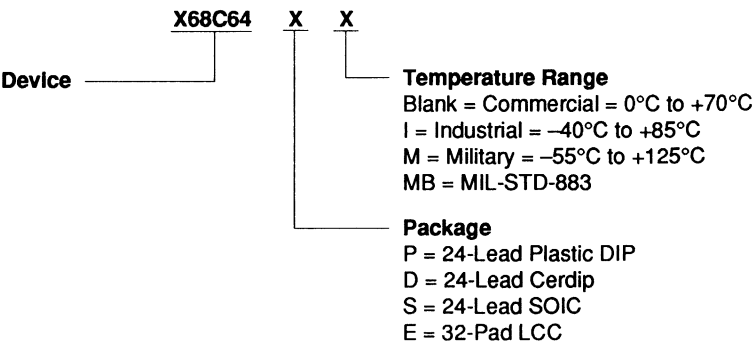
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## X9241: Quad E<sup>2</sup>POT 2K, 10K, 50K Ohms

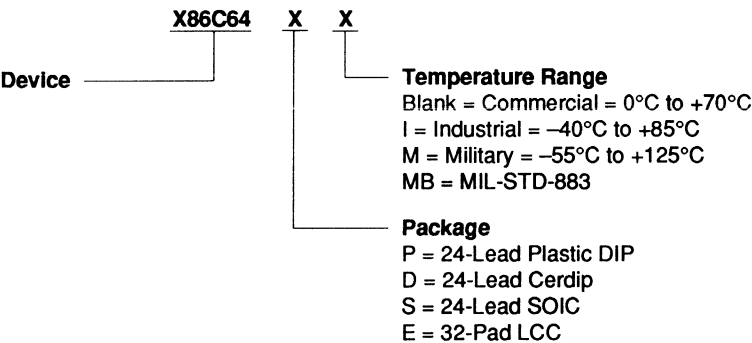


# Ordering Information

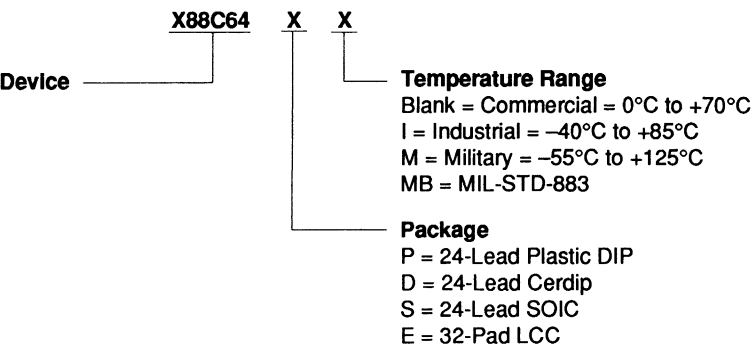
## X68C64: 8K X 8 CMOS Micro-Peripheral E<sup>2</sup>PROM



## X86C64: 8K X 8 CMOS Micro-Peripheral E<sup>2</sup>PROM



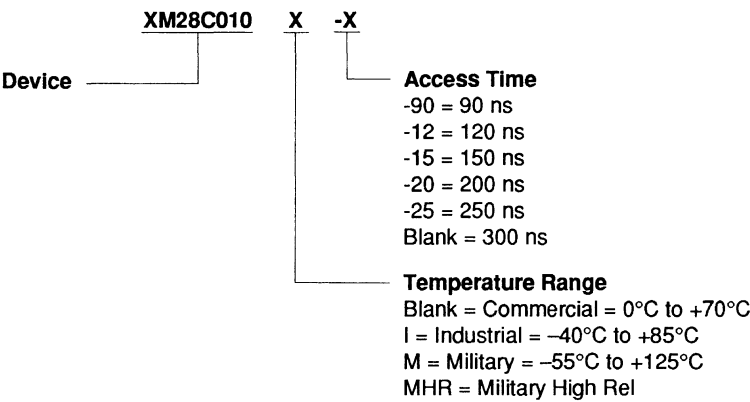
## X88C64: 8K X 8 CMOS Micro-Peripheral E<sup>2</sup>PROM



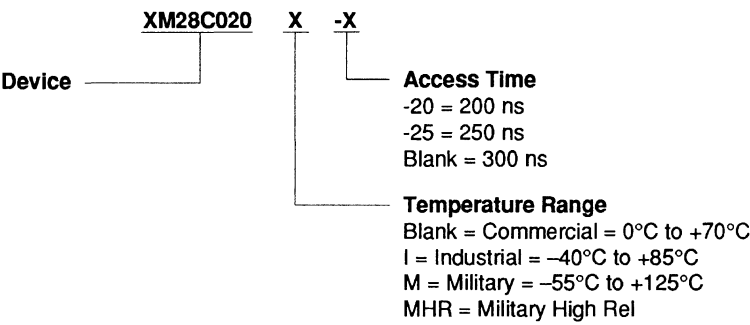
# Ordering Information

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## XM28C010: 128K X 8 CMOS E<sup>2</sup>PROM Memory Module



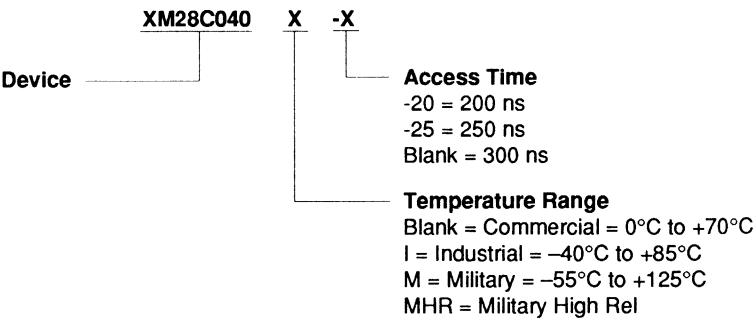
## XM28C020: 256K X 8 CMOS E<sup>2</sup>PROM Memory Module



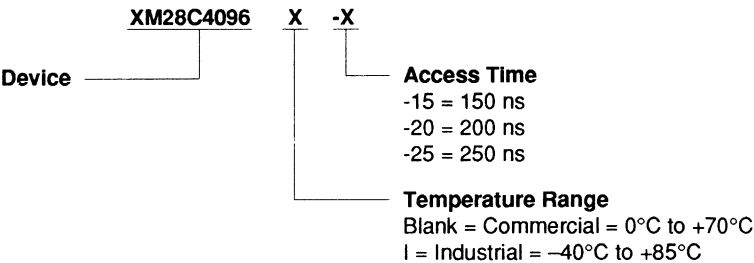
## Ordering Information

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### XM28C040: 512K X 8 CMOS E<sup>2</sup>PROM Module



### XM28C4096: 256K x 16 High Density E<sup>2</sup>PROM Module

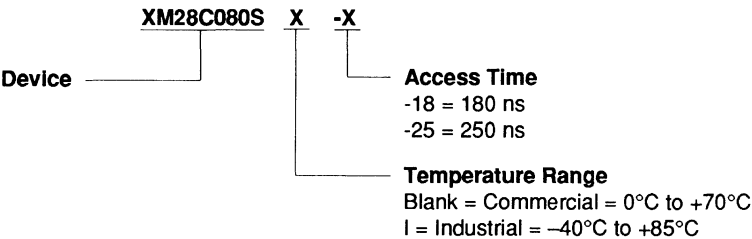




# Ordering Information

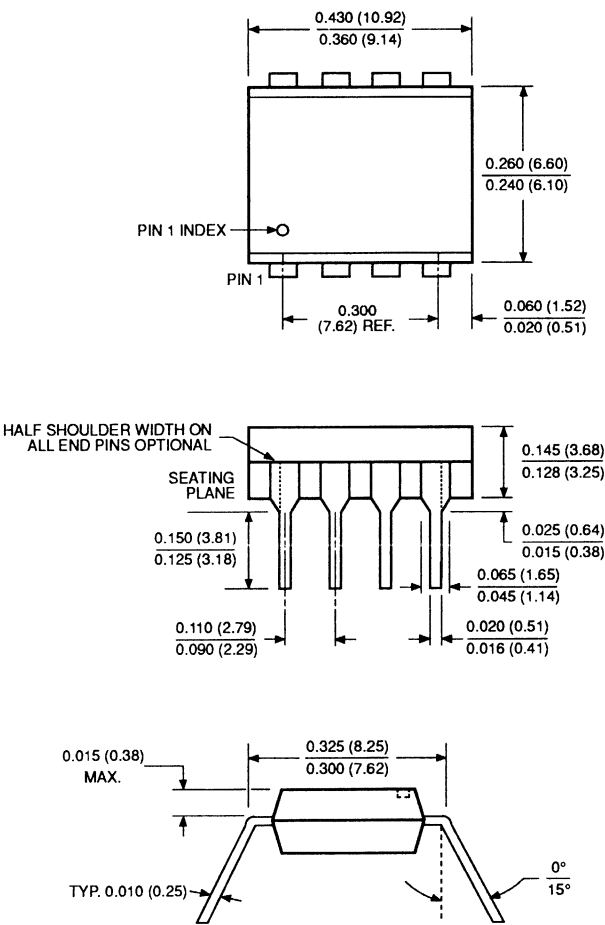
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## XM28C080S: 1Meg x 8, High Density E<sup>2</sup>PROM Module



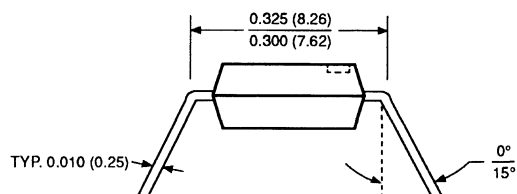
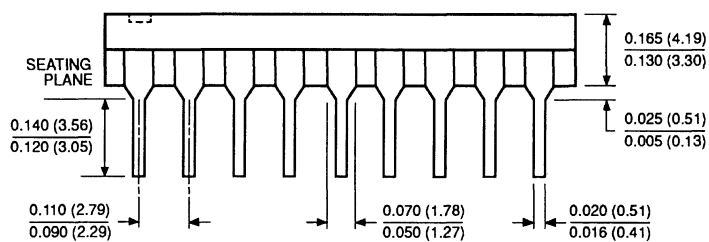
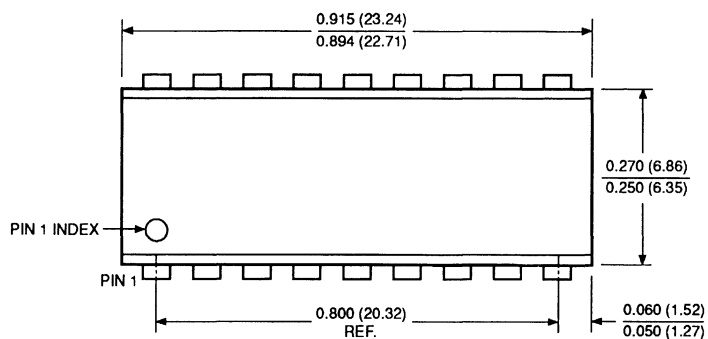
# Packaging Information

## 8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



- NOTE:**
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
  2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

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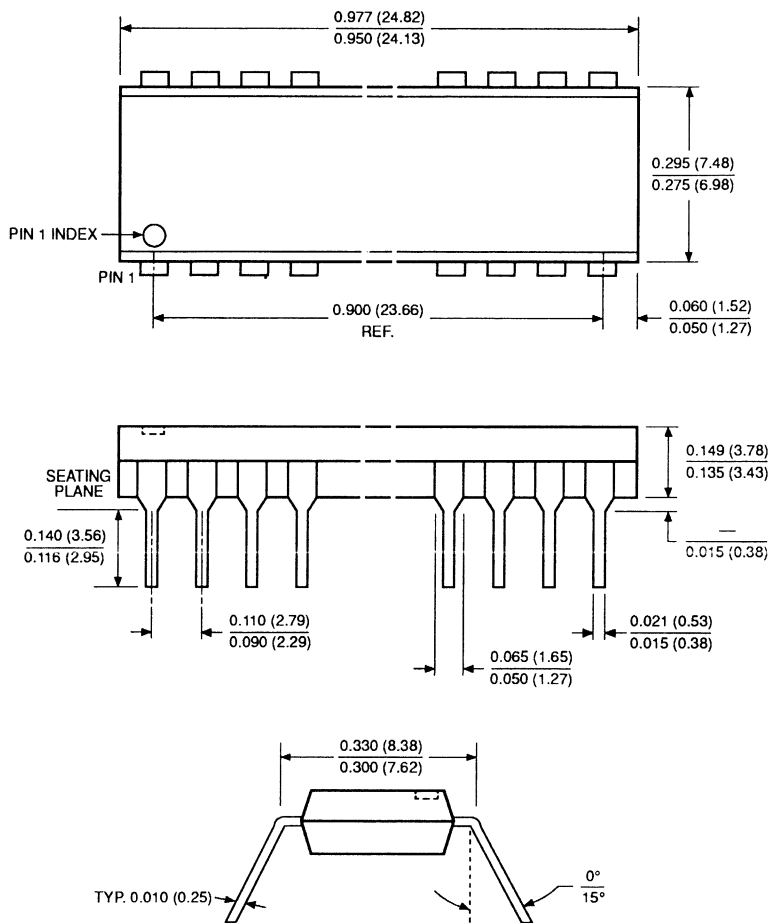


1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)  
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

3926 FHD F02

Packaging Information

20-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

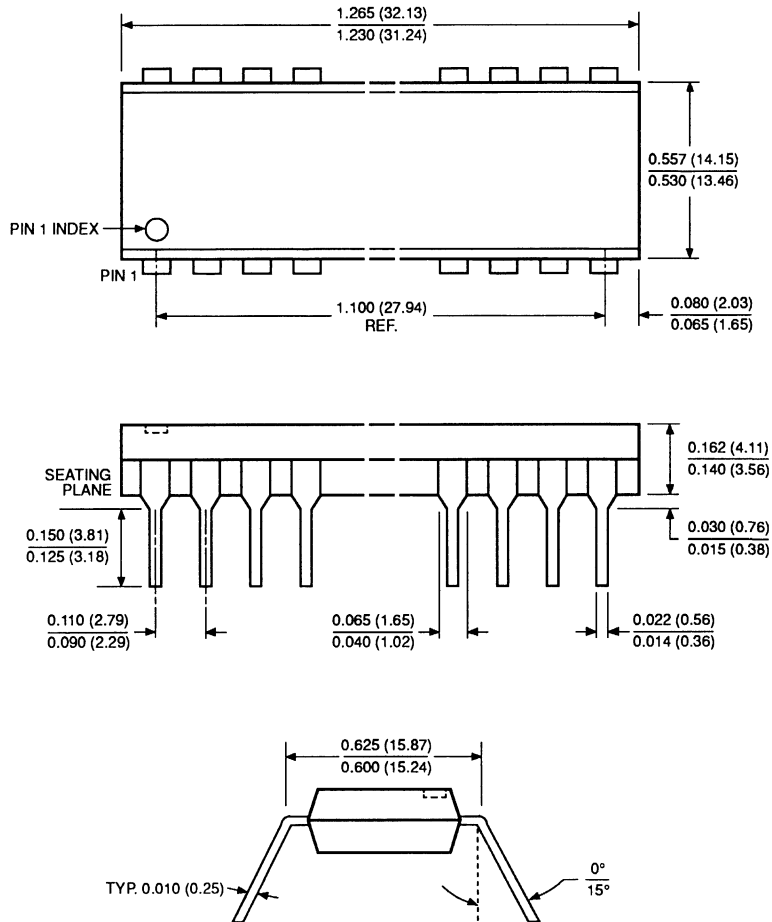


NOTE:  
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)  
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

3926 FHD F18

## Packaging Information

### 24-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



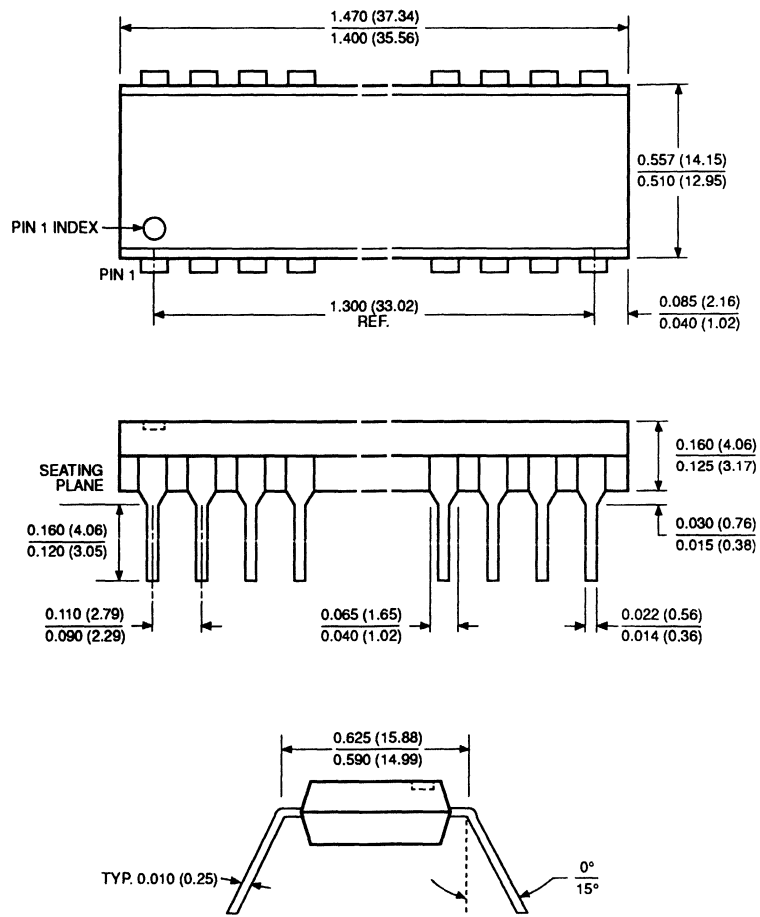
#### NOTE:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

3926 FHD F03

# Packaging Information

## 28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

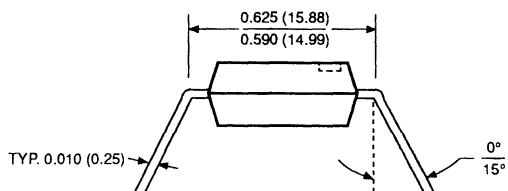
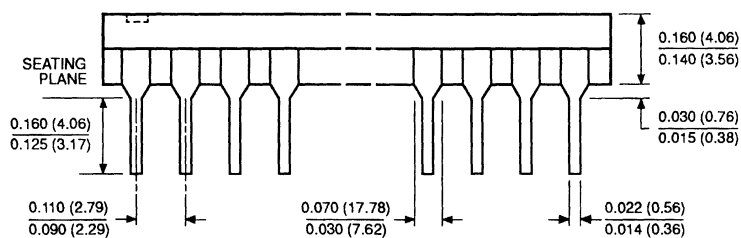
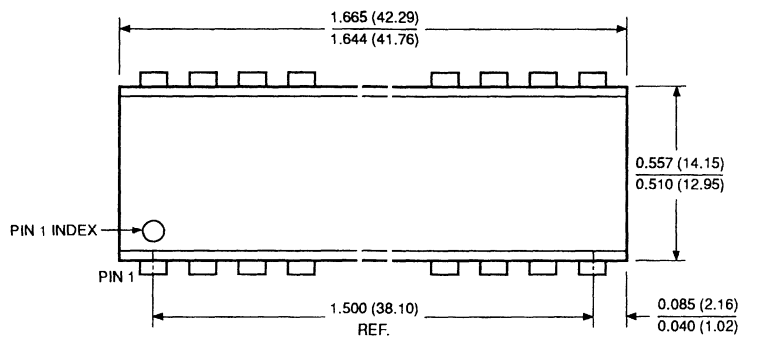


**NOTE:**  
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)  
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

3926 FHD F04

## Packaging Information

### 32-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



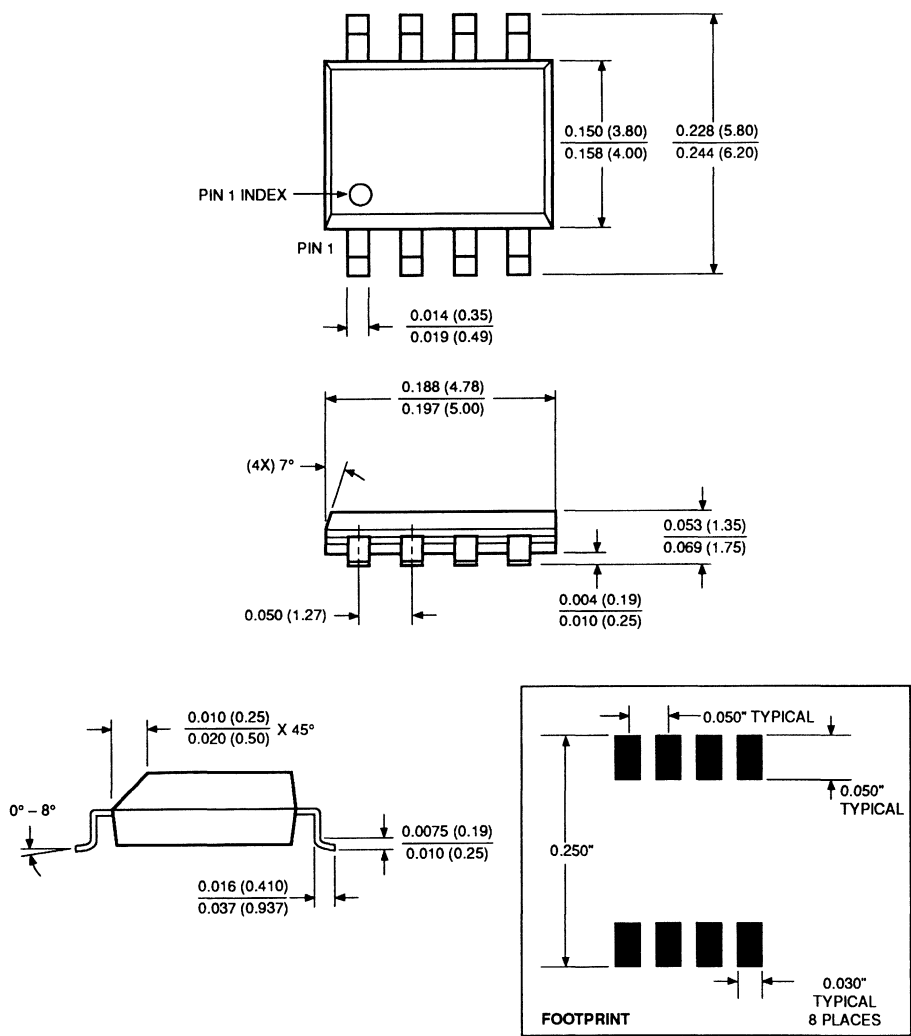
#### NOTE:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

3926 FHD F25

Packaging Information

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



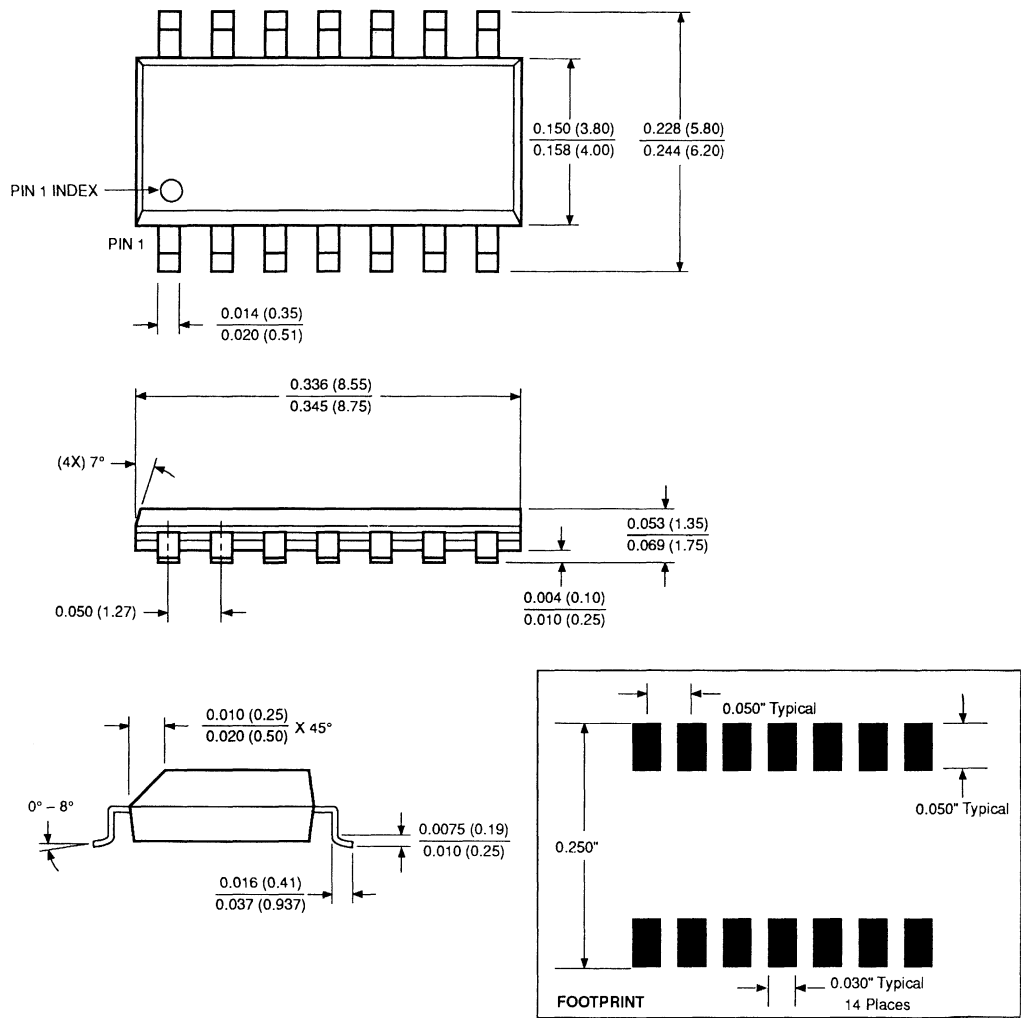
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESIS IN MILLIMETERS)

3926 FHD F22



# Packaging Information

## 14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

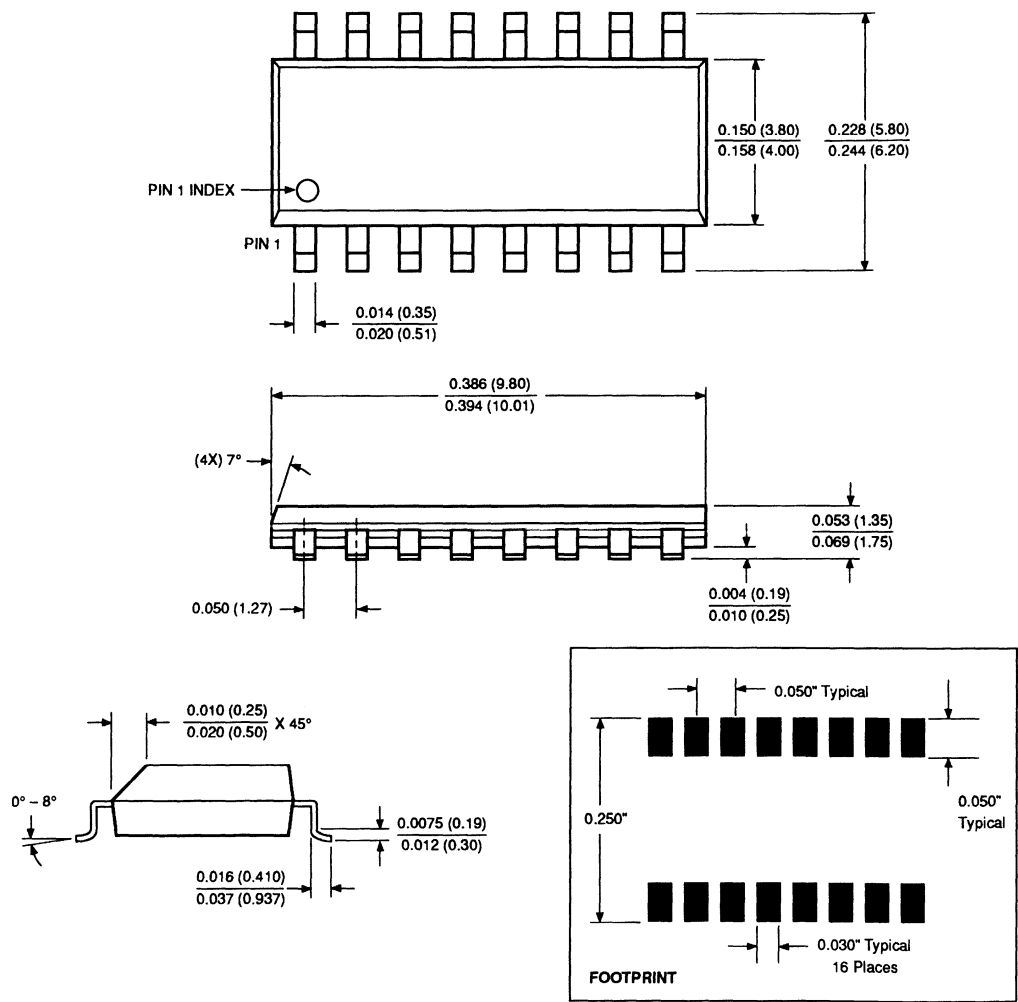


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F10

Packaging Information

16-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

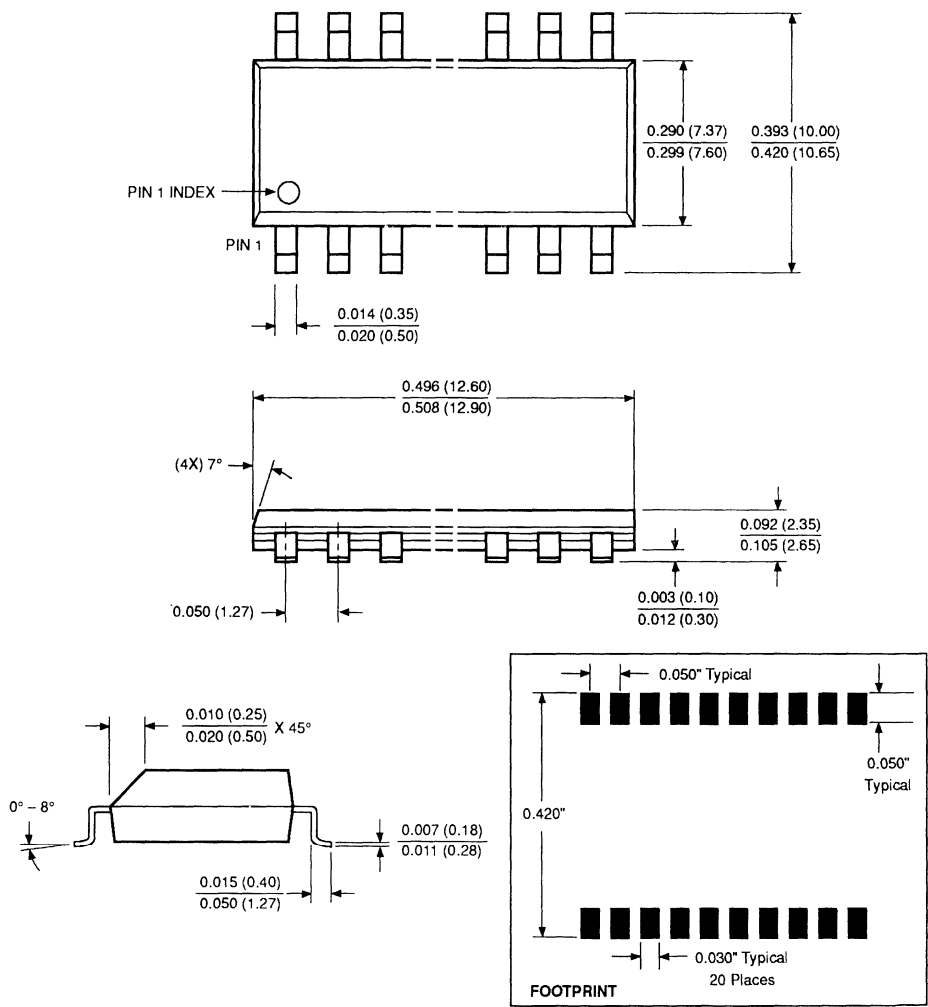


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F26

Packaging Information

20-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F23

## 24-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

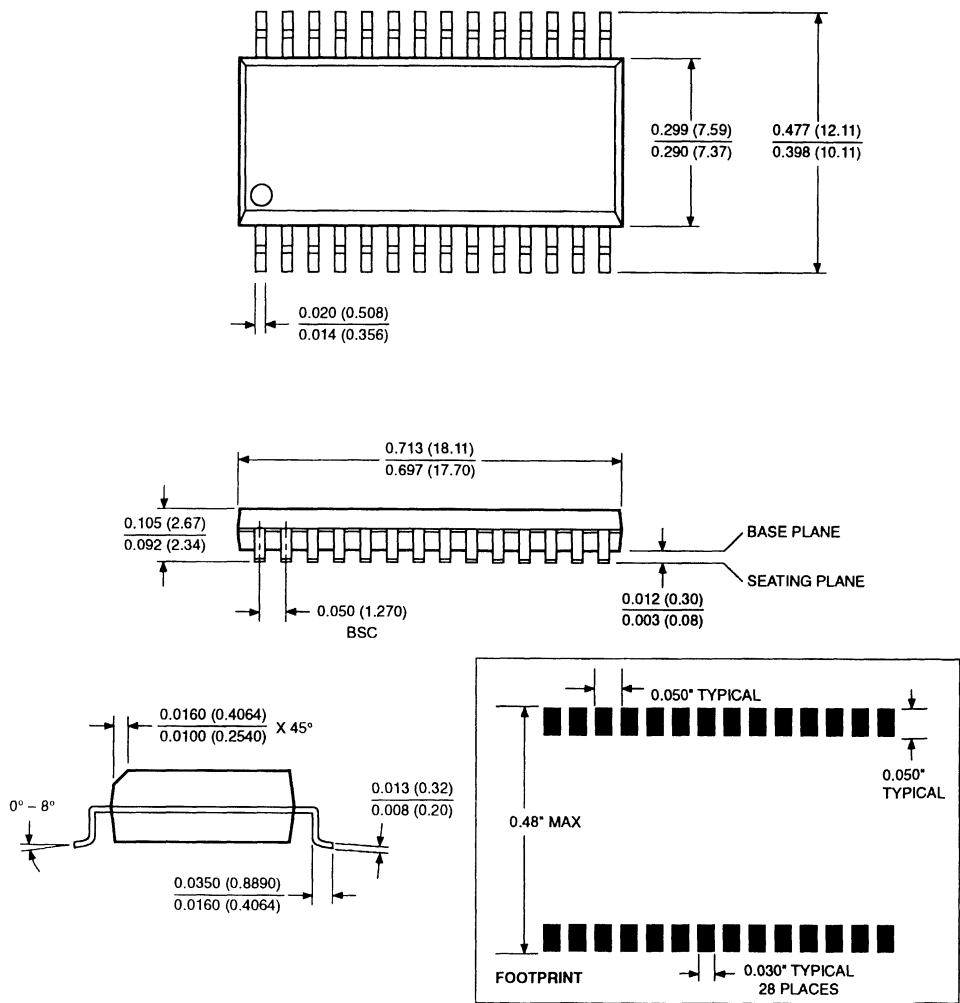


**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**

3926 FHD F24

# Packaging Information

## 28-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

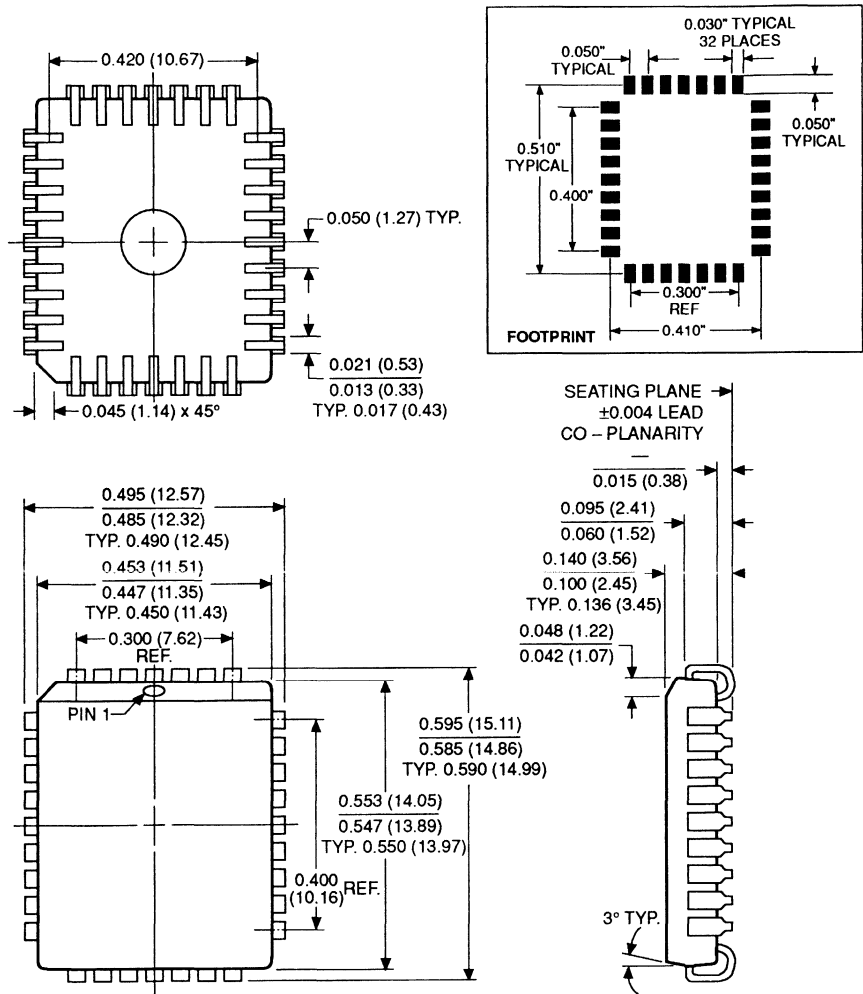


- NOTES:
- 1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
  - 2. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.004 INCHES

3926 FHD F17

Packaging Information

32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J

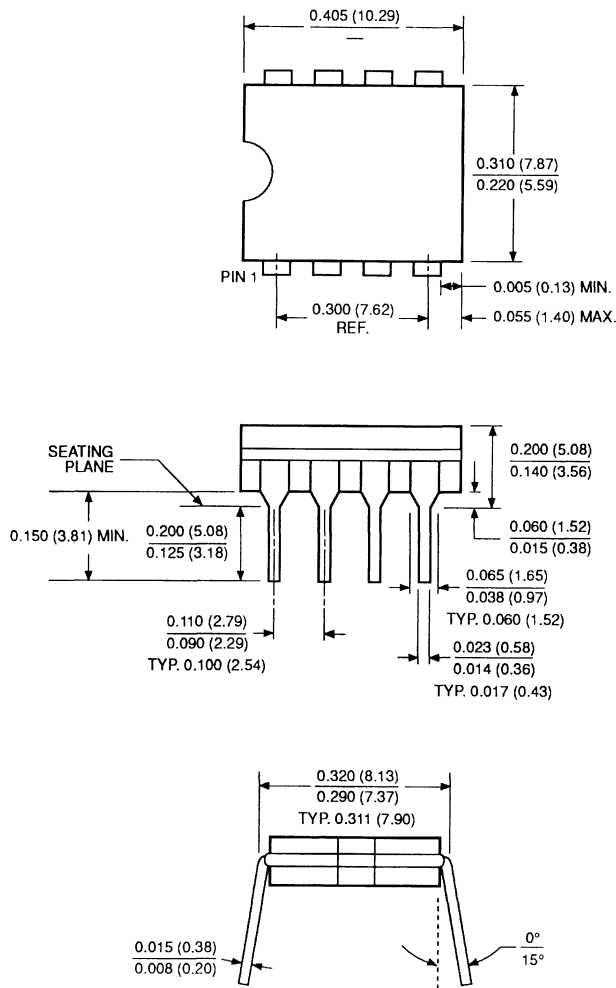


- NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
  2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

3926 FHD F13

# Packaging Information

## 8-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

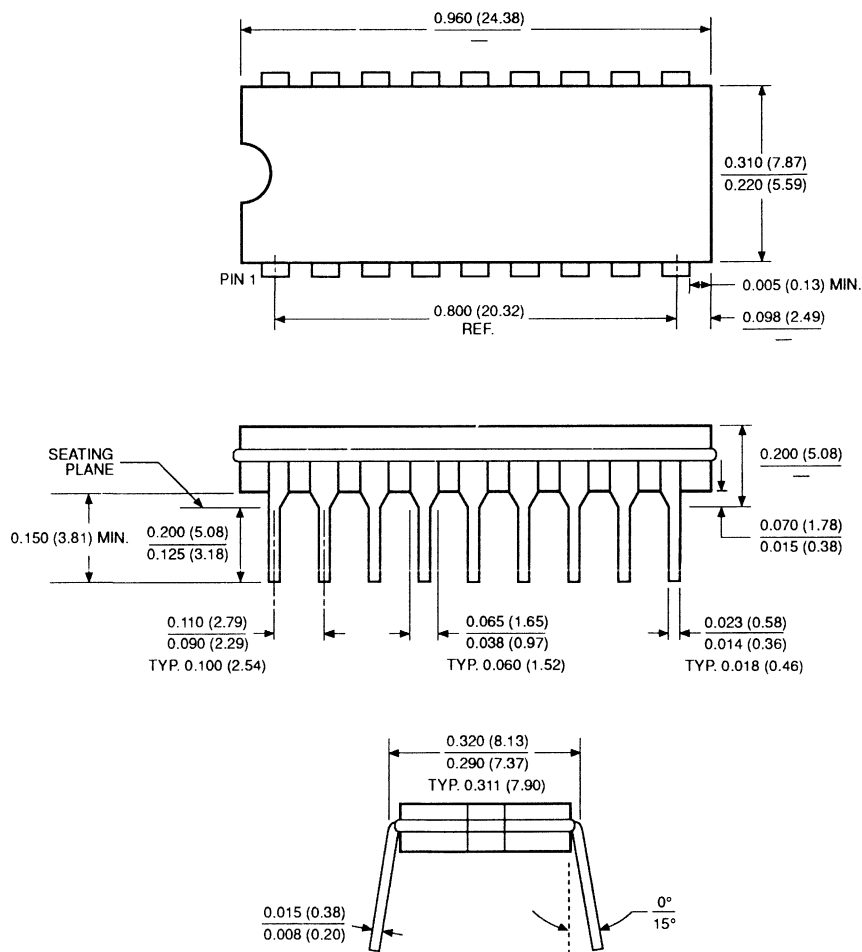


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F05

# Packaging Information

## 18-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

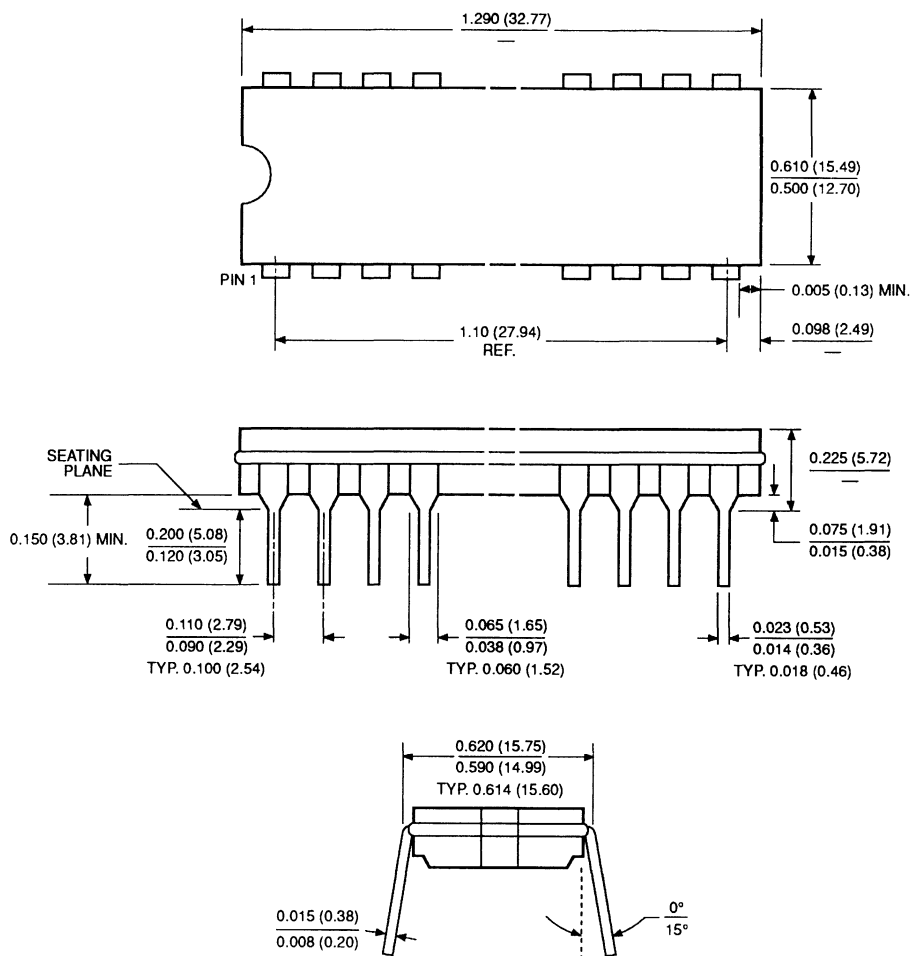


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F06



## 24-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

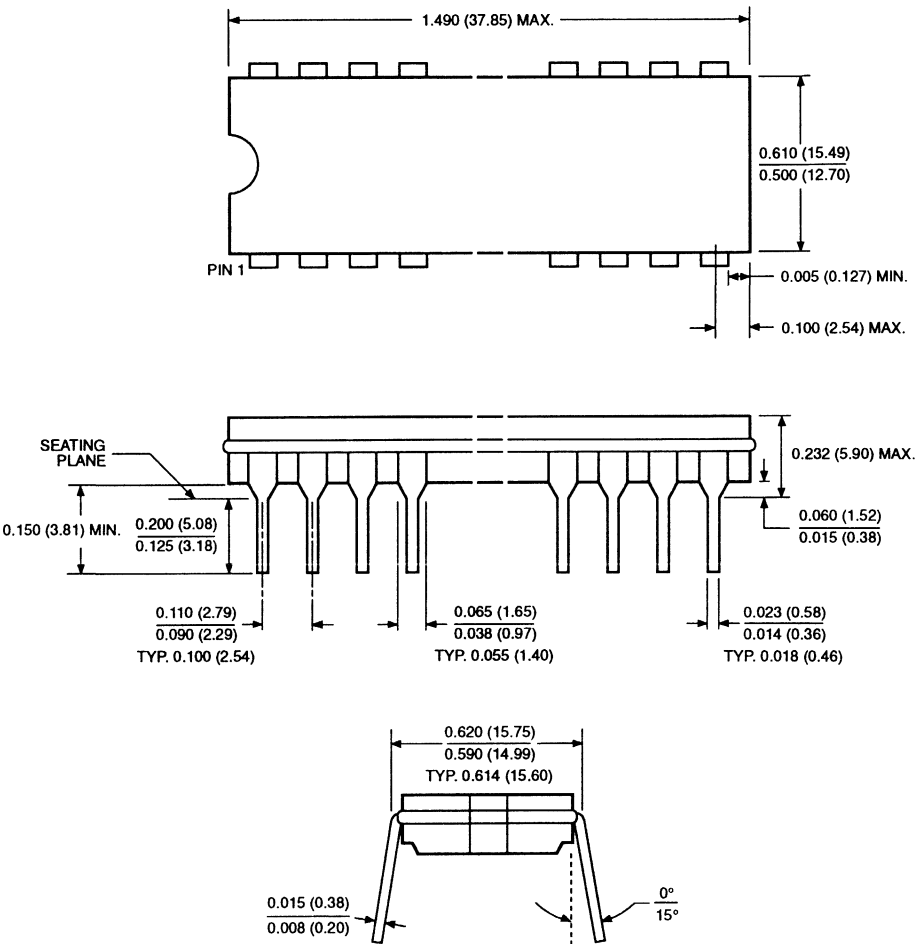


**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**

3926 FHD F07

Packaging Information

28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

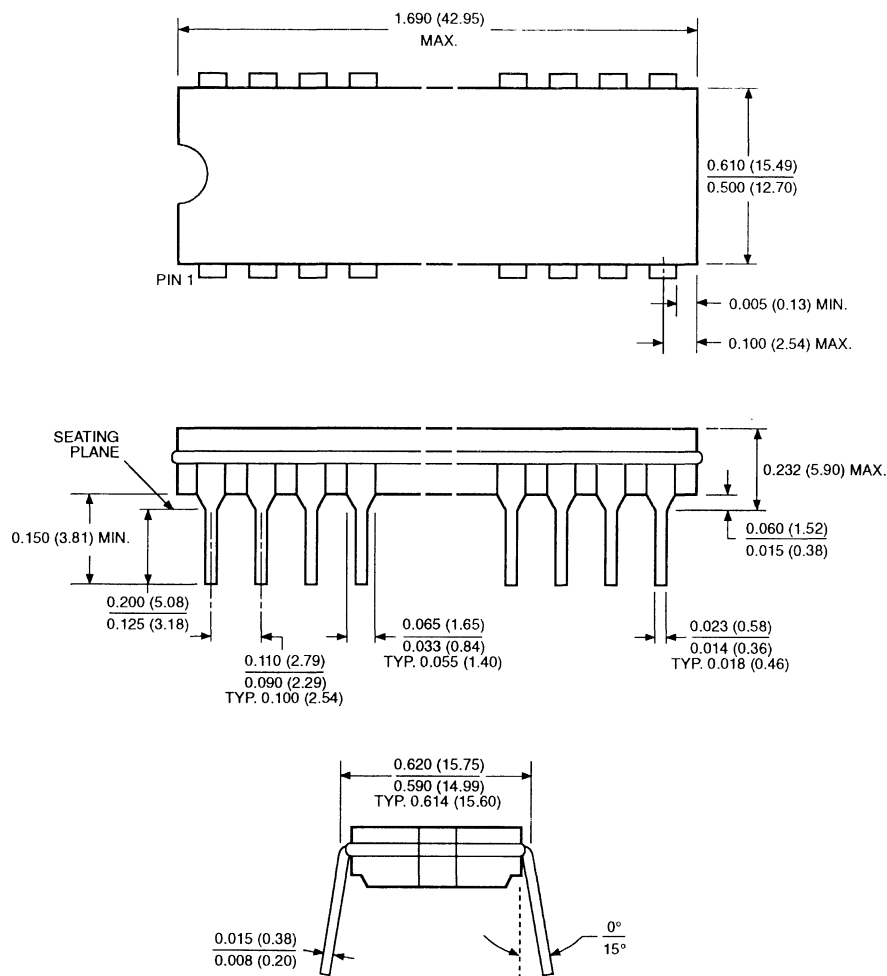


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F08

# Packaging Information

## 32-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

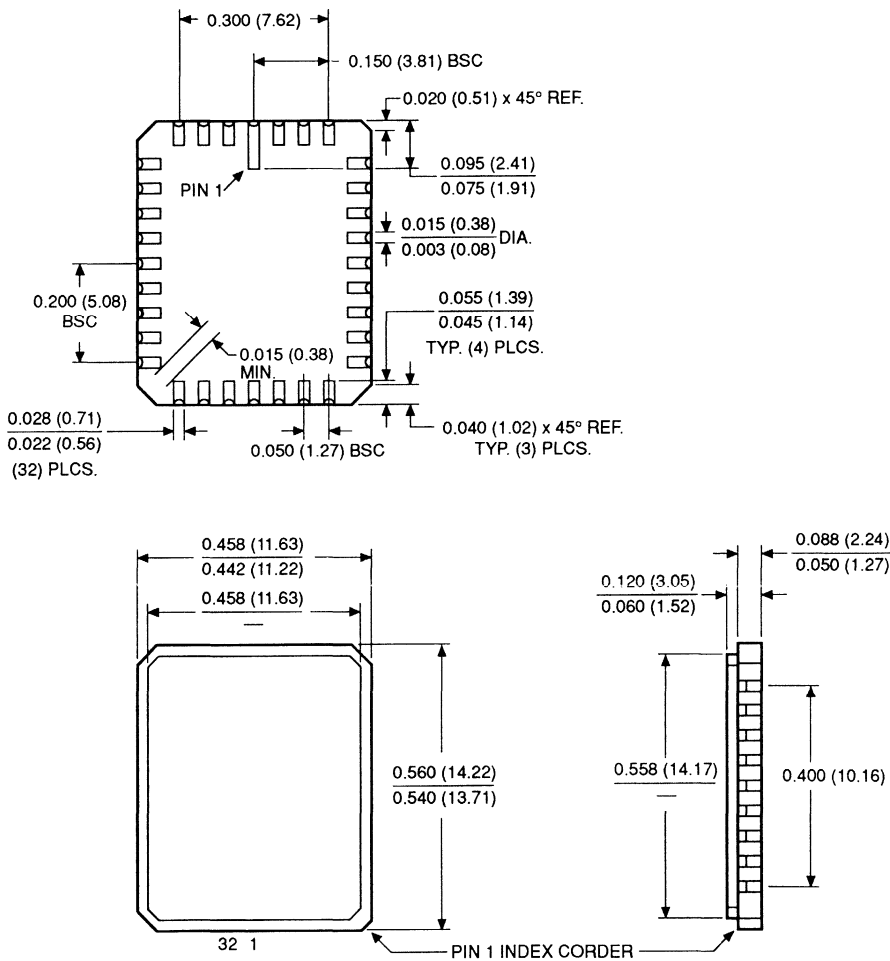


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F09

# Packaging Information

## 32-PAD CERAMIC LEADLESS CHIP CARRIER (GLASS FRIT SEAL) PACKAGE TYPE G

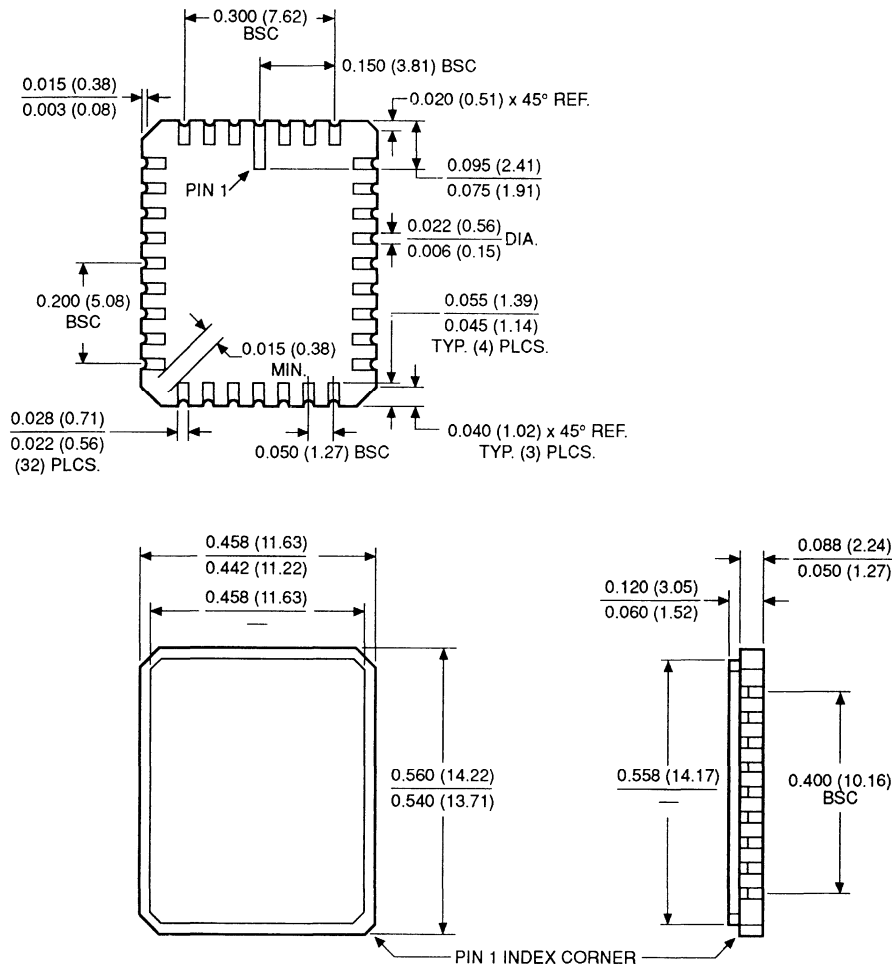


- NOTE:**
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
  2. TOLERANCE:  $\pm 1\%$  NLT  $\pm 0.005$  (0.127)
  3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS

3926 FHD F19

# Packaging Information

## 32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E

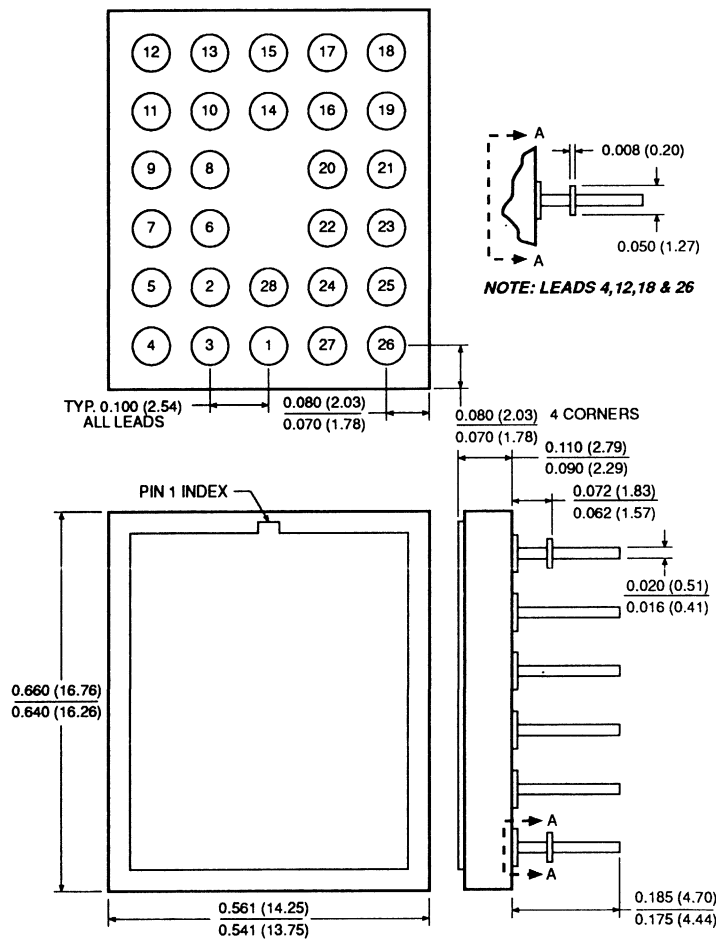


**NOTE:**  
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)  
2. TOLERANCE:  $\pm 1\%$  NLT  $\pm 0.005$  (0.127)

3926 FHD F14

Packaging Information

28-LEAD CERAMIC PIN GRID ARRAY PACKAGE TYPE K

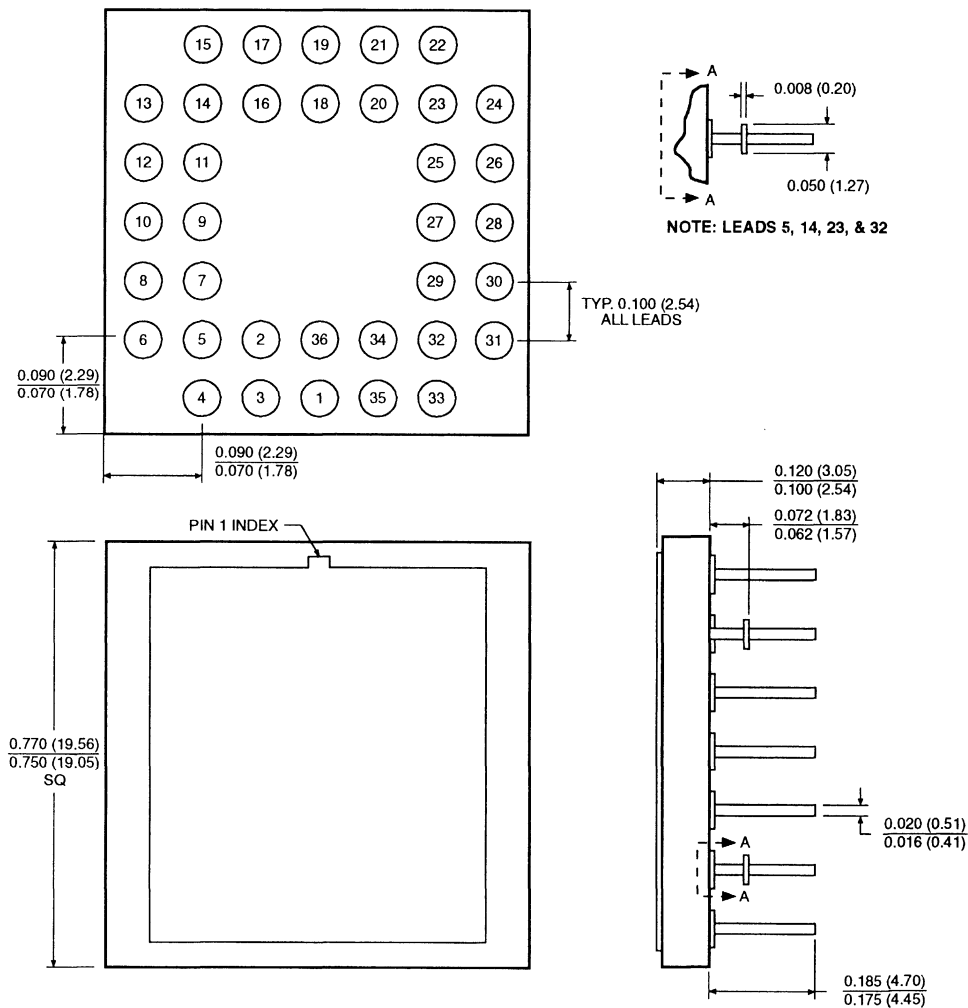


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F15

Packaging Information

36-LEAD CERAMIC PIN GRID ARRAY PACKAGE TYPE K

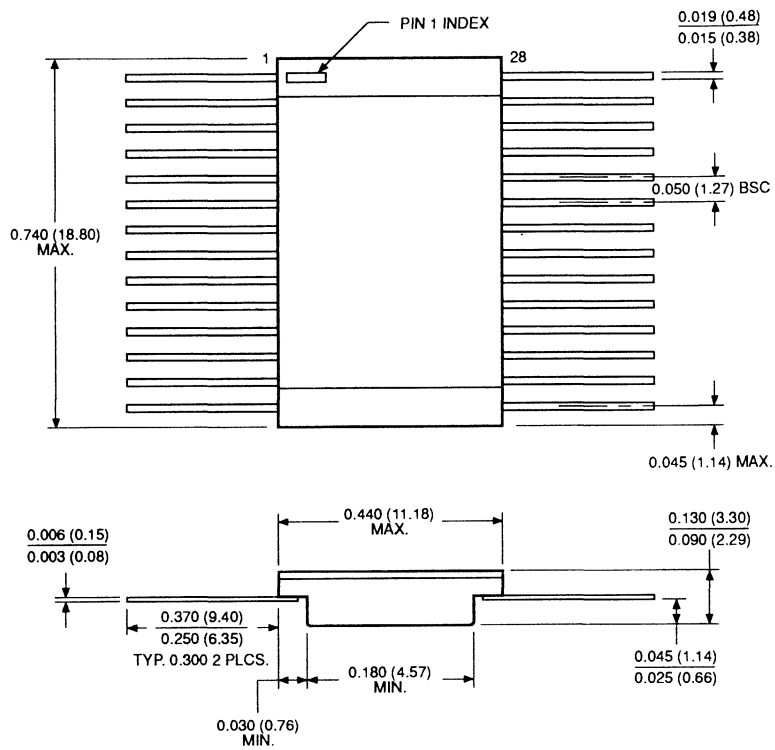


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F21

Packaging Information

28-LEAD CERAMIC FLAT PACK TYPE F

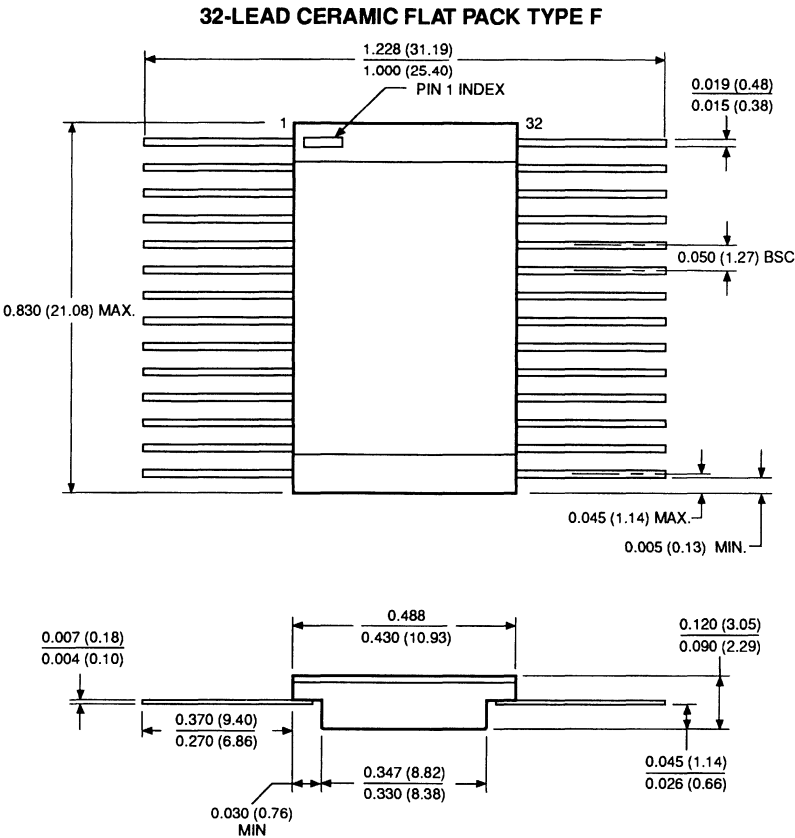


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F16



Packaging Information

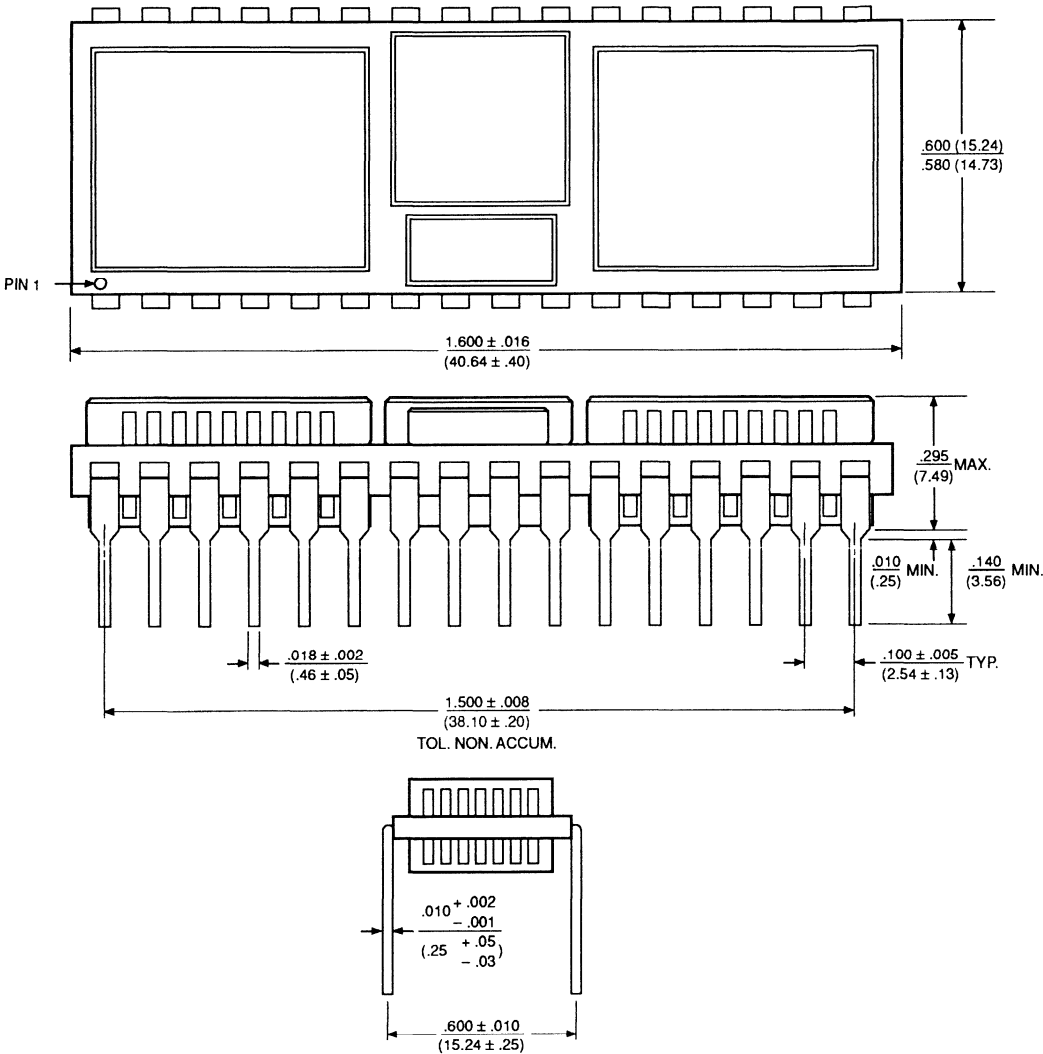


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F20

# Packaging Information

## 32-PIN DUAL-IN-LINE PACKAGE CERAMIC LEADLESS CHIP CARRIERS ON SIDE BRAZED CERAMIC SUBSTRATE

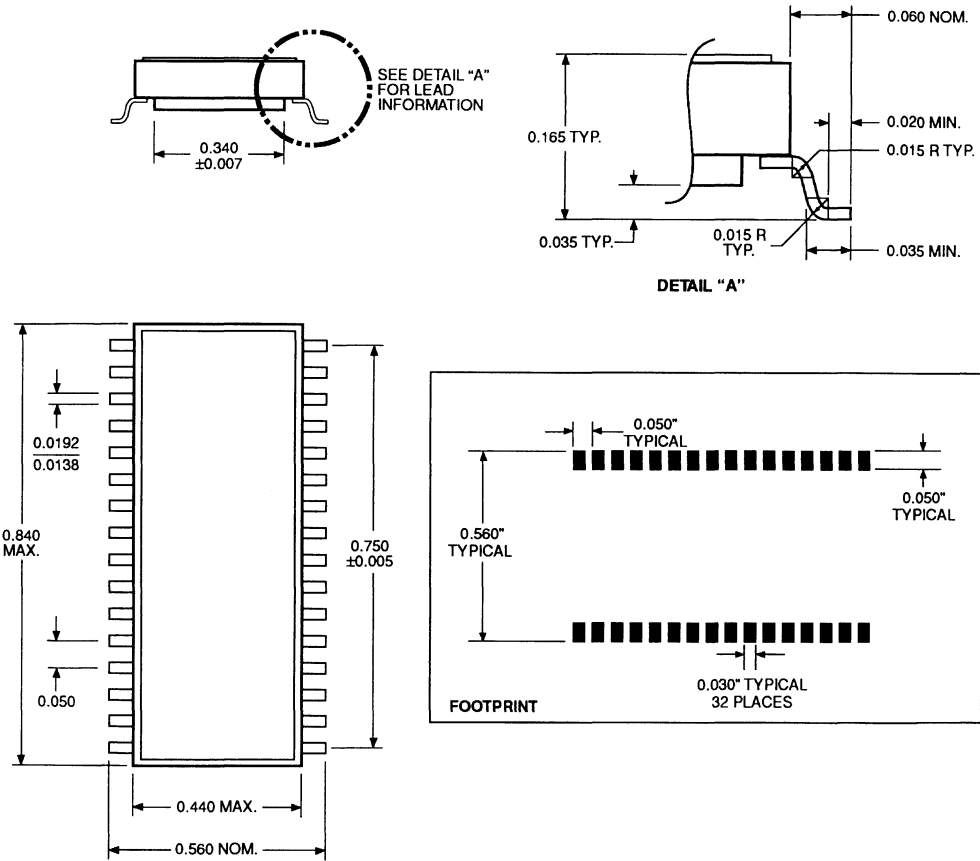


- NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
  2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

3926 FHD F12

# Packaging Information

## 32-LEAD CERAMIC SMALL OUTLINE GULL WING PACKAGE TYPE R



- NOTES:
1. ALL DIMENSIONS IN INCHES
  2. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.004 INCHES

3926 FHD F27

## Sales Offices

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Altamonte Springs, Florida 32701  
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Fax: 714/752-8634

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Fax: 408/980-9478

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Fax: (49) 711.83.80.521

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Fax: (81) 3/3225.2319

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Santa Clara, California 95054  
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Milpitas, California 95035  
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\*NOVRAM is Xicor's nonvolatile static RAM device.



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